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Review

Progress in the developments of $(Ba,Sr)TiO_3$ (BST) thin films for Gigabit era DRAMs

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Abstract

This paper reviews the recent developments of $(Ba,Sr)TiO_3$ (BST) thin films for future Gbit era dynamic random access memory (DRAM) applications. The trends of DRAM capacitors in the last decade are briefly described first. Then the technological aspects of BST films such as deposition techniques, post-annealing, physical, electrical and dielectric characteristics of the films, effects of electrode materials, dielectric relaxation and defect analysis and the reliability phenomena associated with the films are briefly reviewed with specific examples from recent literature. The basic mechanisms that control the bulk electrical conduction and the origin of leakage currents in BST films are also discussed. Finally, possible developments of gigabit era DRAM technology are summarized. © 2000 Elsevier Science S.A. All rights reserved.

Keywords: BST; Thin films; Dielectrics; DRAM capacitors; Leakage current density; Dielectric constant; Reliability

1. Introduction

Previous and today's dynamic random access memories (DRAMs) have been advanced by mainly focussing on how to make memory cells small to realize high density DRAMs. The continuous 'shrink technology' up to Gbit density exposes many challenges. The most critical challenges in gigabit density DRAMs are yield loss due to large die size and small feature size, standby current failure caused by large chip size and small data retention times owing to reduced charge packet in the memory cell. Narrowing the bandwidth mismatch between fast processors and slower memories and achieving low-power consumption together with aforementioned challenges drive DRAM technologies toward smaller cell size, faster memory cell operation, less power consumption and longer data retention time. In addition, a tight control of increasingly complicated wafer processing requires DRAM process technology to be simpler and less sensitive to processing variation. Thus, DRAM technology in Gbit era should solve the challenges imposed by the shrink technology system application requirement and manufacturing technology [1–5].

One of the most critical challenges which Gbit density DRAMs face will be memory cell capacitance. Memory cell capacitance is the crucial parameter which determine the sensing signal voltage, sensing speed, data retention times and endurance against the soft error event. It is generally accepted that the minimum cell capacitance is more than 25 fF per cell regardless of density. However, lower supply voltage and increased junction leakage current due to high doping density drive memory cell capacitance toward higher value more than 25 fF per cell in the Gbit density DRAMs. The strategy to increase memory cell capacitance has been focussed on the increase of the memory cell capacitor area and decrease of the dielectric thickness up to now.

In the memory cell capacitor which is the most important technology in the Gbit era, high dielectric constant capacitor seems to be the only solution [6–8]. In the recent years thin film perovskite materials with high dielectric constant such as PZT, $SrTiO_3$ and $(Ba,Sr)TiO_3$ (BST) [9–25] have been investigated as dielectric materials for future DRAMs. The best suited dielectric material would have a low leakage current and a high dielectric constant and would also be in paraelectric phase to avoid fatigue from ferroelectric domain switching. $SrTiO_3$ has a smaller dielectric constant than BST and PZT is in ferroelectric phase at room temperature. Thus, BST is very appealing for DRAM capacitors.

Barium strontium titanate $(Ba,Sr)TiO_3$ (BST) thin films are being widely investigated as alternative dielectrics for ultra large scale integrated circuits (ULSIs) DRAM storage

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capacitors due to its (1) high dielectric constant (ε_r>200), (2) low leakage current, (3) low temperature coefficient of electrical properties, (4) small dielectric loss, (5) lack of fatigue or aging problems, (6) high compatibility with device processes, (7) linear relation of electric field and polarization and (8) low Curie temperature [11–13,26–31]. However, whether or not BST thin film can be successfully applied largely depends on more thorough understanding the material's properties. The deposition techniques and electrical properties of BST films have received increasing interest. According to those investigations the electrical and dielectric properties and reliability of BST films heavily depend upon the deposition process, post-annealing process, composition, base electrodes, microstructure, film thickness, surface roughness, oxygen content and film homogeneity.

Successful applications of any thin film material require the development of sophisticated synthesis and processing techniques, the understanding of structure–property relationships and the implementation of various novel devices. The purpose of this paper is to present an overview of BST film production methods, electrode selection, microstructure–property relationships, leakage current reduction and reliability of the film and its applicability to the processing of the next generation of ultra-large-scale integrated (ULSI) DRAMs.

In this review, we first describe the different methods of BST thin film material processing, since they are the ultimate factors determining the oxide properties. We then look into the main physical and electrical characteristics, highlighting some well established experimental results. Specific examples from the recent literature are reviewed to exemplify how the technique has been utilized to date in solid state technology. The general theories of electrical conduction mechanisms and the various methods of leakage current reduction are reviewed in order to check the limits of their applicability to ULSI. Background information is given on the materials chemistry and physics and over 164 references are cited. The paper will end with a critical review of summary and future trends.

1.1. Trends in the development of ULSI DRAM capacitors

The capacitor materials currently utilized in DRAMs are either silicon dioxide (SiO_2) or a silicon oxide/nitride composite layer (ONO) with a relative dielectric constant of 6. Use of SiO_2 or ONO allows the memory cell to be fabricated as a metal-oxide-semiconductor (MOS) device. As the number of memory cells increase to gigabits, the available area for the capacitor decreases rapidly (≈0.4 μm^2 for a 256-Mbit device and 0.2 μm^2 for a 1-Gbit device) to maintain acceptable die sizes. Table 1 indicates that the capacitance-per-unit area should be increased to achieve higher DRAM densities [32]. For maintaining sufficient storage capacitance of memory cell, manufacturers have abandoned the idea of flat integrated circuits and three-dimensional cell structures were consequently incorporated by use of deep trenches and stacked layer to offer more surface area. So far, these structures with ONO storage dielectrics can adhere to the requirements of 256-Mbit DRAMs. The capacitor areas will be close to 0.2 and 0.1 μm^2 for future 1-Gbit and 4-Gbit DRAMs, respectively, and there is a requirement that the capacitance per unit area be increased as shown in Table 1. The ONO dielectrics will not be used in these products since the capacitor area cannot be maintained constant in a cell that is still manufacturable and also the ONO dielectric thickness has reached a lower limit set by electron tunneling through the dielectric [33,34]. Consequently, an increasing effort has been made in search of alternative dielectric having a substantially higher permittivity.

The first step in the direction of high dielectric constant materials is to consider some single metal oxide materials such as Ta_2O_5, TiO_2, or others. Table 2 illustrates the dielectric constant and critical capacitance (defined as the maximum capacitance-per-unit area that can be achieved for a film that satisfies DRAM leakage requirements) [35] for various single metal oxides that present dielectric constant values in the range 10–100. As can be seen, the highest capacitance values can be obtained for Ta_2O_5 films. These

Table 2
Medium dielectric constant materials [35]

Dielectric	ε (thick films)	C_{crit} (fF μm^{-2})[a]	Growth
Ta_2O_5	25	13.8 (20.4)	MOCVD
	50		Sputtering
TiO_2	30–40	9.3	MOCVD
ZrO_2	14–28	9.9	MOCVD
Nb_2O_5	30–100	–	–
Y_2O_3	17	4.7	Sputtering
Si_3N_4 (comparison)	7	7–8.6 (120)	MOCVD

[a] The values in parenthesis are given for the case of a HSG-rugged Si capacitor.

Table 1
The road map of DRAM technology [32]

	Minimum feature size (μm)	*C*/*A* (fF μm^{-2})	Capacitor area (μm^2)	Operating voltage (V)	Year[a] 1 Million devices
16 Mbit	0.60	25	1.10	3.3	1992
64 Mbit	0.35	30	0.70	3.3	1995
256 Mbit	0.25	55	0.35	2.2	1998
1 Gbit	0.18	100	0.20	1.6	2001
4 Gbit	0.15	140	0.10	1.1	2004

[a] Year in which 1 million devices were/are projected to be produced.

Table 3
High dielectric constant materials for DRAM applications [35]

Dielectric	ε	t (nm)	C_{crit} (fF μm^{-2})	References
$SrTiO_3$	230	53	55.0	[14]
$(Ba_{1-x}Sr_x)$ TiO_3 (BST)	320	70	40.5	[42]
	800	60	118.1	
Ba $(Ti_{0.8}Sn_{0.2})TiO_3$ (BTS)	210	100	–	[43]
(Ba,Pb) (ZrTi)O_3 (BPZT)	200	200	8.9	[44]
$(Pb_{1-x}La_x)$ TiO_3 (PLT)	1400	500	24.8	[45]
(Pb,La) (Zr,Ti) O_3 (PLZT)	1474	150	87.0	[46]
$(PbZr_{1-x})$ Ti_xO_3 (PLT)	>1000	70	>70.0	[47]

films are also compatible with MOS fabrication facilities and can be easily deposited by the chemical vapor deposition (CVD) technique required to form complex 3D features. Integration issues relative to the choice of electrodes, in particular, a top CVD-TiN electrode is needed and post-deposition annealings have to be limited to obtain the best film properties, before such film can be used in mass production [36,37]. The reported storage capacitances for Ta_2O_5 are around 10–20 fF m^{-2} [38]. If utilized at all, it appears that Ta_2O_5 will only be appropriate for one DRAM generation [38–41].

On the other hand, ferroelectric materials are considered the ideal DRAM dielectrics for the Gbit era since they exhibit dielectric constants in the range 200–2000 range. These values are much lower, however, when thin films are considered. For DRAM applications, ferroelectric films that are in the paraelectric phase in the DRAM operating temperature range should be considered to benefit from the full stored charge during the read operations. Table 3 lists some of the most promising ferroelectric material candidates for DRAM applications. Among this, $(Ba_{1-x}Sr_x)TiO_3$ (BST) films have recently been investigated as the most promising capacitor material in future DRAM applications because the films have the advantages of a low leakage current, a room temperature paraelectric with a high dielectric constant and a large dielectric breakdown strength [41–48]. High dielectric BST capacitor is basically formed in metal-insulator-metal (MIM) structure. In this MIM structure, the storage poly-silicon electrode is replaced with metal electrode. By using a proper metal electrode to have strong resistance to native oxide, the native oxide on storage electrode can be completely removed. Pt-storage node electrode is one of the good examples for metal to have strong resistance to oxidation. Therefore, MIM cell capacitor using BST dielectric seems to be the ultimate solution for the Gbit era. Fig. 1 compares the leakage capacitance characteristics of BST, Ta_2O_5 and ONO dielectrics to illustrate the considerable improvement that can be obtained with such materials. While the capacitance improvements are clear, the integration issues faced with the introduction of these new materials are not simple.

Although the BST capacitor can provide the sufficient cell capacitance for the Gbit era, many issues regarding BST capacitor should be solved. The key issues of BST capacitor are barrier height between metal electrodes and BST dielectric, thickness dependent dielectric constant, crystallization temperature after BST film deposition, the barrier layers between storage electrode and poly-silicon plug and its resistance to oxidation during crystallization temperature and electrode formation. The current conduction of BST capacitor is known to be governed by Schottky emission current [50]. Since the Schottky conduction current is strongly dependent on the barrier height between metal electrode and BST, the metal electrode giving a higher barrier height is needed. It is very important to control surface property of metal electrode and interface property between metal electrode and BST in order to maintain good barrier property. The dielectric constant of BST is known to be dependent on the thickness of the BST film [51]. As BST film thickness decreases, the dielectric constant decreases. This can be explained by the lower dielectric constant resulting in depletion region between metal and BST dielectric. The deposited BST dielectric requires a high temperature annealing around 750°C in O_2 ambient in order to achieve crystalline structure. Crystalline structures of BST film is found to have higher dielectric constant and lower leakage current density [52]. During high-temperature annealing in O_2 ambient, considerable amount of oxygen penetrates storage Pt electrode, resulting in oxidizing poly-silicon at the interface between plugged poly-silicon and BST film. Therefore, the barrier

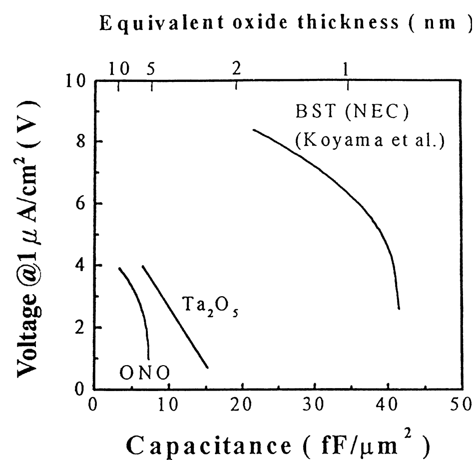

Fig. 1. Voltage at 1 μA cm^{-2} vs. capacitance for ONO, Ta_2O_5 and BST capacitors [35].

layer to block the oxygen penetration is needed between Pt electrode and plugged poly-silicon. The barrier layer should have resistance to oxygen penetration at high annealing temperature. Unfortunately, TiN/Ti barrier commonly used in current metallization scheme is not proper because of loss of barrier property around 500°C. Another thing is the electrode formation because it determines the surface area of capacitor. A more vertical etching profile of storage node and a larger capacitor area can be achieved. So far the Pt electrode is found to have superior leakage current characteristics as well as the highest capacitance [38,41]. But Pt is very difficult to etch vertically [53]. Ru or RuO_2 electrodes are found to be easy in vertical etching. However, Ru or RuO_2 based BST capacitor suffers from higher leakage current and lower dielectric constant. Therefore, the above mentioned issues need to be fully understood before BST films are subjected to mass production. In the following sections, we have addressed these issues in detail by making use of the extensive research work carried out on BST films by various groups.

1.2. Barium strontium titanate (BST) thin films

$BaTiO_3$ is a ferroelectric perovskite and has been well studied in bulk ceramic form where the measured permittivities are well into the thousands. The utilization of the $BaTiO_3$–$SrTiO_3$ solid solution allows the Curie temperature (ferroelectric–paraelectric transition temperature, T_c) of $BaTiO_3$ can be shifted from 120°C to around room temperature for $Ba_{1-x}Sr_xTiO_3$ films. For Sr addition into $BaTiO_3$, the linear drop of T_c is ca. 3.4°C per mol%. Therefore, 30 mol% Sr (x=0.3) would bring the T_c down to room temperature. The effect of several isovalent substitutions on the transition temperatures (Curie temperature) of ceramic $BaTiO_3$ is as shown in Fig. 2 [6,28,42,46,49]. $Ba_{1-x}Sr_xTiO_3$ films are not only paraelectric at the DRAM operating temperature range (0–70°C ambient and 0–100°C on chips) [33], but also achieve maximum permittivity around the operating temperature. On the other hand, the volatilities of the BST components are lower than Pb-based ferroelectric materials, thereby making it relatively easier to introduce into fabrication facilities [33,34].

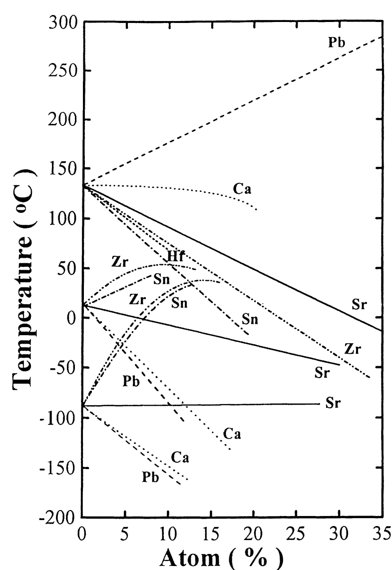

Fig. 2. Effect of several isovalent substitutions on the transition temperature of ceramic $BaTiO_3$ [49].

BST films are polycrystalline. Their properties heavily depend on composition, stoichiometry, microstructure (grain size and size distribution), film thickness, characteristics of electrode, and homogeneity of the film. The BST thin film growth method significantly affects the composition, stoichiometry, crystallinity, and grain size of the film and, consequently, its dielectric properties. A variety of techniques such as rf-sputtering [42,46,51,52], laser ablation [79], metal-organic deposition (MOD) [54,55], chemical vapor deposition (CVD) [56–58], and sol–gel processing [59] have been used to deposit BST thin films. Above methods are highly competitive, each having advantages and disadvantages in terms of homogeneity, processing temperature, and processing costs. Because of the multicomponent nature of BST materials precise microscopic control of stoichiometry is essential for obtaining uniform single phase films.

The basic parameters for applying capacitor thin films on DRAMs are dielectric constant, leakage current density and reliability. The targets for ideal Gbit era DRAM dielectrics include the followings [33]: (i) SiO_2 equivalent thickness <0.2 nm for Gbit; (ii) leakage current density $<1\times10^{-7}$ A cm^{-2} at 1.6 V; (iii) life time 10 years at 85°C and 1.6 V; (iv) stability 10^{15} cycles at >100 MHz; and (v) general compatibility to semiconductor processing.

2. Materials processing

Deposition process are generally divided into two categories: physical vapor deposition (PVD); and chemical vapor deposition (CVD). CVD is of the most interest since PVD processes such as evaporation and sputtering do not generally produce films of the same quality as CVD processes. The commonly used techniques for depositing dielectric thin films include low pressure chemical vapor deposition (LPCVD), metal organic chemical vapor deposition (MOCVD), sputtering, pulse laser ablation, and sol–gel methods. Each technique has its merit and drawbacks. For example, MOCVD can be used for large scale production but elevated growing temperature is required for cracking the metal-organic (MO) source. Pulse laser ablation is suitable for low temperature epitaxial growth but it can only process samples on limited scale. Thin films are used in a host of different applications in ULSI fabrication and can be prepared by a variety of techniques. Regardless of the method by which they are formed, however, the process must be economical and the resultant films must exhibit the following characteristics: (a) good thickness uniformity; (b) high purity and density; (c) controlled composition

stoichiometries; (d) high degree of structural perfection; (e) good electrical properties; (f) excellent adhesion; and (g) good step coverage [60].

In the recent, rapid thermal annealing (RTA) has become more important in the application on ULSI technologies, such as thin dielectric deposition, polysilicon growth, shallow junction formation, silicidation and annealing [61,62]. The great advantages of the technique are a rather short processing time and its relative process simplicity as compared with the conventional furnace apparatus. A short processing time will be beneficial to reduce the time–temperature product such that the physical or chemical processes are completed while unwanted processes such as dopant diffusion penetration, interface reactions and decomposition are effectively controlled. Rapid thermal N_2O annealing (RTN_2O) has been applied to reduce the leakage current in the BST films prepared by CVD [33].

Table 4 shows the comparison of the best properties of BST films prepared by various methods. Among the various techniques described above, the most common techniques that have been frequently utilized to deposit BST thin films are dc and rf-sputtering, CVD, PECVD, MOCVD, LSCVD, ECR-CVD, laser ablation and sol–gel method. For application to storage capacitors, the dielectric films must have a very small leakage current to maintain the favorable retention characteristics and in the case of topography for three-dimensional memory cells have the ability for excellent step coverage. DC or rf-sputtering deposition has the advantage of depositing BST films at low temperatures, which is very desirable for applications where the processing temperature or thermal budget is a major concern. A major difficulty in the sputtering deposition technique is choosing the process conditions to obtain stoichiometric BST films at the highest deposition rate. Several researchers have investigated the sputtering deposition process and have proposed different criteria of the deposition condition for preparing stoichiometric BST films.

Although as-deposited sputtered films have low leakage currents in amorphous phase, the high temperature treatments, which are necessary for standard DRAM processes, will lead to the crystallization of these films and hence a drastic increase in the leakage current [33,41]. This, obviously, limited their application on DRAMs in terms of the refresh characteristics of the cells. ECR-CVD process provides lower processing temperature (≤500°C), for BST films thereby keeps the leakage current at the lower level

Table 4
Comparison of electrical data from BST samples prepared by various deposition techniques

Deposition techniques	Composition	Film thickness (nm)	Dielectric constant	Leakage current density ($A\,cm^{-2}$) @ $100\,kV\,cm^{-1}$	Dielectric strength ($MV\,cm^{-1}$) @ $10^{-6}\,A\,cm^{-2}$	Capacitor structure (Top/BST/Bottom)	References
rf-Sputtering	$Ba_{0.75}Sr_{0.25}TiO_3$	80	320	1×10^{-8}	0.5	Pt/BST/Pt	[63]
rf-Sputtering	$Ba_{0.75}Sr_{0.25}TiO_3$	60	400	1×10^{-7}	0.5	Pt/BST/Pt	[64]
rf-Sputtering	$Ba_{0.65}Sr_{0.35}TiO_3$	100	400	5×10^{-9}	0.35	Pt/BST/Pt	[65]
rf-Sputtering	$Ba_{0.5}Sr_{0.5}TiO_3$	100	470	3×10^{-9}	0.5	TiN/BST/Pt	[66]
rf-Sputtering	$Ba_{0.5}Sr_{0.5}TiO_3$	100	600	3×10^{-7}	0.3	Pt/BST/Pt	[67]
rf-Sputtering	$Ba_{0.5}Sr_{0.5}TiO_3$	100	250	3×10^{-7}	0.7	Pt/BST/LNO	[68]
rf-Sputtering	$Ba_{0.5}Sr_{0.5}TiO_3$	60	200	1×10^{-8}	1	Pt/BST/SRO	[69]
rf-Sputtering	$Ba_{0.5}Sr_{0.5}TiO_3$	36	338	2×10^{-8}	0.69	Pt/BST/Ir Pt/BST/IrO_2	[70]
rf-Sputtering	$Ba_{0.5}Sr_{0.5}TiO_3$	100	375	8×10^{-9}	1.6	Pt/BST/Pt	[71]
rf-Sputtering	$Ba_{0.5}Sr_{0.5}TiO_3$	100	230	8×10^{-8}	0.5	BRO/BST/BRO	[72]
rf-Sputtering	$Ba_{0.5}Sr_{0.5}TiO_3$	20	274	8×10^{-9}	1	SRO/BST/SRO	[73]
rf-Sputtering	$Ba_{0.5}Sr_{0.5}TiO_3$	75	350	1×10^{-7}	–	LSCO/BST/LSCO	[74]
rf-Sputtering	$Ba_{0.5}Sr_{0.5}TiO_3$	120	600	10^{-9}	–	Pt/BST/TiO_2/Pt	[75]
rf-Sputtering	$Ba_{0.5}Sr_{0.5}TiO_3$	100	573	10^{-7}	–	Pt/BST/RuO_2	[76]
ECR-sputtering	$Ba_{0.55}Sr_{0.45}TiO_3$	200	320	2×10^{-7}	0.09	Pt/BST/Pt	[77]
Excimer laser ablation	$Ba_{0.5}Sr_{0.5}TiO_3$	200	375	5×10^{-7}	0.15	Pt/BST/Pt	[78]
Excimer laser ablation	$Ba_{0.5}Sr_{0.5}TiO_3$	500	467	10^{-7}	–	Au/BST/Pt	[79]
MOCVD	$Ba_{0.7}Sr_{0.3}TiO_3$	40	450	2×10^{-8}	0.7	Pt/BST/Pt	[80]
MOCVD	$Ba_{0.7}Sr_{0.3}TiO_3$	40	210	1×10^{-8}	0.37	Ir/BST/Pt	[66]
ECR-MOCVD	$Ba_{0.4}Sr_{0.6}TiO_3$	100	600	7×10^{-7}	0.15	Al/TiN/BST/RuO_2	[81]
ECR-PCVD	$Ba_{0.5}Sr_{0.5}TiO_3$	27	140	1×10^{-8}	0.44	Pt/BST/Pt	[82]
LSCVD	$Ba_{0.5}Sr_{0.5}TiO_3$	200	300	3×10^{-7}	0.15	Pt/BST/Pt	[83]
LSCVD	$Ba_{0.5}Sr_{0.5}TiO_3$	50	200	1×10^{-8}	0.35	Pt/BST/Pt	[84]
LSCVD	$(Ba, Sr)_{1+x}TiO_{3+x}$ $x=\pm0.2$	30	260	1×10^{-7}	–	Pt/BST/Pt	[85]
CVD	$Ba_{0.5}Sr_{0.5}TiO_3$	100	400	8×10^{-8}	0.7	Pt/BST/Pt	[86]
MOD	$Ba_{0.7}Sr_{0.3}TiO_3$	140	420	1×10^{-9}	0.43	Pt/BST/Pt	[54]
MOD	$Ba_{0.7}Sr_{0.3}TiO_3$	300	563	10^{-6}	–	Au/BST/Pt	[87]
MOD	$Ba_{0.7}Sr_{0.3})(Ti_{0.95}Nb_{0.05})O_3$	300	250	2×10^{-6}	–	Au/BST/Pt	[87]

($<10^{-6}$ A cm^{-2}) and also helps to use various multiple electrode structures such as RuO_2/Ru/TiN/$TiSi_x$, which are not stable otherwise at higher temperatures >750°C [88] The as-deposited CVD BST films have rather leaky current characteristics due to oxygen deficiency and impurity contamination existing in films, this can be significantly reduced to acceptable levels for applications by annealing techniques. Reports indicate that RTA processed BST thin films in O_2 or N_2O ambients showed better electrical characteristics [33,41]. CVD BST films can provide better step coverage ability and good thickness uniformity across the wafer. Thus, based on the consideration of the electrical characteristics and step coverage, CVD BST is more suitable for application to mass production.

3. Factors that influences BST thin film properties

The parameters that have been identified to affect the properties of BST film capacitors are processing methods, annealing conditions, microstructure, interface structure, electrode materials and their correlation. These factors are discussed briefly as follows.

3.1. Processing methods

A variety of deposition techniques, such as rf- and ion-beam sputtering, laser ablation, chemical vapor deposition, metallo-organic deposition and sol–gel have been successfully used to synthesize BST films. The various techniques employed to fabricate BST films are designed to produce the films' specific microstructure and dielectric properties. In addition, it is also essential to obtain the lowest possible process temperature to comply with silicon technology and to minimize post-deposition thermal treatments under low oxygen partial pressures to maintain the resistance of the films. Meanwhile, maintaining precise microscopic control of the stoichiometry, large area deposition and achieving good step coverage, are also relevant tasks [33,41].

The deposition methods stated above are highly competitive. Each method has its own merits and limitations related to the deposition mechanics and film properties. For instance, the properties of rf-sputtered BST films can satisfy the requirements for use in a 256-Mbit DRAM capacitor. The rf-sputtering method using a multicomponent oxide target not only satisfies this requirement but is also an appropriate method to produce BST films. NEC, Mitsubishi and Samsung have made great studies in rf-magnetron sputtered $(Ba_{0.5}Sr_{0.5})TiO_3$ films to a practical stacked DRAM capacitor [42]. They sputter deposited thin BST films having an equivalent SiO_2 thickness of 8 Å over Pt/Ta electrodes, subsequently attaining an unit area capacitance of 40 fF μm^{-2} and leakage current of $<10^{-7}$ A cm^{-2}. They also observed the dependence of dielectric constant on film thickness, BST's dielectric constant decreased with reduced film thickness. The dielectric constant of the 70 nm thick film exceeds 300 and 200 nm thick film is more than 600, which are much larger than those of $SrTiO_3$. Mitsubishi deposited thin $(Ba_{0.75}Sr_{0.25})TiO_3$ films by an rf-sputter at substrate temperatures of 480–750°C [89]. The 30 nm thick films deposited at 660°C on Pt/SiO_2/Si substrate have a dielectric constant of 250 corresponding to an equivalent SiO_2 thickness of 0.47 nm, and a leakage current density ca. 1×10^{-8} A cm^{-2} which partially satisfy the requirements for use in a 256-Mbit DRAM capacitor. Samsung researchers have studied rf-magnetron sputtered $(Ba_{0.5}Sr_{0.5})TiO_3$ films with thickness of 15–50 nm at 640–660°C on 6 in. Pt/SiO_2/Si substrates and post-annealed at 550–850°C in O_2 or N_2 [52]. The 20 nm thick film with SiO_2 equivalent thickness of 0.24 nm possesses a leakage current of 4×10^{-8} A cm^{-2} and unit area capacitance of 145 fF μm^{-2} which is the highest storage capacitance reported to date for BST films. They also contended that the N_2 annealing of the BST thin film after the top electrode deposition is critical for obtaining a low leakage current because n-type BST film is required to form a high interfacial potential energy barrier. However, their dielectric constants are insufficiently large for application to a Gbit era DRAM with a planar type storage capacitor.

The pulsed laser deposition method have been successfully used to synthesize $(Ba_{0.5}Sr_{0.5})TiO_3$ thin films [79]. Though this method has the ability to grow crystalline films at low substrate temperature with a good control of stoichiometry, the reported leakage current density values are very high. The MOD technique provides advantages of reproducible coating thickness and compositions and low deposition cost. Fujii et al. [54], employed this technique to prepare BST films over Pt/Ti/Si substrate based on alcohol-based precursor liquid. They obtained the dependence of the lattice constant and the dielectric constant of the fabricated BST film on the Sr composition. These results present maximum dielectric constants for films close to the composition of $Ba_{0.7}Sr_{0.3}TiO_3$. They also employed this BST film which allows the planar-type single stack structure to be incorporated into the ULSI DRAM storage capacitor and achieve 1.3 nm equivalent SiO_2 thickness and 2×10^{-9} A cm^{-2} leakage current density at 3.3 V.

The advantages of CVD include a high deposition rate, uniform deposition over large areas and satisfactory step coverage [60]. However, the CVD of BST film is restricted by a low vapor pressure of source materials and deterioration during storage. Researchers at Mitsubishi Electric Corporation have developed an alternative way of precursor transportation. That is, suitable precursors are dissolved in organic liquids and the liquid is injected into a CVD reactor [84]. The liquid-source delivery methods have produced BST thin films on 6-in. Pt/SiO_2/Si substrates by using Ba $(DPM)_2$, $Sr(DPM)_2$ and $TiO(DPM)_2$ (DPM=dipivaloylmethanato, $C_{11}H_{19}O_2$) dissolved in tetrahydrofuran and achieved the reproducibility of ±3% for (Ba+Sr)/Ti, coverage of 72%, dielectric constant of 230, equivalent SiO_2 thickness of 7.8 Å, and leakage current density of 6.7×10^{-6} A cm^{-2} at 1.65 V.

Mitsubishi also constructed a DRAM cell with dimensions appropriate for 1-Gbit device on the basis of a Ru/BST/Ru stacked capacitor. The BST films, having an equivalent SiO_2 thickness of 0.5 nm and excellent step coverage, were deposited at 420°C by a two-step process of LSCVD. Moreover, NEC corporation employed ECR-CVD to develop a Gbit storage capacitors. The BST films having a thickness of 61 nm, were deposited on $Pt/TaO_x/Si$ substrates at 450°C and treated with RTA at 700°C for 1 min. These films had a dielectric constant of 220 and leakage current density of 3×10^{-7} A cm^{-2} at 1 V [90]. They also developed ECR-MOCVD BST-based stacked capacitor with $RuO_2/Ru/TiN/TiSi_x$ storage nodes for Gbit DRAM generations [91]. Sol–gel processing involves hydrolysis and condensation of organo-metallic precursors where the resulting sol is coated onto the substrates and dried to a solid film (gel). The resulting gel film is then decomposed and densified by heat treatment to produce a crystallized film. Tahan et al. [92] sol–gel deposited 400 nm thick $(Ba_{0.8}Sr_{0.2})TiO_3$ films on $Pt/Ti/SiO_2/Si$ substrates to obtain a dielectric constant of 400 and a leakage current density of 0.17 μA cm^{-2} at 3 V. Although the BST films with adequate dielectric properties can be deposited by using various techniques, on the basis of DRAM capacitor cell structures proposed by NEC, Mitsubishi, Samsung and US DRAM consortium, CVD BST films are required in the future Gbit era DRAM to increase the storage capacitance. Integration issues include selection and stability of electrode and barrier layer materials, step coverage of dielectric films, high temperature endurance and etching methods must be solved before high-permittivity film based DRAMs are commercialized.

Thus, the step coverage of BST films deposited using the CVD technique has attracted increasing attention for use in the side area of bottom electrodes in DRAM capacitors to increase the storage capacitance. NEC researchers have applied ECR plasma MOCVD BST films to a practical stacked Gbit DRAM capacitor. Applying this stacked capacitor technology can achieve a sufficient cell capacitance of 25 fF for 1-Gbit DRAMs in a capacitor area of 0.225 μm^2 with only 0.3 μm high storage nodes [88].

Comparison of the electrical properties of the BST films prepared using various deposition techniques are tabulated in Table 4. For the leakage current densities, an extremely large variation in results is found for capacitors using various electrodes, compositions and thickness of BST films. This table also includes values of the dielectric constant for $(Ba_{0.5}Sr_{0.5})TiO_3$ between 140 and 600. Different studies markedly vary with respect to the dielectric breakdown strength. Such a variation might be ascribed to intrinsic film properties (e.g. microstructure and stoichiometry) as well as electrode and interface properties [33,41].

According to previous investigation, oxygen vacancies in BST films play a prominent role in the leakage current [93]. In general, BST films sensitive to oxygen deficiencies are prepared or annealed in oxygen ambience to reduce the concentration of oxygen vacancies and to improve the dielectric properties of the films. As recently demonstrated, the dielectric properties depend on a gas ratio of $O_2/(Ar+O_2)$ (OMR) during rf-sputtered BST films [71]. In that investigation, the dielectric constant increased with an increase of OMR and reached a maximum value at 50% OMR (Fig. 3). The leakage current density, although decreasing with an increasing oxygen flow, had a minimum value at 40% OMR. The film deposited at 450°C and 50% OMR had a dielectric constant of 375 and leakage current density of 7.35×10^{-9} A cm^{-2} at an electric field of 100 kV cm^{-1} with a delay time of 30 s. The BST films can exhibit large dielectric constants due to polarization of electric dipoles. It has been reported that the dielectric constant of the films was influenced by oxygen stoichiometry, composition, grain size, grain boundary and crystallinity (dipole density, polarization). High oxygen incorporation in the films seems to play an important role in promoting the polarization of electric dipoles. A related study fabricated the Pt/BST/Pt capacitors using a sputtering technique and post-annealed under a N_2 or H_2 atmosphere indicating abnormally higher leakage current when the negative bias was applied to the top electrode [94]. In addition, the enhanced leakage currents were effectively reduced by annealing under an O_2 atmosphere. These results can be accounted for by compensating for the oxygen vacancy in the BST films by introducing oxygen through the top Pt electrodes with the grain boundaries of the columnar structure acting as a diffusion path for the oxygen.

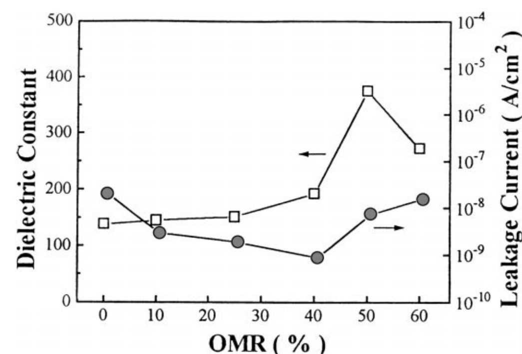

Fig. 3. Effect of OMR on the dielectric constant and leakage current of the $Ba_{0.5}Sr_{0.5}TiO_3$ films deposited at 450°C [71].

The properties of BST thin films prepared on (1 1 1) $Pt/Ti/SiO_2/Si$ and (1 0 0) Si substrates by pulsed laser ablation (PLA) were reported as a function of the target composition and the oxygen pressure [95]. Surface morphology of the films prepared at high oxygen pressure was rough compared with that of the films prepared at low oxygen pressure. Dielectric constant of those films was found to be lower than that of the films prepared at low oxygen pressure. The authors suggested that the excessively high oxygen pressure during the PLA deposition deteriorated the crystal structure and the dielectric property of the BST films depends on the composition of BST films.

BST thin films were deposited on $Pt/SiO_2/Si$ substrates with various O_2/Ar ratios by rf-sputtering and the

crystallinity, microstructure and electrical properties of the films were investigated by Lee et al. [96]. The deposition rate decreased with increasing of the O_2 content of the sputtering gas. It was believed that this resulted from the sputtering yield of O^{2-} being lower than that of Ar^+. Park et al. [97] examined how post-annealing affects the electrical properties of 20 nm thick sputtered BST films. According to their results, the dielectric constant increased without significantly increasing the leakage current by annealing at 750°C. Later, Horikawa et al. [85] developed post-annealing process for 30 nm thick CVD-deposited BST films. Their results indicated that direct annealing of BST capacitors roughened the surface morphology of the upper Pt electrodes of BST capacitors. However, the post-annealing of capacitors with a silicon dioxide passivation only slightly changed the surface morphology of Pt and BST, and also did not significantly deteriorate the leakage current.

The deposition temperature, a major parameter in the deposition process, determines the decomposition rate of the precursors and has a strong influence on the crystallinity and structure of the deposited films. Depositing good quality BST thin films requires a rather high process temperature owing to its high crystallization temperature. In addition to influencing the BST material, high temperature process also affects the interfaces with the electrodes, which critically controls the overall electrical properties of the capacitor, particularly when the BST film thickness is very small [52].

3.2. Film composition

Film composition pronouncedly affects the dielectric constant [80,85]. The film with a composition of $Ba_{0.5}Sr_{0.5}TiO_3$ has the highest dielectric constant at room temperature. Several researchers have conferred that a film has it's maximum dielectric constant at room temperature when the (Ba+Sr)/Ti ratio is 1:1. According to their results, the dielectric constant decreases when films are either titanium-rich or titanium poor [84]. It has been found that in $(Ba_xSr_{1-x})Ti_{1+y}O_{3+z}$, the factor y corresponding to the (Ba+Sr)/Ti ratio, strongly affects most film properties at a given x and deposition temperature [84,98,99] and is therefore one of the primary parameters used to control film performance. For example, BST films with x=0.7 have a maximum resistance degradation lifetime at approximately y=0.083, although the maximum value of the dielectric constant is found at y=0 [98]. Reasonable film behavior is generally achieved up to y=0.15, which greatly exceeds the solubility of excess Ti in bulk BST, of approximately $y \leq 0.001$. Given this large stoichiometry, a necessary step in understanding the composition dependence of film properties is to determine the locations within the microstructure at which the excess titanium is accommodated in BST thin films. Stemmer et al. [99] reported measurements of the microstructural accommodation of nonstoichiometry in BST thin films grown by liquid source chemical vapor deposition (LSCVD). Their observations indicate that partial accommodation of excess titanium in the grain interiors of polycrystalline BST films, either concurrent with or followed by accommodation at the grain boundaries. At extreme titanium excess, an amorphous phase, possibly TiO_x, was found between grains. The increased grain boundary area in these nanocrystalline films compared with that in much larger grained bulk ceramics, in combination with the nonequilibrated microstructure of the films due to lower processing temperature were said to be responsible for why Ti contents well beyond the bulk solid solubility limit are tolerated by their BST film structure.

It has been reported that the addition of dopants seriously influences the electrical properties of BST thin film capacitors [100,101]. The effects of Al and Nb doping on the leakage current behavior of $Ba_{0.5}Sr_{0.5}TiO_3$ thin films deposited by rf-magnetron sputtering were reported by In et al. [101]. Al and Nb were known to replace Ti-sites of the BST perovskite. BST thin films deposited at room temperature and annealed subsequently in air showed improved electrical properties. In particular, the leakage current density of the Al-doped BST thin film was measured to be around 10^{-8} A cm^{-2} at 125 kV cm^{-1}, which was much lower than those of the undoped or Nb-doped thin films.

Copel et al. [102] investigated the effects of Mn impurities on $Ba_{0.7}Sr_{0.3}TiO_3$ films using X-ray photo emission spectroscopy. The decrease in leakage current in the acceptor-doped films were attributed to the increased barrier to thermionic emission of electrons from Pt contacts into the dielectric. Doping in the films lowered the dielectric constant. This lowering effect is owing to the incorporation of aliovalent ions which hinders the crystallization of the films due to the requirement for higher solution energies to form compensating point defects [87]. In addition, the composition of surfaces/interfaces also largely determines the properties of the films and the characteristics of the devices based on the film. These results suggest that the segregation of acceptor or donor dopants at the grain boundaries in the film's interior heavily influences the barrier height, which could determine the leakage behavior in the BST thin films.

3.3. Crystalline structure

Crystalline BST films are usually obtained at relatively high substrate temperature. During the film growth, however, inter-layers and specific grain structures are developed which cause serious problems of low dielectric constant and the leakage current. An alternative approach is to grow amorphous BST films at low temperature and to crystallize them in a post-annealing process. Improvement of the dielectric constant and the leakage currents has been reported on post-annealed amorphous BST films. The crystallization of amorphous $Ba_xSr_{1-x}TiO_3$ thin film grown on single crystal MgO (0 0 1) substrate by rf-sputtering was studied by Noh et al. [103] in a synchrotron X-ray scattering experiment. Their study shows that a metastable intermediate phase that was nucleated at around 500–600°C at the interface plays a crucial role in the crystallization process. In a 550 Å thick

film, the crystallization to perovskite phase was occurred at around 700°C, while a 5500 Å thick film became crystalline at 550°C. The thickness dependence of the crystallization was attributed to the observed intermediate phase nucleated at near 600°C at the interface.

In thin films, high annealing temperature was required due to the energy barrier between the perovskite phase and the intermediate phase. In the thick films, the perovskite phase was nucleated directly from the amorphous phase in the bulk of the film concurrent to the nucleation of the intermediate phase at the interface. A transmission electron microscopy (TEM) study by Paek et al. [104] has also reported the observation of an intermediate phase near the interface.

X-ray diffraction patterns of as-grown BST films deposited at various substrate temperatures are shown in Fig. 4 [67]. Cubic perovskite structure of BST films was typically obtained under all conditions. As can be seen in Fig. 4, the crystal orientation and the crystallinity of the films are strongly dependent on the deposition temperature. Films deposited below 600°C have the cubic perovskite structure and show the polycrystalline state. The crystallinity of the films increases with increasing deposition temperature. Films deposited at 600 and 650°C have textured structures with [1 1 0] and [1 0 0] orientations, respectively. At 650°C, highly [1 0 0] oriented BST films were obtained. Many researchers reported that BST thin films in the polycrystalline state were obtained on the polycrystalline Pt electrode at a substrate temperature of ~500–650°C. However, the cause of the difference in crystal structures is not clearly understood yet. It is speculated that these are strongly associated with the crystallinity and the orientation of the Pt electrode. Furthermore, the change of the preferred orientation from the [1 1 0] to [1 0 0] direction above 600°C is considered to be related to the surface energy. In the perovskite structure, the (1 0 0) plane is a closely packed oxygen plane which has the lowest surface energy. Even if there is a large lattice mismatch, the [1 0 0] preferred orientation is strongly developed at high deposition temperatures. In general the films deposited on Si surface require sufficiently higher substrate temperature to form the crystalline phase than on Pt surface. These results reveal that the Pt surface can enhance the nucleation of the BST film more effectively than the Si surface [105]. BST films on Pt/Ti and Pt/Ta have higher dielectric constant than that of BST films directly on Si, $TiSi_2$, and $TaSi_2$.

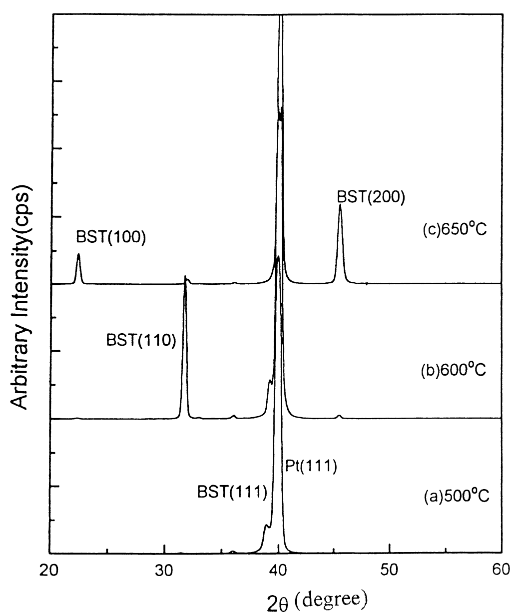

Fig. 4. XRD patterns of $Ba_{0.5}Sr_{0.5}TiO_3$ thin films deposited at various substrate temperatures [67].

3.4. Microstructure

The dielectric property of polycrystalline BST films is affected not only by the composition and crystalline structure of the phase present but also by the microstructure. The dielectric film in the next generation DRAM capacitor should have an equivalent SiO_2 thickness (t_{eq}) of <1 nm. When the BST film with dielectric constant of ca. 300 is applied for the DRAM, the actual film thickness must be <130 nm to obtain t_{eq} <1 nm. The grain size effect on the dielectric properties will be important for application to the DRAM capacitor because the BST film has such a small thickness [13]. Notable size effects of the dielectric constant, including thickness dependence and grain size dependence have been reported in BST films. Miyasaka and Matsubara [11] have reported that the highest value of dielectric constant exhibited by a polycrystalline $(Ba_{0.5}Sr_{0.5})TiO_3$ film with thickness of 500 nm was 900, while that of bulk ceramics is known to be >5000. They have also reported that thinner films of 80 nm thickness showed a smaller dielectric constant of ca. 400. Horikawa et al. [13] have investigated the correlation between the dielectric constant and broadness of an X-ray diffraction in $(Ba_{0.65}Sr_{0.35})TiO_3$ thin films. According to their result, the polycrystalline film with grain size of 45 nm had a dielectric constant smaller than 200, while the film with grain size of 220 nm showed a dielectric constant larger than 700 (Fig. 5). Horikawa et al. [13] studied the effect of grain size on the dielectric properties $(Ba_{0.65}Sr_{0.35})TiO_3$ films deposited at substrate temperatures of 500–700°C. The dielectric constant of these films ranges from 190 to 700 at room temperature. This value changes with the grain size rather than the film thickness. The effects of plasma bombardment on the initial growth of BST films and their properties were studied by Tsai et al. [106]. The films that were grown outside the plasma region exhibited better crystallinity, higher dielectric constants, higher electrical conductivity and rougher surfaces than those that were grown inside the plasma region. However, plasma bombardment did not affect the initial growth of the films on $Pt/SiO_2/Si$ or MgO substrates, as explored by atomic force microscopy (AFM). The films that were grown on $Pt/SiO_2/Si$ showed island growth characteristics, whereas those that were grown on MgO substrates revealed layer-by-layer growth characteristics.

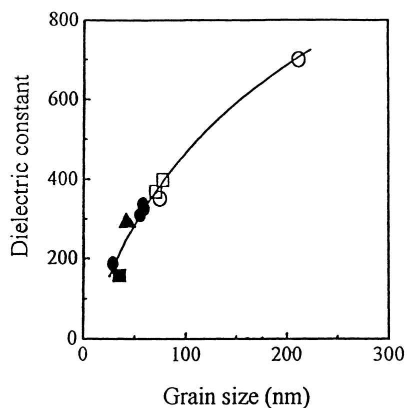

Fig. 5. The dependence of the dielectric constant on the grain size from XRD for the $Ba_{0.65}Sr_{0.35}TiO_3$ films deposited at the different substrate temperatures of 500–700°C. The substrate temperatures are 500°C (■), 550°C (●), 600°C (△), 650°C (▲) and 700°C (○) [13].

Kawahara et al. [107] observed that protrusions of BST crystallites appeared on BST film surfaces prepared by LSCVD (at 420°C). It was considered that these protrusions (consist of cubic BST perovskite phase) appeared because the BST films deposited in the first ~150 Å layer were not sufficiently crystallized, that is, the density of nuclei in that layer was small. As the ratio (Ba+Sr)/Ti increases, the density of protrusions increases with a rate of increase similar to that of the BST (1 1 0) peak intensity. The protrusions were successfully restrained by two-step deposition.

Mukhortov et al. [108] have reported heteroepitaxial growth of BST films on MgO (1 0 0) single crystals. Abe et al. [109] studied, $(Ba_{0.24}Sr_{0.76})TiO_3$ thin film epitaxially grown on a Pt/MgO (1 0 0) substrate, where the Pt film was also epitaxially grown on the MgO as a bottom electrode. The reason for choosing the Sr-rich composition was explained as due to the closeness of the lattice constant (a=3.93 Å) of BST to that of Pt (a=3.923 Å), was expected to bring about easy epitaxial growth on Pt. However, from the surface morphology observations using scanning electron microscopy (SEM) and reflected high energy electron diffraction (RHEED), they noticed 'stitch' like projections, which was assumed to have probably resulted from the lattice constant inequality between $(Ba_{0.24}Sr_{0.76})TiO_3$ and Pt. Recently, Yoon et al. [110] have successfully prepared BST thin films which were epitaxially grown on Pt/MgO and YBCO/MgO substrates by means of a laser ablation technique. The thickness of their BST film was ca. 200 nm. However, anomalous elongation of the lattice constant has not been reported.

Lee et al. [111] studied the microstructure dependence of the electrical properties of BST thin films deposited on $Pt/SiO_2/Si$ using cross-sectional TEM and diffraction analysis. Accordingly, BST film has a columnar structure which grows from Pt to BST surface. Also, the different layers were dense and smooth. Generally, when BST films grow with random orientation, diffraction patterns show rings. However, spot patterns were observed by Lee et al. for their BST films, which indicate that their film growth has [1 1 0] preferred orientation. Their grain size measurement by the line intercept method on the surface of the SEM micrograph demonstrated that as the film thickness increased, grain sizes increased slightly. It was observed that the dielectric constant increased from 348 to 758 when the grain size increased from 32 to 82 nm in the 600°C deposited BST films [65]. They suggested that the abrupt decrease of dielectric constant in the thin film (below 75 nm) was due to another factor in addition to that by a low dielectric layer which formed during the initial deposition stage. They speculated that it is strongly associated with the grain size of BST thin films

In the case of $(Ba_{0.75}Sr_{0.25})TiO_3$ and $(Ba_{0.5}Sr_{0.5})TiO_3$ films, film structure changed from granular to columnar with increase in substrate temperature and was columnar for the film deposited at 750°C [51]. Dielectric constant correlated closely with grain size in the direction parallel to film thickness for both films. The grain size in the direction perpendicular to film thickness increases with deposition temperature as does the grain size in the direction parallel to film thickness. Therefore, it is considered that the dielectric constant is greatly affected by film crystallinity, grain size and the ratio of Ba/Sr composition interactively.

The properties of interfaces between electrodes and BST depend not only upon the electrode material but also on the processing, such as deposition conditions and post-annealing. The existence of an interfacial layer between the BST film and the Pt bottom electrode was confirmed by HRTEM [104]. The interfacial layer appeared to have crystallinity different from both the BST thin film and the Pt bottom electrode which resulted in variation of the interfacial states between BST and Pt. As the thickness of the BST films decreased from 300 to 50 nm, the thickness of the interfacial layer increased from 9.5 to 11 nm. The dielectric constant of the interfacial layer calculated from its measured overall capacitance and thickness, confirmed by HRTEM, was ca. 30, This low-dielectric constant interfacial layer has been shown to affect the electrical degradation of BST thin films with decreasing thickness. The role of the interface becomes increasingly dominant in the overall electrical conduction process when the film thickness is typically $<$100 nm.

3.5. Surface morphology

The bottom electrode materials greatly affect the electrical characteristic of BST thin films through resultant formation of the surface morphologies. Increasing the OMR during the film deposition process increases the root-mean-square (rms) surface roughness of BST films [71]. The rms surface roughnesses are 1.67, 3.199, 4.179 and 3.782 nm for 0, 25, 50 and 60% OMR BST films, respectively and the rms value decreases for BST films deposited above 60% OMR. The diffusion energy of sputtered atoms is probably reduced when OMR increases and the lateral movement on the surface also may be reduced, because the sputtered atoms

Table 5
Properties of BST deposited on the various bottom electrodes [48][a]

Properties	Bottom electrodes				
	Pt	Ir	IrO_2/Ir	Ru	RuO_2/Ru
Dielectric constant	219 (503)	309 (593)	234 (501)	548 (325)	322 (433)
Leakage current (10^{-8} A cm^{-2}) @ 100 kV cm^{-1}	2.2 (2.5)	4.9 (2.1)	2.5 (3.3)	39.4 (2.1)	3.5 (2.4)
Tangent loss	0.014 (0.015)	0.046 (0.019)	0.016 (0.02)	0.32 (0.019)	0.017 (0.012)
Work function (eV)	5.6	5.35	–	4.8	–
Breakdown field (MV cm^{-1})	3.84	3.68	3.49	1.94	1.84
Fatigue endurance (cycling number)	$>10^{11}$	$>10^{11}$	$>10^{11}$	$>10^{11}$	$>10^{11}$
Surface roughness (nm)	1.9	1.27	2.25	4.40	4.12
H_2 damage endurance (dielectric constant variation)	−16%	−12%	−13%	−29%	−14%
Stability in O_2 ambient	Up to 700°C	Up to 700°C	Up to 700°C	Up to 500°C	Up to 700°C

[a] The values within parenthesis, 700°C; O_2 annealing for 20 min.

collision increase with oxygen atoms and mean free path may also be shorter. Therefore, the surface roughness of the films prepared at below 50% OMR would be expected to be increased. But above 50% OMR, O_2 re-sputtering rate may be stronger than Ar-sputtering rate and hence the surface roughness would decrease at 60% OMR. The film deposited at 450°C and 50% OMR exhibited good surface morphology and had dielectric constant of 375, tangent loss of 0.074 at 100 kHz, leakage current density of 7.35×10^{-9} A cm^{-2} at 100 kV cm^{-1} with a delay time of 30 s. Lee et al. [96] envisaged similar surface morphology studies for as-deposited and annealed BST films deposited in 0 and 50% OMR. Their observations indicate that the surface roughness of the as-deposited film decreased with increasing O_2/Ar ratio and the annealing resulted in a sharp increase in the roughness of the films. The dielectric constants of the film increased with increasing O_2 content, whereas the leakage current density decreased. From the AFM analysis, the authors verified that the leakage current characteristics of the BST films are strongly related to the surface roughness of the films.

Also, the rms value showed greater variation for BST films deposited at different bottom electrode materials [48,112]. Table 5 indicates that greater rms surface roughness of BST deposited on Ru and RuO_2/Ru compared to the Pt,Ir and IrO_2/Ir, which is attributed to the higher rms roughness Ru and RuO_2/Ru bottom electrode itself. If the as-grown film tends to be an amorphous layer with significant surface mobility of adatoms, the film usually has a smooth surface. The rms surface roughness may also be affected by the numbers of bottom stack-layers and it mostly increases with the increase in the numbers of stack layers. Tsai and Tseng [48] observed that BST films deposited on Pt, Ir and IrO_2/Ir with small grain size and smooth surface roughness showed higher breakdown field, whereas the BST on Ru or RuO_2/Ru with larger grain size and surface roughness exhibited lower breakdown fields.

3.6. Film thickness

The effect of film thickness on the microstructure and the associated property variation of BST thin film is discussed in earlier sections. The details on the role of film thickness on the BST film's electrical and dielectric parameters are briefly presented in the following. The thickness dependence of the dielectric constant of rf-sputtered BST films varies with the substrate temperature in connection with the grain size effect [65]. Film thickness has been established to impact primarily the zero bias permittivity through a thickness dependence of the first-order coefficient of the Landau–Ginzburg–Devonshire approach [113,114]. The dependence of inverse of the zero bias capacitance density of BST thin film to its thickness is often attributed to the presence of a constant-valued capacitance density, C_i/A, represented by the nonzero intercept, in series with the thickness-dependent capacitance density of the bulk of the film [113,114]. The constant capacitance is usually thought to represent some type of interfacial layer between the dielectric and one or both of the electrodes, and might arise from surface contamination of the BST, nucleation or reaction layers at the film/electrode interfaces, or changes in the defect chemistry at the dielectric–electrode interfaces. The apparent capacitance density at zero field may then be expressed as

$$\frac{A}{C_{\mathrm{app}}} = \frac{A}{C_{\mathrm{i}}} + \frac{A}{C_{\mathrm{B}}} = \frac{t_{\mathrm{i}}}{\varepsilon_{\mathrm{i}}\varepsilon_0} + \frac{(t - t_{\mathrm{i}})}{\varepsilon_{\mathrm{B}}\varepsilon_0} \quad (1)$$

where A is area, C_{app} the apparent capacitance, C_i the interfacial capacitance, C_B the bulk film capacitance, ε_B the film bulk permittivity, ε_i the interfacial layer permittivity, ε_0 the permittivity of the free space, t the total film thickness and t_i the interfacial layer thickness. Therefore, the nonlinear ferroelectric response is a long range cooperative phenomenon and the true permittivity may quite well change with film thickness.

Noh et al. [103] suggested that the observed thickness dependence of the crystallization in BST might be related to the film substrate interfacial behavior during crystallization. In thin films, the amorphous phase first transforms to the intermediate metastable phase. Since the energy barrier from the metastable phase to the perovskite phase is probably higher than that from the amorphous to the perovskite phase, the crystallization temperature in the thin film is

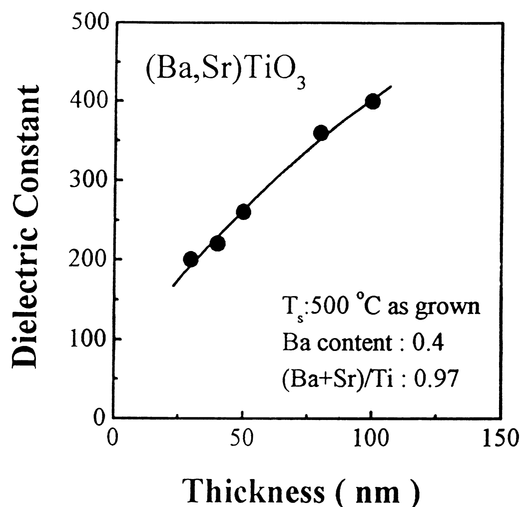

Fig. 6. Thickness dependence of the dielectric constant for $Ba_{0.4}Sr_{0.6}TiO_3$ films deposited on RuO_2 electrodes at 500°C by ECR-MOCVD [88].

higher. In thick films, the amorphous phase transforms directly to the perovskite phase at relatively low annealing temperature. The thickness dependence of dielectric constant for as-grown BST films deposited on RuO_2 at 500°C was studied by Yamamichi et al. [88]. Although the ϵ_r decreases with decreasing film thickness, the value larger than 400 was obtained for 100 nm BST without post-annealing (Fig. 6). This crystallization in the as-grown states is one of the most important advantages of ECR-MOCVD, resulting in the process step reduction for capacitor fabrication.

Film thickness dependences of the leakage current density at the applied voltage of 1.65 V and the SiO_2 equivalent thickness (t_{eq}) are shown in Fig. 7, as reported by Kuroiwa et al. [51]. The t_{eq} is given by $(\varepsilon_{SiO_2}/\varepsilon_{BST})\times t$, where t is the thickness of the BST film and ε_{SiO_2} and ε_{BST} are relative dielectric constants for SiO_2 and BST, respectively. The leakage current density increased considerably for the film of thickness <30 nm but no marked difference is found between the $(Ba_{0.5}Sr_{0.5})TiO_3$ and $(Ba_{0.75}Sr_{0.25})TiO_3$ films. It is regarded that leakage current depends on film thickness rather than the difference in the target compositions. The t_{eq} is 0.35 nm for 30 nm thick $(Ba_{0.5}Sr_{0.5})TiO_3$ film in comparison with 0.47 nm for 30 nm thick $(Ba_{0.75}Sr_{0.25})TiO_3$ film and the leakage current density is less than 1×10^{-7} A cm^{-2} in both films. Similar studies by Horikawa et al. [89] showed that the dielectric constant remains ca. 320, in the thickness range of 50–90 nm and the t_{eq} decreases linearly with film thickness. At thickness of <50 nm, the dielectric constant is no longer constant but goes down to 25 in the 30 nm thick film and the minimum t_{eq} value of 0.47 nm is obtained in this film.

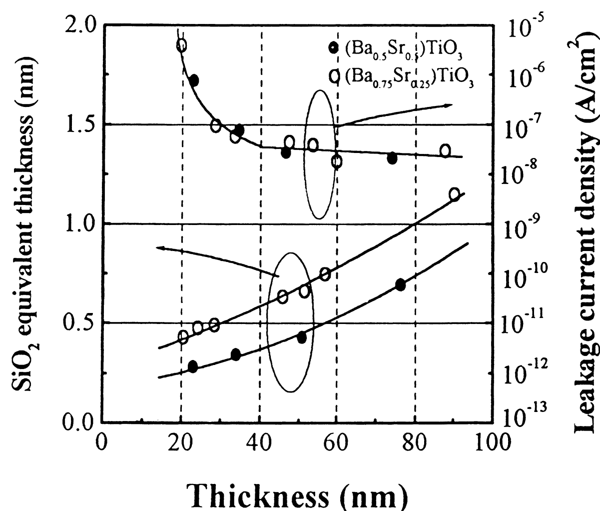

Fig. 7. Thickness dependences of leakage current density at an applied voltage of V and SiO_2 equivalent thickness. $Ba_{0.5}Sr_{0.5}TiO_3$ and $Ba_{0.75}Sr_{0.25}TiO_3$ films were deposited at the substrate temperature of 660°C [51].

Paek et al. [104] observed that the leakage current of BST increases exponentially with decreasing film thickness. A leakage current of 9.8×10^{-8} A cm^{-2} was obtained when their BST film thickness was 300 nm. However, this increased rapidly to 1.06×10^{-7} A cm^{-2} for the 50 nm thick BST film. The increased proportion of grain boundaries in 50 nm thick BST film was said to be the main cause of the abrupt increase in the leakage current. On the other hand, Hwang et al. [52] notified that oxide equivalent thickness does not decrease in proportion with the decreasing BST film thickness but more slowly due to the decreased dielectric constant of the film when they become thinner. Also they found that the dielectric constant of the BST thin film sandwiched between two Pt electrodes decreases as the thickness decreases because there exists a low dielectric constant layer which is a static space charge layer, at both interfaces with the electrodes due to the difference between the work function of Pt (5.5 eV) and electron affinity of the BST (ca. 1.7 eV). The abrupt decrease in dielectric constant of the thinner BST films (below 75 nm) is attributed to another factor in addition to that by a low dielectric layer which is formed during the initial deposition stages. Many authors speculate that it is strongly associated with the grain size of BST thin films [42,111].

3.7. Electrode materials

The metallic oxides of transition metals may present a very attractive metallization option in a variety of very large scale integrated (VLSI) applications [115]. Dioxides of Ru, Ir, Os, Rh, V, Cr, Re and Nb, have bulk metallic resistivities ranging from 30 to 100 μΩ cm, with IrO_2 being the best conductor in this group. There exist other transition metal oxides that merit attention such as ReO_3 has a resistivity of 10 μΩ cm, which is lower than that of the widely used $TiSi_2$. The heats of formation of transition metal oxides are comparable to that of transition metal nitrides [116] which emphasizes their normal stability. Ruthenium dioxide was reported to have low contact resistance on Ti metal [117]

comparable to pure ruthenium and gold. Chromium oxide, although fairly resistive has been used successfully as a diffusion barrier in the late seventies and recently, films of RuO_2 prepared by CVD were also reported to exhibit good diffusion barrier properties [118].

The electrode materials used in BST film capacitors can be classified into two general groups: the first group consists of noble metals, such as Pt, Ir and Ru [119–121], while the second group involves conducting oxides, such as RuO_2, IrO_2, $BaRuO_3$, $YBa_2Cu_3O_7$, $SrRuO_3$ and (La,Sr)CoO_3 [30,81,122,123]. The metal electrodes normally indicate a lower leakage current density than oxide electrodes, implying that the electrical conduction mechanisms are closely related to the BST/electrode interfaces. The greater leakage current appears in oxide electrodes to be related to the lack of a potential barrier at the BST/oxide electrode interface. High work function metals such as platinum ($\sim$5.6 eV) or iridium ($\sim$5.3 eV) films are primarily employed as the electrode material. Pt appears to be the material of choice for use as electrodes for BST capacitors, given its excellent electrical properties. However, in practical application of Pt bottom electrodes, there are still a few drawbacks, including the formation of hillocks at higher temperatures, amiability for oxygen diffusion, poor adhesion with Si and difficulty in patterning [53].

The dielectric constant and leakage current density of BST films deposited by rf-sputtering on the various bottom electrode materials (Pt, Ir, IrO_2/Ir, Ru and RuO_2/Ru) before and after annealing in O_2 and N_2 ambient were investigated by Tsai and Tseng [48,112]. Improvement in crystallinity of BST films deposited on various bottom electrodes was observed with annealing. The dielectric constant of BST thin films deposited on various bottom electrode materials also increases with increasing annealing temperature. The effect of bottom electrodes is summarized in Table 5. Based on the dielectric constant, leakage current and reliability, they suggested that the optimum electrode material for the bottom electrode with annealing was Ir and the Ru electrode was found unstable, because inter diffusion of Ru and Ti occurs at the interface between BST and Ru after annealing.

Conducting oxides, such as RuO_2 (rutile-type), are known to be easily etched in the fabrication of Gbit density DRAMs [124,125] and acts as a good diffusion barrier against oxygen. It has also been reported that oxide electrodes greatly mitigate fatigue problems which are encountered in ferroelectric memory capacitors. However, one serious issue related to the oxide electrode is its large leakage current. Lesaicherre et al. [125] reported a leakage current density of several $\mu A\,cm^{-2}$ at an applied voltage of 1.5 V from their ECR-MOCVD BST thin films which were deposited on a RuO_2 electrode. The large leakage current appears to be related to the absence of a potential barrier at the BST/RuO_2 interface. The phenomena of reduction and re-oxidation of ruthenium oxide during a BST deposition procedure appears to be the cause of the high leakage current and large property variation of BST thin films deposited on RuO_2 electrodes. Therefore, it is very important to set up the process condition to inhibit the reaction of $RuO_2 \Leftrightarrow Ru+O_2$, especially in the case of a high vacuum process, such as sputtering, PECVD and ECR-CVD [76].

$SrRuO_3$ is known to be a conductive oxide with a pseudocubic perovskite structure. It has metallic conduction with low resistivity ($\rho < 1\,m\Omega\,cm$), and has a pseudocubic lattice parameter of 0.393 nm which provides a suitable base for heteroepitaxial growth of BST films [126]. Abe et al. [30] and Jia et al. [127] have described the heteroepitaxial growth of a BST films on $SrRuO_3$/$LaAlO_3$ and $SrRuO_3$ electrodes, respectively, and verified good electrical properties. According to Abe et al. [128], their film deposited on the $SrRuO_3$ electrodes demonstrated a dielectric constant of 740 (t=42 nm) and a leakage current density $<10^{-8}\,A\,cm^{-2}$ (at 5 V). In addition, Hou et al. [129] made a $Ba_{0.5}Sr_{0.5}TiO_3$ (100–200 nm)/$SrRuO_3$/YSZ capacitor on an Si substrate using 90° off-axis sputtering. They used Au/Ti as the top electrode.

Pt-based structures with a Si diffusion barrier layers such as Pt/TiN and Pt/Ta are also used as storage electrodes because of their stability. However, difficulty in fine patterning of thick Pt will restrict its use for Gbit DRAM capacitors where the use of the side wall area of thick electrodes will be necessary to obtain a sufficient storage charge density [88,125]. The authors have proposed RuO_2/TiN storage nodes for a Gbit DRAM capacitor. A thick RuO_2 layer can easily be patterned into a 0.15 μm line-and-space structure by O_2–C_{l2} plasma [88,125]. In addition, the sputtered BST/RuO_2 interface was shown to be stable and no hillocks were observed on the RuO_2 surface after BST deposition at 650°C. Consequently, high dielectric BST thin film capacitors with low leakage current have been obtained [130].

Grill et al. [131] and Yoshikawa et al. [132] have reported structural changes occurring in RuO_2-based stacked structures on Si during annealing and film deposition. Even a slight degradation of the electrode/ barrier or barrier/contact/plug-interface affects the electrical properties of the capacitors used for high density DRAM application. The electrical properties of thick RuO_2/TiN-based storage electrode with poly-Si contact plugs for BST films have been studied by Takemura et al. [133]. Resistance of the storage electrodes including contact plugs can be evaluated from the dispersion observed in capacitance-frequency measurements. A Ru layer inserted at the RuO_2/TiN interface, a TiN/$TiSi_2$/Si junction and RTA annealing in N_2 ambient of the TiN layer are effective ways to reduce the resistance of RuO_2/TiN-based electrode. The barrier layer is required to prevent the electrode from being reacted with poly-Si plug. However, the oxidation of barrier during BST deposition and post-annealing imposes a serious problem on the integration because the barrier layer must remain conductive after the whole integration process.

Continued efforts on the etching of Pt recently generate a much improved storage node shape. An integrated BST capacitor for 256 Mbit, with Pt electrodes and TiSiN as

diffusion barrier, covered by SiO_2 spacers was recently fabricated by Samsung electronics [134]. Excellent diffusion barrier and oxidation resistant properties of TiSiN, further protected from being oxidized by the SiO_2 spacers, make post-annealing up to 650°C be possible. 72 fF per cell of capacitance and 1.0 fA per cell at ±1.0 V of leakage current density were obtained from a capacitor having projected area of 0.3×00.8 μm^2 (0.58 μm pitch) and 200 nm with 256 M density. The capacitance is correspondent to a value of 25 fF per cell of a DRAM with 0.30 μm pitch which is expected to be the cell size of 1-Gbit DRAM.

An appropriately placed oxidation resistant barrier and adhesion layers enhance the thermal and physical stability of the bottom electrode structure. Khamankar et al. [135] successfully demonstrated novel BST storage capacitor node technology using Pt electrodes for Gbit DRAMs. Promising results were obtained in separate Pt etch experiments using TiAlN as a hard mask. A 40 nm TiAlN hard mask was utilized to etch 300 nm Pt. The absence of thick photo resist during the Pt etch and the high Pt/hard-mask etch selectively led to the formation of fence free bottom electrodes with a high side-wall angle (∼70°). No elaborate post-etch clean up, regarded as a major issue with the Pt etch process was required. A capacitance of 17 fF per cell, with a leakage current density of 1.2×10^{-7} A cm^{-2} at 1 V was obtained for a capacitor array with 0.5 μm features for 100 nm Pt bottom electrode. The BST with 250 nm Pt thickness showed a capacitance of ∼33 fF per cell and tan δ∼0.009. These results demonstrate the promise of integrating Pt as an electrode material with BST as the capacitor dielectric for Gbit DRAMs.

4. Conduction mechanisms

The study of carrier transport in BST films is important both from the fundamental and the practical points of view. Although the conduction mechanisms in BST films have been studied very broadly, the subject is still controversial and very often confusing. More recently, several conduction mechanisms have been reported in literature to describe the nature of electrical conductivity in BST thin films and some controversies still exist regarding the major leakage mechanisms as suggested by different researchers depending on the electrode materials, processing conditions and the type of storage node structures used for the BST capacitors. Many experimental results show that thin dielectric films subjected to an external high electric field displayed a linear relationship in the $\log_{10}(I/V)$ vs. $V^{1/2}$ plots, where I is the current passing through the film and V the voltage applied across the film. This dependence is attributed to either the field-enhanced Schottky (SE) [136] or the Poole–Frenkel (PF) mechanism [136,137]. The former is a Schottky emission process across the interface between a semiconductor (metal) and an insulating film as a result of barrier lowering due to the applied field and the image force. The latter is associated with the field-enhanced thermal excitation of charge carriers from traps, sometimes called the 'internal Schottky effect'. These two transport mechanisms are very similar, except that in the PF mechanism the barrier lowering is twice as large as in the SE mechanism due to the fact that the positively charged trap in PF mechanism is immobile and the interaction between the electron and the charged trap is twice as large as the image force in the SE mechanism. This phenomenon leads to the doubling of the slope, which is given by $(q^3/\pi\varepsilon)^{1/2}$, in the $\log_{10}(I/V)$ vs. $V^{1/2}$ plot. q is the electronic charge and ϵ the dielectric constant of the film.

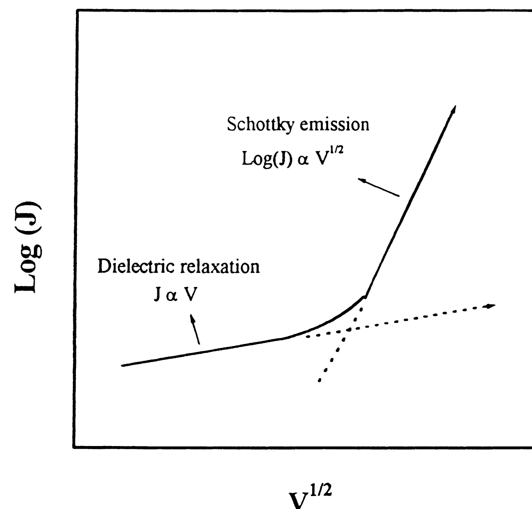

Fig. 8. Typical J–V behavior of $Ba_{0.5}Sr_{0.5}TiO_3$ capacitors [139].

Many papers have reported on the leakage properties of BST thin films with high work function metals such as Pt [14,21,28,97,138,139]. Fig. 8 shows a typical J–V behavior as reported by Fukuda et al. [139]. Two distinct regions are observed; in the low voltage region the current density is almost proportional to the applied voltage, while in the high voltage region it is proportional to the $V^{1/2}$. It has been accepted by some researchers that the former region is attributed to the dielectric relaxation and the later is to the Schottky emission from the cathode [14,21,28,97,138,139]. Fukuda et al. [140] also reported that post-annealing in oxygen ambient is very effective in reducing the currents due to both mechanisms. Since the diffusion coefficient is proportional to the oxygen vacancy density in the BST, the increase in the Pt/BST Schottky barrier height by post-annealing is thought to be caused by the decrease in the oxygen vacancy density at the Pt/BST interface. In other words, the Fermi level of the BST thin film may be pinned at the interface because of the oxygen vacancies in the film [139].

It is well known that oxygen vacancies in BST films play a prominent role in leakage current of films [71,93,141]. Tsai and Tseng [141] made an attempt to correlate the electrical leakage mechanism and possible concentration variation of oxygen vacancies in the BST films deposited

at various $O_2/(O_2+Ar)$ mixing ratios (OMR). The results indicated that the BST films prepared at low OMR (0–25%) exhibit the SE mechanism dominated below the transition electric field of 490 kV cm^{-1} and the PF transport mechanism dominated beyond 490 kV cm^{-1} and while those prepared at high OMR (40–60%) display SE mechanism dominated both below and above the transition electric field. The difference in dominant mechanism (bulk and electrode limited conduction) between the films was ascribed to the concentration variation of the oxygen vacancies in the films.

Leakage properties have been studied for BST thin films grown using LSCVD by Dietz et al. [114] and the following conclusions were drawn based on their findings. The leakage current through BST films was primarily limited by an interfacial Schottky barrier whose properties showed dependence on the electrode material and deposition conditions. They have used thermionic emission model to interprete the temperature and voltage dependence of BST electrical leakage data. Analysis in terms of a Schottky barrier limited current flow gives acceptable values for the cathode barrier height. A barrier lowering in addition to the Schottky effect was observed which was attributed due to a distribution of deep acceptor states in the bandgap of the ceramic.

The temperature-dependent current–voltage characteristics of fully processed $Ba_{0.7}Sr_{0.3}TiO_3$ thin film capacitors integrated in a charge-coupled device delay-line processor as bypass capacitors were studied by Shimada et al. [50]. The leakage current measured after completion of the integration process was 1–2 orders of magnitude higher than that measured after capacitor patterning. The leakage current at low voltages (<1 V, 50 kV cm^{-1})) indicated Ohmic conduction within a measured temperature range of 300–423 K. At high voltages (>10 V, 500 kV cm^{-1}), the SE mechanism plays a dominant role in leakage current, while the PF emission begins to contribute to the leakage current as the temperature is elevated.

Lee et al. [142] reported the electrical properties of BST film capacitor, focussing on the variation of the barrier height at interfaces with top and bottom electrodes and leakage conduction mechanisms according to different deposition power of top Pt electrode. The capacitors having a top Pt electrode with deposition power of 0.2 kW showed SE behavior at both top and bottom electrode interfaces with potential barrier heights 1.24–1.48 and 1.88–2.08 eV, respectively. The barrier height increased with post-annealing temperature and the capacitors having top Pt electrode with larger deposition power of 0.5 kW showed SE behavior only at bottom electrode interface with barrier of 1.61–1.89 eV. Under negative bias, a peculiar *J–V* behavior indicating a positive temperature coefficient of resistivity (PTCR) effect was observed at bottom electrode interface. This was attributed to the reduction of the interface potential barrier height between top Pt and BST which was caused by roughening of the top Pt during the post-annealing. Hwang et al. [52,122] also found that the Pt/BST/IrO_2 capacitor shows a PTCR effect when the Pt electrode was positively biased whereas the Schottky emission behavior was obtained when the Pt electrode was negatively biased even though the BST was paraelectric (The PTCR effect is known to be due to abrupt decrease in the dielectric constant of the ferroelectrics, such as $BaTiO_3$ at their Curie temperature) [143]. A model based on an upward band bending at the Pt/BST interface and downward band bending at the BST/IrO_2 interface was suggested to explain the asymmetrical electrical conduction behavior and the PTCR effect.

It has been reported that leakage currents increased asymmetrically for negative and positive bias voltage with increasing annealing temperature [124]. A model of leakage characteristics was proposed on the basis of SE mechanism. Using this model, Maruno et al. [124] predicted that at the Pt/BST interfaces there exist high density of oxygen vacancies, ca. 10^{20} cm^{-3}. These oxygen-deficient layers induce large built-in electric fields within BST. This electric field results in the enhanced leakage currents through reduction of Schottky barrier height due to image force increase and changes the *J–V* characteristics with increasing annealing temperature.

During fabrication of top electrode by the sputtering technique, some accelerated sputtering gases struck on the surface of the BST films. This results in out diffusion of oxygen from the BST films to the platinum top electrode. Oxygen vacancy generated by such a process ($O_0=V_0^{\cdot\cdot}+2e^-+1/2O_2$) may act as an electron trap site so it causes a high leakage current of Pt/BST/Pt capacitors. Joo et al. [94] have shown that when Pt/BST/Pt capacitors fabricated by a sputtering process are post-annealed under N_2 or H_2 atmosphere, higher leakage currents flow at negative bias region than at positive bias region, when bias voltage is applied to the top electrode. And the enhanced leakage currents are effectively reduced by annealing under O_2 atmosphere or adding oxygen into sputtering gas of platinum top electrode.

The presence of trap states (acceptors and donors) play a prominent role in the leakage current characteristics of BST capacitors. By employing a deep level transient spectroscopy (DLTS) technique, Wang et al. [93] investigated the deep trap levels of rf-sputtered $(Ba_{0.4}Sr_{0.6})TiO_3$ films deposited at various temperatures. A single trap was observed located at 0.45 eV in 450°C deposited films. Whereas two traps located at 0.2 and 0.40 eV appeared in 550°C deposited films.

Further, the *I–V* characteristics of the films at temperature range of 43–298 K reveal the presence of two conduction regions, indicating a Ohmic behavior at low voltage (<1 V) and SE or PF at high voltage (>6 V). The barrier height and trapped level estimated to be 0.46 and 0.51 eV from SE and PF mechanism, respectively, were in comparison to those obtained from the DLTS technique and hence they concluded that oxygen vacancy seems to be a more reasonable candidate for the source of the trap than cation vacancy. Moreover, the elementary nature of this trap is a prominent factor to affect the conducting properties of BST thin films.

5. Dielectric relaxation and defect analysis of BST thin films

The performance of capacitor in DRAM cell applications is affected by the charge storage capacity, dissipation of stored charge, dielectric response, and lifetime from the quality and reliability standpoints [144–147]. The capacitor in every DRAM cell must store sufficient charges for preserving memorized information although the cell area and the power supply voltage have been reduced due to the downsizing trend. Many efforts have been made to achieve sufficiently large capacitance in a small area. Furthermore, the reduction of leakage current is also important because it decreases the electric charge once stored.

In BST thin film capacitors, the capacitance has been observed to have dielectric dispersion, which result in dielectric relaxation [144,147]. The amount of charge stored on a capacitor during the write operation would therefore depend on the dielectric dispersion. It has been shown that dielectric relaxation phenomenon in thin film capacitors greatly affects its electrical properties [147]. Dielectric relaxation arises due to the dispersive nature of dielectric and increases with increasing value of the power law dependence of capacitance on frequency which is termed as the dispersion parameter. The most crucial influence of the dielectric relaxation on DRAM operation is that on the pause refresh property [25]. Horikawa et al. [28] estimated that charge loss by the dielectric relaxation for the pause time of 1 s would amount to ca. 8% of the initially stored charge, which is about two orders of magnitude larger than that by dc leakage current. There are at least four possible defects namely, the interface defect, grain boundary defect, shallow trap levels and oxygen vacancies, may often exist in the MIM capacitor films, lead to dielectric relaxation as a function of frequency [25,147].

Tsai and Tseng [147] investigated the dielectric relaxation and defect analysis of BST thin films through the measurement of dielectric dispersion as a function of frequency (100 Hz $\leq f \leq$ 10 MHz) and temperature (27°C $\leq T \leq$ 150°C). The capacitance at low frequency (<1 MHz), passes through a minimum. At high frequency (>1 MHz), the capacitance increases, goes through a maximum and decreases abruptly, passing through zero and attains negative values, i.e. the BST capacitor film showed a resonance in capacitance at high frequency between 1 and 10 MHz. Fig. 9 shows the complex capacitance plot of BST thin films measured at various temperatures. At high frequencies (1–10 MHz), resonance phenomenon emerges as a circle in the complex capacitance plane (C^*). The complex capacitance plot in the high frequency region continues to exhibit an abrupt discontinuity in dispersion with increasing frequency which indicates the onset of resonance phenomenon.

Figs. 10 and 11 show the complex impedance and admittance plane plots of BST deposited on Pt at various temperatures, respectively. On the basis of Z and Y analysis, Tsai and Tseng [147] proposed a practical equivalent circuit for BST capacitors as shown in Fig. 12. In the equivalent circuit, the R_{el} represents the electrode resistance, C_f the frequency dependent capacitance due to the grain and R_f the frequency dependent resistance due to grain boundary and interface. The above equivalent circuit for BST capacitor film agrees well with the one described by Jonscher [148].

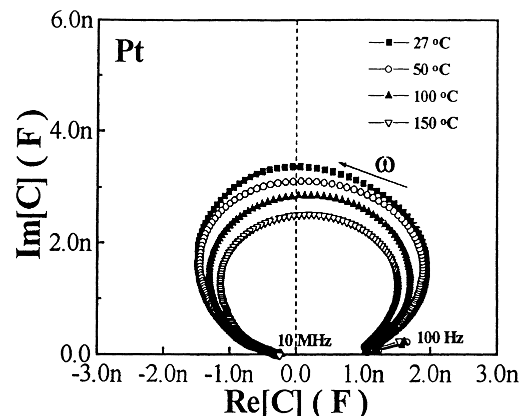

Fig. 9. Complex capacitance plot of $Ba_{0.47}Sr_{0.53}TiO_3$ films at various temperatures [147].

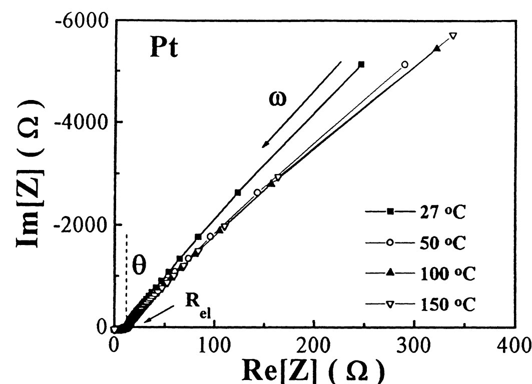

Fig. 10. Complex impedance plot of $Ba_{0.47}Sr_{0.53}TiO_3$ films at various temperatures.

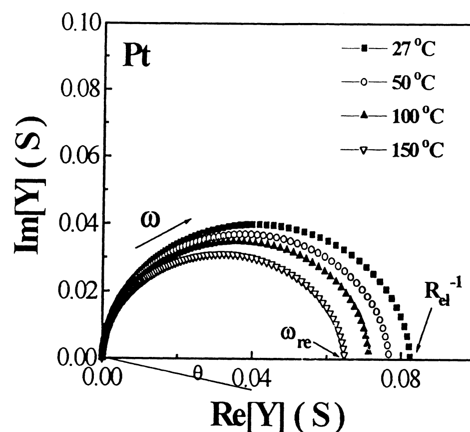

Fig. 11. Complex admittance plot of $Ba_{0.47}Sr_{0.53}TiO_3$ films at various temperatures.

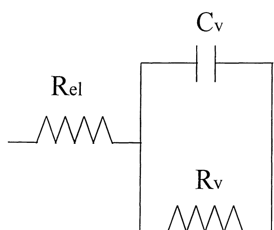

Fig. 12. The schematic equivalent circuit model for $Ba_{0.47}Sr_{0.53}TiO_3$ film capacitors for the frequency range 100 Hz to 1 MHz.

Further, through the measurement of admittance spectral studies in the temperature range of 27–150°C, they observed a shallow trap level located at 0.005–0.01 eV below the conduction band. Since the measured trap energy values are much smaller than the thermal energy (KT) 25.9 meV at 27°C, they concluded that the effect of shallow trap level can be neglected at the normal temperature range of DRAM operation: 0–70°C ambient and 0–100°C on chip (at the measurement frequency range <1 MHz) and the equivalent circuit has contribution only from grain, grain boundary and interface (BST/metal) defects. Yoon and Safari [149] have also observed resonance in capacitance at a frequency between 10 and 15 MHz for capacitance of 3–5 nF and explained that the resonance phenomena is the reason for the observed increase in the dielectric loss above 100 kHz. And the resonance phenomenon was attributed to electrical resonance occurred at 10 MHz and was related to the electrode area of the films (0.6 mm diameter).

The dielectric relaxation of $(Ba_{0.5}Sr_{0.5})TiO_3$ films deposited by the rf-sputtering method have been investigated by Horikawa et al. [28]. Their observations indicate that the dielectric constant decreased with frequency following the relationship of $d\varepsilon/d(\log_{10}f)\sim -0.01\varepsilon$ and the dielectric loss was almost constant at <1% in the measurement frequency range. The transient current response for a stepwise change of applied voltage was found to be inversely proportional to time in the time range of 1×10^{-4}–5×10^{2} s. Based on the quantitative correspondence between the ϵ dispersion and the transient response, the authors confirmed that the transient current is the absorption current due to dielectric relaxation. The absorption current for the thin films of BST is attributed not to a set of a several distinct dielectric relaxations but to a series of dielectric relaxations continuously distributed throughout the wide frequency range

Fukuda et al. [150] described the mechanism of the dielectric relaxation of BST capacitors post-annealed in oxygen ambient. From comparison of the electrical characteristics of the as-deposited and post-annealed BST film capacitors, it was concluded that electrons from oxygen vacancies in the interfacial depletion layer are the origin of the dielectric relaxation phenomenon. They also studied the temperature dependence of the dielectric relaxation current of the BST capacitor and found that its thermal activation energy is 0.3 eV. This relatively small activation energy suggests that the electron is most likely responsible for the observed dielectric relaxation. Furthermore, considering that an oxygen vacancy is an electron donor in perovskite oxide, the effect of post-annealing is assumed to compensate for such vacancies by the introduction of oxygen atoms.

The ionic and electronic conductivity characteristics and the diffusion of oxygen ion in the $(Ba_{0.47}Sr_{0.53})TiO_3$ thin films rf-sputtered at 450°C on Pt bottom electrode at various $O_2/(Ar+O_2)$ mixing ratios (OMR) were reported by Tsai and Tseng [151]. Capacitance versus frequency measurements were performed on BST films with varying thicknesses by Zafar et al. [146]. Their study shows that the interfacial capacitance is independent of frequency and increases with temperature. Also, the bulk dielectric constant is observed to have a power law dependence on frequency and decreases with increasing temperature. Based on the bulk and interfacial study the authors showed that the observed increase in the dispersion with BST film thickness is a volumetric effect and the measured increase in dispersion with temperature is attributed mainly to decreasing bulk dielectric constant with increasing temperature.

Dielectric dispersion in BST film capacitors is also influenced by the properties of the electrode–dielectric interface in addition to bulk of the film. Balu et al. [152] studied the dielectric dispersion in BST thin films of compositions $Ba_{0.5}Sr_{0.5}TiO_3$ and $Ba_{0.4}Sr_{0.6}TiO_3$ deposited on Ir bottom electrode using rf-sputtering. In the case of $Ba_{0.5}Sr_{0.5}TiO_3$ films an increase in dispersion with increasing thickness was observed while the $Ba_{0.4}Sr_{0.6}TiO_3$ films exhibit a decreasing dispersion with thickness. Their study showed that the dispersion in the case of $Ba_{0.5}Sr_{0.5}TiO_3$ film was bulk dominated while that of $Ba_{0.4}Sr_{0.6}TiO_3$ was interface controlled and the BST capacitors of each composition was modeled as a series of combination of an interfacial and a bulk capacitance. The authors also envisaged various multi-layered BST capacitors with combinations of the above compositions and different individual layer thicknesses and observed that the experimental data agrees with the model predictions for films with layer thicknesses >150 Å.

6. Reliability

Yield and reliability of thin dielectric films have been major reliability concerns throughout the history of MOS integrated circuit production. As devices are scaled down, dielectric films become thinner, but despite scaling of power supply voltage, the electric field applied to the dielectric during operation is increased. Due to the high field present in the dielectric mandated by the aggressive dielectric scaling and the presence of oxide defects, catastrophic failure of the dielectric has always been the predominant oxide reliability concern, thereby limiting scaling. The manufacturing economics and more stringent customer requirements demand higher yield and lower failure rates. The measurement methods commonly used in dielectric yield and reliability assessment are the following [153]:

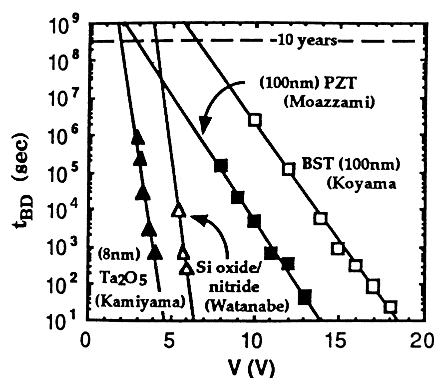

Fig. 13. TDDB for various DRAM dielectrics [164].

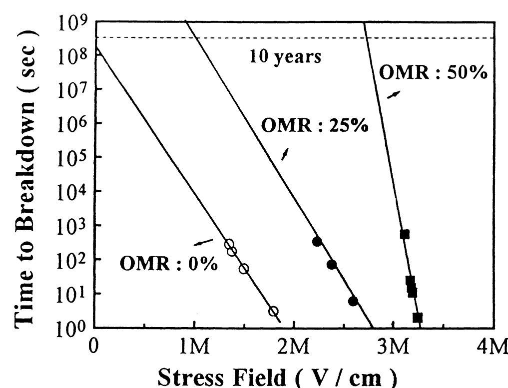

Fig. 14. Time to breakdown of the $Ba_{0.5}Sr_{0.5}TiO_3$ films deposited at 450°C at various OMR as a function of stress field [71].

1. Constant voltage stress (CVS): constant voltage stress is used to measure the time to breakdown (T_{BD}) at different stress fields.
2. Constant current stress (CCS): constant current stress is employed for the measurement of the charge to breakdown (Q_{BD}).
3. Ramped voltage stress (RVS): ramped voltage stress is used to measure breakdown fields (E_{BD}) and current–voltage (I–V) characteristics.
4. Exponentially ramped current stress (ERCS): this stress method is employed to obtain a fast measure of charge to breakdown (Q_{BD}), the breakdown strength (J_{BD} and E_{BD}) and the current–voltage (I–V) characteristics.
5. Combined ramped/constant stress measurements: these measurements are used to record extrinsic breakdowns and intrinsic times to breakdown with short measurement times and high resolution.

Fig. 13 shows the TDDB lifetime for various DRAM dielectrics. TDDB is also referred as resistance degradation of the dielectrics which shows a slow increase of leakage current under dc field stress. Degradation may takes place at a much lower electric field than the field of dielectric breakdown or thermal breakdown. Waser et al. [25] proposed an empirical power law between the electric field, E and the characteristic time constant t_{ch} (or lifetime), i.e., $t_{ch} \propto E^{1.1}$ to determine the resistance degradation of dielectric materials.

Electrical properties such as a low leakage current, fast dielectric response, low dielectric loss and long lifetime are essential for ensuring the reliability of BST film capacitors. The dielectric relaxation greatly affects the electrical properties of the BST capacitor, such as field-stress leakage current [150], stored-charge loss [28] and pause refresh properties [25]. TDDB and stress induced leakage current (SILC) have been investigated for the reliability of BST thin films [154]. The breakdown was strongly affected by leakage current properties, and did not depend upon the dielectric constant. Notably, the 10-year breakdown field for BST was six times larger than SiO_2.

Lifetime extrapolation using CVS–TDDB studies (Fig. 14) predicts the 10 year lifetime at a 1 V operating voltage [71]. It indicates that a 50% OMR sample has a longer lifetime than 25 and 0% OMR samples. The simplest way to improve the TDDB is to reduce the concentration of oxygen vacancies in the materials. In fact, a significant improvement is seen in the 50% OMR sample as compared to the 0% OMR sample (Fig. 14). Tsai and Tseng [48] reported that BST films deposited on Pt, Ir, Ir(600°C) and IrO_2/Ir samples have longer TDDB lifetime at 1 V operating voltage than BST on Ru and RuO_2/Ru (Fig. 15).

Extrapolated lifetimes of $(Ba_{0.7}Sr_{0.3})TiO_3$ (t_{oxeq}=6 Å) films were reported to be in a safe regime for ±1 V but not for ±2 V operation [155]. Therefore, the authors predict that further scaling of BST to t_{oxeq}=3 Å and below will not yield the required reliability. Time dependent leakage currents under high voltage stress (±5 V) to BST film at high temperatures (~225°C) were investigated by Yamabe et al. [156]. Their results indicate that under the application of negative stress, the leakage current increases once and decreases after reaching the maximum point, whereas the application of positive stress leads to steep increase of the leakage current after a given time. Three possible mechanisms were proposed to be responsible for the above

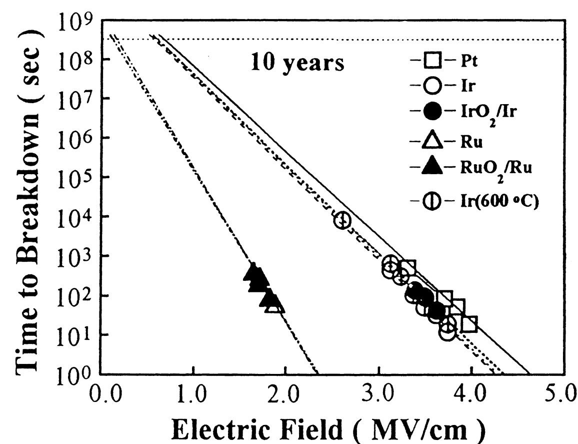

Fig. 15. Time to breakdown of the $Ba_{0.47}Sr_{0.53}TiO_3$ films deposited on various bottom electrodes as a function of stress field [48].

degradation processes. The first mechanism involves a combination of electron and hole trapping in the BST film. The second involves a combination of cation and anion distribution in the BST film. The third consists of a combination of the electron trapping and the cation distribution or that of the hole trapping and the anion distribution in the BST film. Numata et al. [31] suggested that a possible cause of the polarity dependence of the *I–V* characteristics of BST films is the intrinsic inhomogeneous distribution of the oxygen vacancies in the films. Accumulation of electrically drifted oxygen vacancies is thought to be the cause of the resistance degradation of BST: singular characteristic at the initial stage of the sputtering deposition or reaction between the deposited films and the bottom electrodes might cause greater concentration of oxygen vacancies near the bottom interface, leading to the polarity dependence of the resistance degradation. Shimada et al. [50] ascribed the time dependent increase in leakage current of BST films to the change in the conduction mechanism from the interface-controlled Schottky type to the bulk-related space-charge-limited type due to the accumulation of oxygen vacancies near the cathode as a result of interface barrier lowering and the migration of distributed oxygen vacancies across the film. For a 100 nm thick $(Ba_{0.5}Sr_{0.5})TiO_3$ film, the time required for 50% device failure, T_{50} was determined to be larger than 10^2 years under a stress voltage of 5 V [42]. Similar TDDB studies on BST films by Fujii et al. [54] and Ohno et al. [157] supports the observations of koyama et al. [42]. Park et al. [97] also reported the high reliability of BST thin films of thickness 20 nm.

The preceding discussion on the electrical reliability of BST thin films clearly demonstrates that the lifetime of BST has a quantitative relationship with voltage or current stress, film thickness and temperature of measurement and it only hints at the physical mechanism responsible for breakdown. During the course of electrical stress, dielectric damage manifest itself as generated interface and bulk traps, stress induced leakage current and finally catastrophic breakdown. Suitable deposition techniques and the associated post-annealing process need to be developed to minimize the charge trapping, thereby, reduce the interface instability and enhance the electrical reliability of BST film capacitors for Gbit era DRAMs.

7. Integration issues

There have been encouraging developments in the integration of BST-based ferroelectrics into high density DRAMs. One of the primary problems is the need to deposit the BST films under oxidizing conditions and to minimize post-deposition thermal treatments under low-oxygen partial pressures, as the perovskites are susceptible to reduction. This also limits the choice of electrodes for the capacitor stack to either Pt, Ru, or conducting oxides, since forming an insulating oxide at the BST–electrode interface will lower the stack capacitance. The electrode-material selection then results in a host of consequences for both processing and integration. NEC utilizes a stack consisting of polysilicon plug/thin Ti (forms Ti silicide)/TiN/RuO_2/BST/TiN/Al [81]. The RuO_2 is deposited under conditions that minimize oxidation of the TiN. During BST deposition, this RuO_2 also acts as an oxygen diffusion barrier. The approach appears viable if care is taken to ensure that deposition temperatures are kept as low as possible, which NEC achieves by the use of the oxygen ECR plasma-assisted CVD system.

Mitsubishi [158] utilizes a simpler scheme consisting of polysilicon/Ru/BST/Ru. It is believed that the Ru at the BST must partially oxidize, but the oxide has satisfactory conductivity. If the extent of oxidation is kept small, the large volume change associated with the oxidation is apparently not deleterious. The oxidation is minimized by the use of the low deposition temperatures and the use of a nitrogen atmosphere during the rapid thermal anneal used for the crystallization. However, the process temperature cause one to believe that ruthenium silicide formation should occur.

The US DRAM consortium, Samsung and earlier work by NEC [159] utilized a barrier system based upon Pt, for example polysilicon/Ti/TiN/Pt/BST/top electrode. Because oxygen diffusion rates along Pt grain boundaries are high, the Pt does not act as an oxygen diffusion barrier. The process conditions must therefore be selected to minimize the TiN oxidation as oxidation results in a rapid increase in the resistance.

It appears from recent publications that etching methods have been found for Ru and RuO_2 electrodes [81,158]. This is expected, due to known volatile Ru oxides and halides. Encouragingly, Mitsubishi has also reported an attractive X-ray-lithography procedure for Ru and has demonstrated its use for the processing of a very fine scale features [160]. However, there has been little evidence for a true reactive ion etch for Pt at room temperature. This presents a severe problem, for in the case of fine scale features with high aspect ratios, the Pt is redeposited on the side of the mask, forming unwanted features. One known solution to the Pt etch problem is to under take the reactive ion etch at elevated temperatures, which then requires compatible hard masks.

Recently, Kim et al. [161] reported that the critical issues of MIM BST capacitor for 0.15 μm can be solved by many novel processes such as recessed barrier with SiN spacer, Pt-encapsulated Ru storage node (modified etch mask structures and controlled etch mask sizes), MOCVD BST deposition and Al_2O_3 barrier layer to suppress hydrogen damage. A novel self-aligned electroplating process to fabricate Pt electrodes of integrated high-dielectric capacitors for 1-Gbit DRAMs and beyond was developed by Horii et al. [162], Samsung electronics. Pt pillars having 210 nm diameter and 650 nm height were fabricated after the SiO_2 wet strip. The leakage current density of sputtered BST capacitor using electroplated Pt was less than 2×10^{-7} A cm^{-2} at ±1.5 V. The t_{eq} and dissipation factor of 40 nm thick BST film were 0.70 nm and 0.0080 at 0 V, respectively. More

recently, Kiyotoshi et al. [163], Toshiba successfully developed a new in-situ multi-step (IMS) process technology to achieve both conformal step coverage and high dielectric constant of CVD-BST. IMS is a sequential repetition of low temperature CVD of BST and its crystallization in a batch type hot wall reactor that enables uniform deposition over 200 mm wafers. The authors demonstrated that using IMS CVD process combined with $SrRuO_3$ electrodes, a conformal growth of local epitaxial grown BST film with dielectric constant more than 300 and leakage current density around 10^{-7} A cm^{-2} at 1 V were easily attained.

8. Summary and future trends

This article has briefly reviewed how factors such as processing, film composition, microstructure, film thickness, electrode materials and interfacial properties affect BST thin film properties. The electrical properties of BST films prepared using various deposition techniques are also compared. The properties of BST films have been indicated to be strongly dependent upon the fabrication method, nature of the substrates and electrode materials and post-deposition annealing treatment. The recent work by Copel et al. [102] demonstrates that acceptor impurities can dramatically increase the depletion width in BST films and contribute to the reduction of leakage current. However, the physical origins of the doping effect on the films must be further elucidated and the possible decrease in dielectric constant caused by the doping must be solved as well. In addition, a new post-annealing technique is necessary to bring forth improvements in crystallinity and defect density reduction and thus improve the electrical properties of the films without significantly roughening the surface morphology of the upper electrode and BST films.

After satisfying the requirements for capacitance and leakage current, another relevant issue is the reliability, in the practical use of the BST films for memory cell capacitors. As commonly observed, leakage current gradually increases with a degradation of the insulation when applying temperature, ac and dc voltage stresses to BST capacitors for a certain time interval. The degradation process limits the lifetime and reliability of BST capacitors. Further understanding the defect formations and distribution, relaxation, conduction and breakdown of BST capacitors is required to enhance reliability. On the other hand, recent results indicate a high integration of BST films into the DRAM capacitor structure. However, relevant issues on how to improve the manufacturing processes and compatibility such as new etch processes and equipment for BST films and electrodes, lithography scale of $\sim$0.1 μm, low temperature processing and thermal stability of electrodes must be addressed as well. Attributed to the advancement of thin film technology and the principles of miniaturization/integration, BST thin films will remain as fertile field of research and development, full of application potential and rich in science.

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