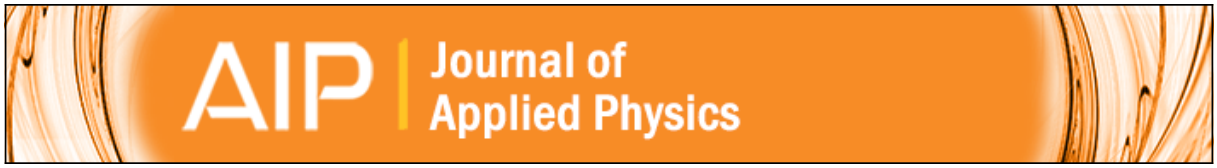


Study on Ge/Si ratio, silicidation, and strain relaxation of high temperature sputtered Co/Si 1x Ge x structures

Hsiang-Jen Huang, Kun-Ming Chen, Chun-Yen Chang, Tiao-Yuan Huang, Liang-Po Chen, and Guo-Wei Huang

Citation: Journal of Applied Physics **88**, 1831 (2000); doi: 10.1063/1.1305832
View online: http://dx.doi.org/10.1063/1.1305832
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/88/4?ver=pdfcov
Published by the AIP Publishing

Articles you may be interested in

Increased nucleation temperature of NiSi 2 in the reaction of Ni thin films with Si 1x Ge x
Appl. Phys. Lett. **81**, 1978 (2002); 10.1063/1.1498868

Characterization of strain in Si 1x Ge x films using multiple angle of incidence ellipsometry
Appl. Phys. Lett. **77**, 3529 (2000); 10.1063/1.1329165

Study of boron effects on the reaction of Co and Si 1x Ge x at various temperatures
J. Vac. Sci. Technol. A **18**, 1448 (2000); 10.1116/1.582368

Thermal stability of a Si/Si 1x Ge x quantum well studied by admittance spectroscopy
J. Appl. Phys. **87**, 1947 (2000); 10.1063/1.372118

High resolution electron microscopy study of molecular beam epitaxy grown CoSi 2 / Si 1x Ge x / Si(100) heterostructures
J. Appl. Phys. **85**, 2119 (1999); 10.1063/1.369512

Re-register for Table of Content Alerts

Create a profile.

Sign up today!

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 140.113.38.11 On: Thu, 01 May 2014 07:45:58

Study on Ge/Si ratio, silicidation, and strain relaxation of high temperature sputtered $Co/Si_{1-x}Ge_x$ structures

Hsiang-Jen Huang, Kun-Ming Chen, Chun-Yen Chang,[a] and Tiao-Yuan Huang
Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, Republic of China

Liang-Po Chen and Guo-Wei Huang
National Nano Device Laboratories, Hsinchu, Taiwan, Republic of China

(Received 25 October 1999; accepted for publication 12 May 2000)

As the transistors continue to scale down, the characteristics of high-temperature-sputtered $Co/Si_{1-x}Ge_x$ junction have received lots of attention because of its potential applications to heterojunction bipolar transistors. In this study, we have fabricated $Co/Si_{1-x}Ge_x$ junction using room-temperature and high-temperature (i.e., at 450 °C) sputtered Co on top of strained $Si_{0.86}Ge_{0.14}$ and $Si_{0.91}Ge_{0.09}$ layers prepared by ultrahigh vacuum chemical molecular epitaxy. The relative composition of Ge in Ge-rich $Si_{1-z}Ge_z$ precipitate and the solid solution of ternary phase silicide of Co–Si–Ge system were compared between room-temperature and high-temperature sputtered samples. We found that the high-temperature-sputtered samples are more effective in inhibiting lattice relaxation, which would be beneficial for manufacturing metal silicide/$Si_{1-x}Ge_x$ structure devices. Mechanisms were proposed to explain the large difference between the room-temperature and high-temperature sputtered samples. It is believed that the mixed Co–Si–Ge solution on high-temperature-sputtered samples is responsible for the different silicidation behaviors. © *2000 American Institute of Physics.* [S0021-8979(00)02616-5]

I. INTRODUCTION

Silicided strained $Si_{1-x}Ge_x$ junction has attracted lots of attention because of its potential applications to band-gap engineering by varying the Ge fraction in the $Si_{1-x}Ge_x$ layer. Some of its potential applications include serving as the base of heterojunction bipolar transistors[1–3] and the raised source/drain in deep submicron metal-oxide-semiconductor transistors. Concurrently, metal silicides have been widely employed in ultralarge scale integrated circuits as contacts and gate electrodes. Significant efforts have thus been made in understanding the phase formations and properties of metal/$Si_{1-x}Ge_x$ reactions.[4–12] Among the potential metal silicides, cobalt silicide is particularly attractive because of its low resistivity, cubic crystal structure, relatively small lattice mismatch with Si, and compatibility with self-aligned silicide (salicide) scheme. The cobalt silicide phases, i.e., Co_2Si, CoSi, and $CoSi_2$, are formed in sequence when a Co/Si bilayer structure is annealed.[13,14] However, as the linewidth of the transistor is scaled down into the deep subhalf-micron regime, it becomes very difficult to fabricate cobalt silicide film with low resistance due to agglomeration of $CoSi_2$ and the formation temperature increase of $CoSi_2$ phase. Significant efforts have been made to improve Co/Si silicidation, including using high temperature sputtering,[15,16] HF gas pretreatment,[17] and pre-amorphization implantation (BF_2, As, Si, N_2) onto the unreacted Co/Si layer.[18,19] These techniques have been shown to be effective in alleviating the linewidth effects and agglomeration of $CoSi_2$ films.

In the past few years, the reaction of a Co/strained $Si_{1-x}Ge_x$/Si system has been actively studied.[9,10,20,21] For the ternary phase diagram of the Co–Si–Ge system, a miscible ternary compound, $Co(Si_{1-y}Ge_y)$ ($y<0.67$), is observed after low-temperature furnace annealing with temperature ranging from 400 to 700 °C, which is based on cubic CoSi structure.[22] However, the crystal structures of $CoSi_2$ (i.e., cubic CaF_2 structure) and $CoGe_2$ (i.e., orthorhombic structure) are different, and the reaction between Co and Si is more favored than the Co–Ge one. As a result, only $CoSi_2$ phase is observed at higher annealing temperatures (~700 °C by furnace annealing). Concurrently, the surface accumulation of Ge in the form of Ge-rich $Si_{1-z}Ge_z$ precipitates is also observed.[12,23] However, despite the many literature reports in $Co/Si_{1-x}Ge_x$ layer reaction, the effects of high-temperature Co sputtering on $Si_{1-x}Ge_x$ layer and their relative reactions are still lacking.

In this article, we have studied the interfacial reaction of high-temperature-sputtered Co and strained $Si_{1-x}Ge_x$ layer with different Ge mole fractions. The phase formation at various rapid thermal annealing (RTA) temperatures and their structure characteristics were compared with the room-temperature-sputtered Co/strained $Si_{1-x}Ge_x$ layer. A systematic and simple model was proposed to explain the observed phenomena. These results would be helpful for $Si_{1-x}Ge_x$ devices.

II. EXPERIMENTS

Strained single-crystal $Si_{1-x}Ge_x$ thin films with $x=0.14$ and 0.09 were grown by an ultrahigh vacuum chemical molecular epitaxy (UHVCME) system.[24] The UHVCME

[a]Author to whom correspondence should be addressed; electronic mail: cyc@cc.nctu.edu.tw

 © 2000 American Institute of Physics

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 140.113.38.11 On: Thu, 01 May 2014 07:45:58

TABLE I. The $Si_{1-x}Ge_x$ growth condition and Co sputtering temperature for all $Co/Si_{1-x}Ge_x$ samples.

Sample	Ge fraction in $Si_{1-x}Ge_x$ layer	Si:Ge gas flow rate (sccm)	Substrate temp during Co sputtering (°C)
AH	0.09	1:1.5	450
BH	0.14	1:3	450
AR	0.09	1:1.5	200
BR	0.14	1:3	200

system included a loading chamber, a water-cooled stainless-steel growth chamber, separate nozzles for process gases, and a computer-controlled gas switching box. The growth chamber was pumped with a 1000 ℓ per second (l/s) turbo-molecular pump to a base pressure of 2×10^{-10} Torr. *N*-type 6 in. (100) silicon wafers with 10–15 Ω cm were used as the starting substrates. Wafers were first subjected to a pre-clean process with hydrogen passivation technique. After the pre-cleaning step, the wafers were loaded into the loading chamber. Then, they were immediately transferred to the growth chamber for epitaxial growth. A base pressure of 1×10^{-9} Torr was routinely obtained within 1 min after the wafer transfer process. Next, wafers were heated to the final deposition temperature of 550 °C at a ramp rate of ~150 °C/min. For growing $Si_{1-x}Ge_x$ layer, pure Si_2H_6 and GeH_4 were introduced into the growth chamber. The chamber pressure was maintained below 1×10^{-3} Torr during epitaxial growth by the turbo-molecular pump. The as-grown $Si_{1-x}Ge_x$ epitaxial layer thickness was 100 nm.

Wafers with grown $Si_{1-x}Ge_x$ layer were then cleaned by a standard clean procedure, and dipped in $HF:H_2O$(1:50) for 30 s to remove the native oxide. Co film was then deposited by ion beam sputtering at a base pressure of 5×10^{-9} Torr. The sputtering rate of Co film was 2 nm/s. The substrates were maintained at 450 °C during sputtering for the high-temperature-sputtered samples. While for the room-temperature-sputtered samples, no deliberate substrate heating was applied, and the substrate temperature was raised to approximately 200 °C. Detailed growth conditions and the abbreviations for the obtained samples were shown in Table I. Next, a 30-nm-thick TiN capping layer was deposited on top of the Co film to prevent Co oxidation during the silicidation process.[25,26] The $Co/Si_{1-x}Ge_x$ reaction was then performed in a RTA system equipped with high-intensity halogen tungsten lamps. The RTA treatment was carried out in a nitrogen ambient for 30 s with different RTA temperatures. The resultant average silicide film thicknesses were 430 Å for the 500 °C anneal, 510 Å for 700 °C, and 850 Å for 900 °C, respectively. After the silicidation process, TiN capping layer and the unreacted Co film were selectively removed by wet etching in $4H_2SO_4:1H_2O_2$ (30%) solution for 5 min. The sheet resistance was subsequently measured by a conventional four-point probe measurement system, while the phase structures of the reacted thin films were carefully examined by high-energy glancing-angle x-ray diffraction, high resolution x-ray diffraction and standard x-ray diffraction. Surface roughness was examined by scanning electron microscopy. Finally, the compositional properties were characterized by Auger electron spectroscopy (AES).

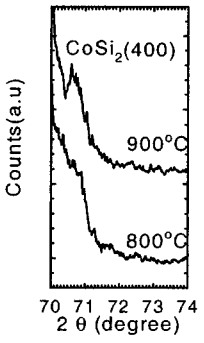
III. RESULTS AND DISCUSSIONS

A. Phase formation and its compositional change in silicide layer

The phase formation together with its crystal orientations after silicidation for both high-temperature and room-temperature sputtered Co samples on $Si_{0.86}Ge_{0.14}$ and $Si_{0.91}Ge_{0.09}$ layers were monitored by x-ray diffraction (XRD) in the θ-2θ geometry and glancing-angle x-ray measurements. The results are summarized in Table II. Only very weak patterns are observed in the standard XRD spectra for the BH sample (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) after annealing for 30 s at temperatures ranging from 500 to 700 °C. To further investigate the phase formation of the high-temperature sputtered samples, the glancing-angle x-ray system was employed. The results are shown in

TABLE II. Summary of silicide phase measured by standard XRD and high-energy glancing angle XRD systems at various temperatures for BR, BH, and AH samples.

	Sample		
RTA temp.	BR $Si_{0.86}Ge_{0.14}$ (200 °C)	BH $Si_{0.86}Ge_{0.14}$ (450 °C)	AH $Si_{0.91}Ge_{0.09}$ (450 °C)
500 °C	CoSi(210),(310) $CoGe_2$(204)	CoSi(110), (111), (200) (210), (211), (310)	The same as BH, except at 800 and 900 °C
600°C	CoSi(210),(310)	CoSi(110), (111), (200), (210), (211), (310)	
700 °C	CoSi(210)	CoSi(110), (111), (200), (210), (211)	
800 °C	$CoSi_2$(111),(200), (220),(400)	CoSi(210) $CoSi_2$(111), (220)	
900 °C	$CoSi_2$(200),(400)	$CoSi_2$(111), (220), weak(400); $CoGe_2$(204)	



[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 140.113.38.11 On: Thu, 01 May 2014 07:45:58

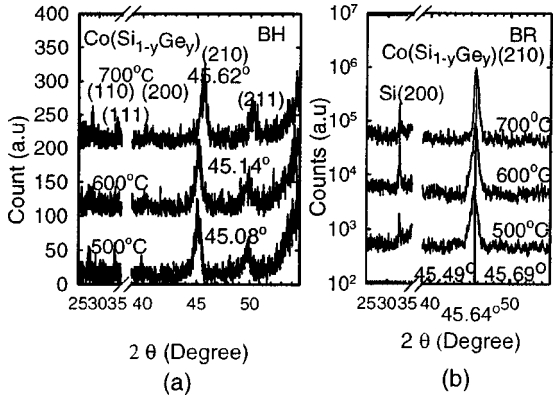


FIG. 1. XRD spectra of $Co(Si_{1-y}Ge_y)$ phase of (a) BH sample, and (b) BR sample after annealing at different temperatures for 30 s.

Fig. 1(a). The peaks corresponding to $Co(Si_{1-y}Ge_y)$ phases are very weak, albeit all possible cobalt monosilicide (CoSi) orientations are depicted. This is drastically different from the room-temperature-sputtered counterpart (i.e., BR sample for $Si_{0.86}Ge_{0.14}$ with 200 °C sputtering temperature). As shown in Fig. 1(b), the BR sample shows a strong peak corresponding to $Co(Si_{1-y}Ge_y)(210)$, whereas peaks representing some other orientations are missing altogether. We believe this drastic difference is due to the large intermixing layer of Co–Si–Ge caused by high-temperature sputtering of Co film on $Si_{1-x}Ge_x$ layer, leading to small but no orientation-preferred grains for the BH sample. In order to compare the relative composition of CoGe in $Co(Si_{1-y}Ge_y)$ phases, we have employed Vegard's equation[9,22] to calculate the phase shift of $Co(Si_{1-y}Ge_y)(210)$ in samples from 500–700 °C. As shown in Fig. 2, the relative ratio y decreases as RTA temperature increases. It can also be seen from Fig. 2 that for high-temperature-sputtered samples, a larger y is incorporated into the $Co(Si_{1-y}Ge_y)$ solid solution, compared to the room-temperature-sputtered counterparts. The composition y for both BH (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) and AH (i.e., $Si_{0.91}Ge_{0.09}$ with 450 °C sputtering temperature) samples is even higher than the initial composition x in the starting $Si_{1-x}Ge_x$ layer. This unexpected phenomenon implies that a large portion of Ge would be incorporated into the Co reaction during Co sputtering on heated substrate at 450 °C. For the RTA annealing temperature that is high enough to form CoSi (>500 °C), the CoSi phase is much preferred over the CoGe phase for its low heat formation.[27] However, for the RTA annealing temperature that is below the CoSi formation range (i.e., 450 °C), some Co–Ge compound (e.g., Co_5Ge_7,[28] CoGe) may be generated in the small grains in the Co–Si–Ge mixing region. This could explain the large fraction of CoGe found in the $Co(Si_{1-y}Ge_y)$ solid solution for AH and BH samples after 500–700 °C annealing.

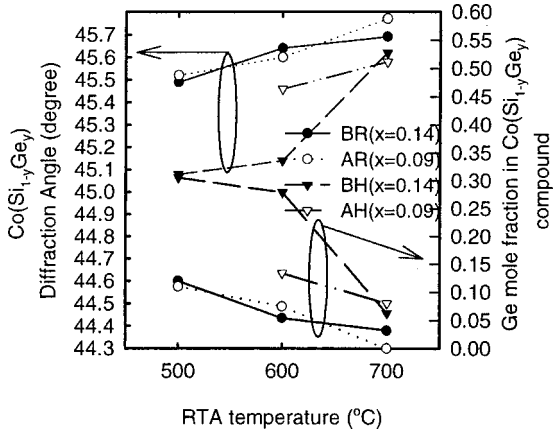


FIG. 2. The diffraction angle of $Co(Si_{1-y}Ge_y)$ phase and the relative Ge ratio y after annealing at various temperatures for 30 s.

For the samples annealed at 800 and 900 °C, $CoSi_2$ phase is formed and $CoSi_2(220)$ is the strongest phase in the BH (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) sample. According to the intensity of the $CoSi_2$ phase in XRD spectra, the silicide grains in high-temperature-sputtered samples grow larger for those annealed at 800 and 900 °C, compared to those annealed at 500–700 °C. However, from the BH sample shown in Table II, the CoSi(210) phase still exists at 800 °C, indicating that cobalt monosilicide has not been entirely converted into cobalt disilicide phase yet. This suggests that Ge atoms in the Co–Si–Ge mixing region may retard the formation of $CoSi_2$, even at 800 °C, and thus alter the thermal reaction behavior. On the other hand, the $CoSi_2(400)$ phase in the BH (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) sample is found to be very weak, while $CoSi_2(400)$ peak is extremely strong in both AR (i.e., $Si_{0.91}Ge_{0.09}$ with 200 °C sputtering temperature) and BR (i.e., $Si_{0.86}Ge_{0.14}$ with 200 °C sputtering temperature) samples. No $CoSi_2$ preferential orientation along the Si substrate is observed in the BH sample. However, for the samples with smaller Ge mole fraction in the $Si_{1-x}Ge_x$ layer (e.g., the AH sample), the orientation behavior of preferential $CoSi_2(400)$ phase shows up again as demonstrated in Table II. This may be because the $CoSi_2$ phase is grown along the Co–Si–Ge intermixing layer, not the Si substrate, for high-temperature-sputtered samples. This may also lead to the possible formation of $CoGe_2$, as is found in the BH (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) sample shown in Table II. With less Ge in the intermixing layer, the silicidation process behaves more like a Co film reacting on a pure Si substrate at 800 and 900 °C, so $CoSi_2$ grows along the (400) direction again.

Figure 3(a) shows the sheet resistance (ρ_s) of room-temperature and high-temperature sputtered samples at various RTA temperatures. From 500 to 700 °C, sheet resistance of the high-temperature-sputtered samples is higher than that of the room-temperature-sputtered counterparts. This can be explained by the formation of smaller but orientation-free $Co(Si_{1-y}Ge_y)$ grains in high-temperature-sputtered samples, or the formation of possible Co oxide as detected by AES during the Co sputtering process. For the high-temperature-sputtered samples with higher Ge content, the sheet resistance value is higher than that with the lower Ge content. At 800 °C, $CoSi_2$ phase is formed and the sheet resistances of all samples fall to a minimum with the exception of the BH (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) sample. This is due to the presence of the high-resistivity $Co(Si_{1-y}Ge_y)$ phase in the BH sample, which is consistent with the XRD

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 140.113.38.11 On: Thu, 01 May 2014 07:45:58

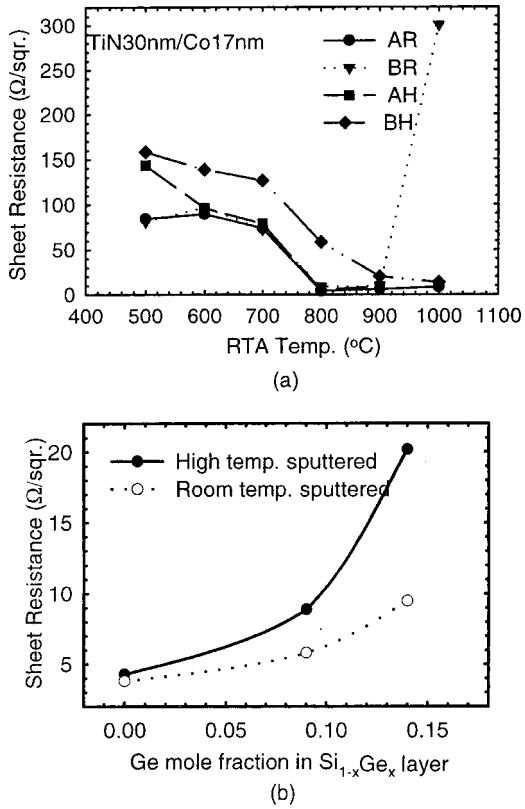


FIG. 3. Sheet resistance (a) as a function of RTA temperature for all samples, and (b) as a function of Ge mole fraction for both high-temperature and room-temperature-sputtered samples after annealing at 900 °C for 30 s.

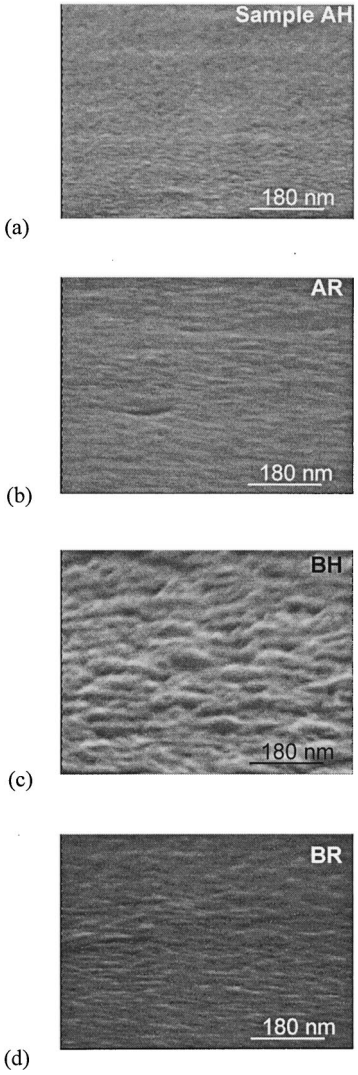


FIG. 4. Scanning electron microscopy (SEM) micrographs of the surface morphology of the (a) high-temperature-sputtered (AH), (b) room-temperature-sputtered (AR) $Si_{0.91}Ge_{0.09}$ sample and (c) high-temperature-sputtered (BH), (d) room-temperature-sputtered (BR) $Si_{0.84}Ge_{0.16}$ sample after being annealed at 900 °C for 30 s.

spectra shown in Table II. We can therefore conclude that the $CoSi_2$ silicide reaction is retarded with the presence of many Ge atoms incorporated into the Co–Si–Ge mixed region during high-temperature sputtering of Co on $Si_{0.86}Ge_{0.14}$ layer. The silicidation reaction mechanism in high-temperature-sputtered samples is based on the mixed Co–Si–Ge region, which is different from the room-temperature-sputtered samples. For the room-temperature-sputtered samples, either no mixed region occurs or the mixed region is simply not wide enough, so the reaction takes place along the $Si_{1-x}Ge_x$ substrate. At 900 °C, all the samples are converted into $CoSi_2$ phase so the sheet resistance value reaches its lowest value. Figure 3(b) shows the sheet resistance ρ_s as a function of Ge mole fraction after annealing at 900 °C by RTA. Generally, due to the large amount of precipitates for higher Ge mole fraction x in the $Co/Si_{1-x}Ge_x$ reaction samples, ρ_s increases as x increases. However, the ρ_s value of the high-temperature-sputtered samples is higher than that of room-temperature-sputtered counterparts. One reason may be the smaller $CoSi_2$ grains for AH (i.e., $Si_{0.91}Ge_{0.09}$ with 450 °C sputtering temperature) and BH (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) samples, which may also reduce the probability of agglomeration at 1000 °C, as shown in Fig. 3(a). So while the BR (i.e., $Si_{0.86}Ge_{0.14}$ with 200 °C sputtering temperature) sample exhibits an extremely high resistance due to agglomeration, the BH (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) sample does not suffer from the same high sheet resistance. Another plausible reason may be the high-resistivity $CoGe_2$ formation[12] in high-temperature-sputtered samples at 900 °C, as was detected by XRD measurements.

According to the scanning electron micrograph, shown in Fig. 4, for the $Co/Si_{0.91}Ge_{0.09}$ sample after annealing at 900 °C for 30 s the grain size of high temperature sputtered (i.e., AH) sample is indeed smaller than the room temperature sputtered (AR) one. This result is consistent with our explanation of higher sheet resistivity in the high-temperature-sputtered sample. As the Ge content increased, the surface became rough in both high-temperature and room-temperature-sputtered samples. However, as for the $Si_{0.86}Ge_{0.14}$ sample, the surface roughness for the high-temperature-sputtered (BH) sample became much poorer than the sample (BR) with room-temperature-sputtered Co film after 30 s annealing at 900 °C. We believe that the rough surface is due to more Ge (0.142 vs 0.130 in Table III) atoms absorbed into the silicide region and mixed compound ($CoGe_2$,$CoSi_2$) formation. In addition, the worst roughness may be the reason that the BH sample (450 °C sputtered

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 140.113.38.11 On: Thu, 01 May 2014 07:45:58

TABLE III. Generalized results detected by AES depth profiles for BR and BH samples after annealing at 500, 700°C and 900 °C.

AES result Sample		x in unreacted $Si_{1-x}Ge_x$ layer		Oxygen pileup	Surface Ge accumulation	Relative Ge fraction in $CoSi_2$ layer 900 °C
Br	500 °C	0.14	$\Delta x=$	No	No	···
	700 °C	0.121	0.019		Yes	···
	900 °C	···			···	0.130
	500 °C	0.14	$\Delta x=$	Silicide	No	···
BH	700 °C	0.136	0.004	$Si_{1-x}Ge_x$	No	···
	900 °C	···		Interface	···	0.142

$Si_{0.86}Ge_{0.14}$ film) kept the highest sheet resistance value at 900 °C. For improving surface roughness of the silicide film, a pre-amorphization implant should be adopted.

B. Change in Ge mole fraction for Ge-rich $Si_{1-z}Ge_z$ precipitate

After high-temperature annealing, possible formation of Ge-rich $Si_{1-z}Ge_z$ precipitates would distribute along the silicide grain boundaries.[29] Figure 5 shows the θ-2θ XRD profiles of $Si_{1-z}Ge_z(400)$ precipitate for BR (i.e., $Si_{0.86}Ge_{0.14}$ with 200 °C sputtering temperature) and BH (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) samples annealed at 700 and 800 °C. It can be seen that as the RTA temperature increases, the diffraction angle of the $Si_{1-z}Ge_z$ value increases. Figure 6 summarizes the diffraction angle and relative Ge composition in the Ge-rich $Si_{1-z}Ge_z$ precipitates for all samples. All precipitates should be relaxed $Si_{1-z}Ge_z$ crystal grains. At 700 °C, the calculated relative Ge ratios for the room-temperature-sputtered samples are higher than those of the high-temperature-sputtered counterparts. This is because there is no Ge accumulation in the silicidation layer for the high-temperature-sputtered samples after annealing by RTA at 700 °C, which should be revealed in AES profiles. When the RTA temperature increases to 800 °C, the entire $Si_{1-x}Ge_x$ layer is totally consumed, and the silicide layer turns into the $CoSi_2$ phase simultaneously. More and more Si and Ge segregate out and form more precipitates. From AES measurements, both the total amount of Si in the silicide region and the Si composition in $Si_{1-z}Ge_z$ precipitates increase. Thus the Ge mole fraction decreases as RTA temperature increases. At 800 and 900 °C, the value of the Ge fraction in the precipitates is nearly the same for both high-temperature and room-temperature sputtered samples.

C. Strain relaxation analysis for the underlying $Si_{1-x}Ge_x$ layer after silicidation

The high resolution asymmetric θ-2θ x-ray diffraction measurement system consisted of a Huber Cu target source with a Si(111) crystal monochromator and a Ragaku scintillation NaI detector to detect the diffracted beams. The sample was mounted in air at the center of the five-circle diffractometer axes.[30] The results of the high resolution XRD spectra of the unreacted $Si_{1-x}Ge_x$ layer for BH (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) and BR (i.e., $Si_{0.86}Ge_{0.14}$ with 200 °C sputtering temperature) samples are shown in Fig. 7. The $Si_{1-x}Ge_x$ peaks shift more toward the Si peak at higher annealing temperature, indicating more strain relaxation in the $Si_{1-x}Ge_x$ layer. Here we assume that the strain relaxation of as-deposited $Si_{1-x}Ge_x$ layer is zero. The strain relaxation of the SiGe layer after annealing can be calculated from the position of SiGe XRD peak. Figure 8 summarizes the calculated strain relaxation for BH and BR samples. The strain relaxation for the BR sample is actually more serious than that of the BH sample, indicating that the high-temperature-sputtering technique can inhibit the degree of lattice strain relaxation during the silicidation process.

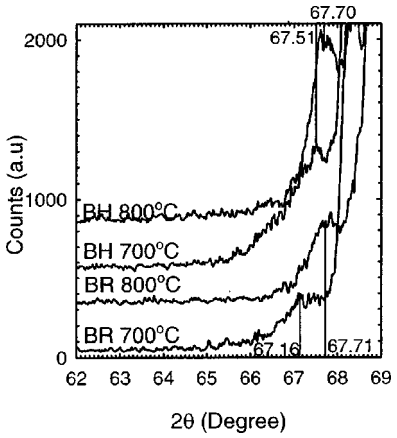


FIG. 5. XRD spectra of Ge-rich $Si_{1-z}Ge_z(400)$ precipitates for BR and BH samples after RTA annealing at 700 and 800 °C.

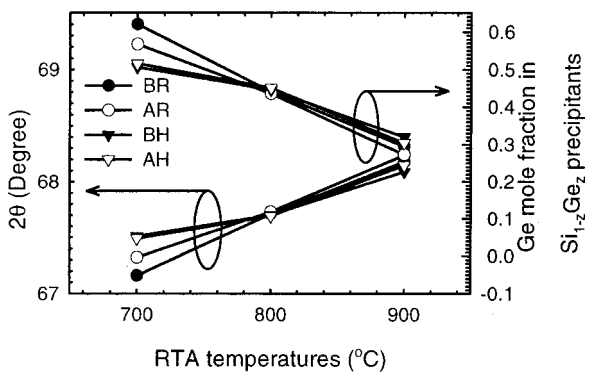


FIG. 6. The diffraction angle and calculated Ge mole fraction z in $Si_{1-z}Ge_z$ precipitates as a function of RTA temperature for all samples.

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 140.113.38.11 On: Thu, 01 May 2014 07:45:58

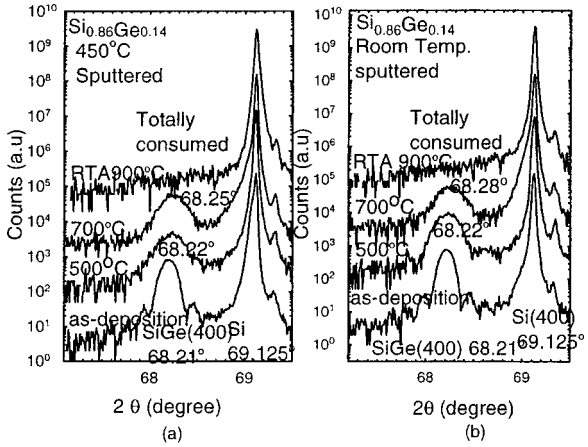


FIG. 7. High resolution XRD spectra of $Si_{1-x}Ge_x(400)$ phase for the underlying $Si_{1-x}Ge_x$ layer after annealing at different temperatures.

D. Redistribution of Si, Ge, O, and Co in the $Co/Si_{1-x}Ge_x$ layer after annealing

The compositional properties analyzed by AES measurements are summarized in Table III. A large oxygen pileup is observed in the BH (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) sample between the silicided and the unreacted $Si_{0.86}Ge_{0.14}$ layer after annealing at 500 and 700 °C. Figure 9 shows the AES profiles for BR (i.e., $Si_{0.86}Ge_{0.14}$ with 200 °C sputtering temperature) and BH samples after annealing at 700 °C. It can be seen that, contrary to the BH sample, no oxygen pileup is found in the BR sample. This may be due to the possible reaction between O and Co[31] during Co sputtering on the hot substrate. In addition, the increase of ρ_s (Fig. 3) in BH and AH (i.e., $Si_{0.91}Ge_{0.09}$ with 450 °C sputtering temperature) samples could possible be due to the formation of Co oxide. Generally, from 500 to 700 °C, the Ge fraction in the underlying $Si_{1-x}Ge_x$ layer is reduced during silicidation.[32] However, the reduction for the BH sample ($x=0.004$) is extremely small, compared to that for the BR sample ($x=0.019$). This implied that the underlying $Si_{1-x}Ge_x$ junction remains intact even after 700 °C annealing for the high-temperature-sputtered samples. At 900 °C, oxygen out-diffuses and the oxygen content decreases in the silicide reaction region for the BH sample. On the other hand,

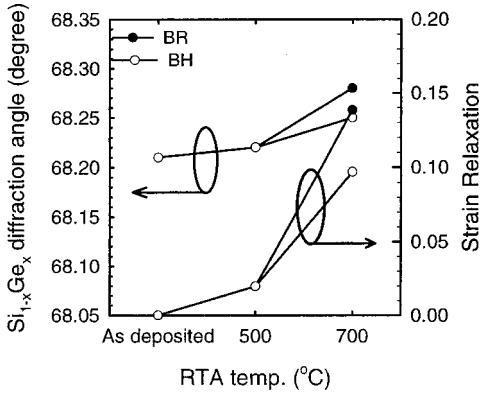


FIG. 8. The $2\theta Si_{1-x}Ge_x(400)$ phase shift and strain relaxation for the unreacted $Si_{1-x}Ge_x$ layer as a function of RTA temperature.

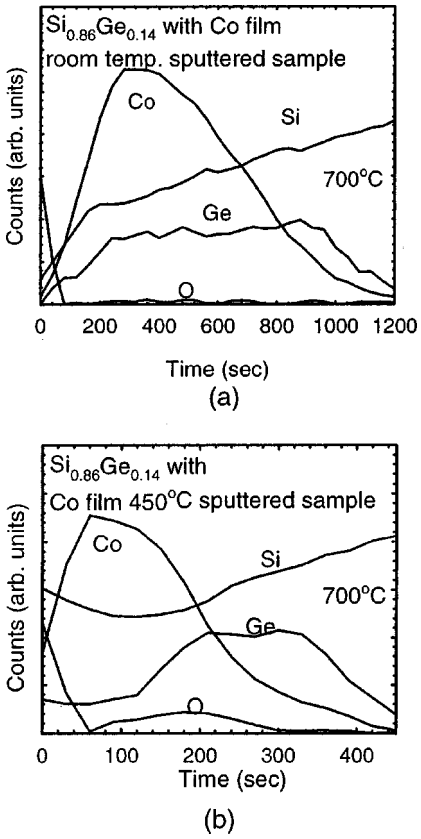


FIG. 9. AES depth profiles of (a) BR and (b) BH sample after annealing at 700 °C for 30 s.

although only 0.06 mole fraction of Ge is incorporated into the $Co(Si_{1-y}Ge_y)$ reaction, the phenomenon of accumulation or nonuniform distribution of Ge found in the BR sample is not found for the BH sample. We therefore conclude that the Ge segregation in high-temperature-sputtered samples is not as significant as in the room-temperature-sputtered counterparts. The Ge-rich $Si_{1-z}Ge_z$ precipitate may be small and uniformly distributed in high-temperature-sputtered samples. This result is consistent with the precipitate analysis shown in Fig. 6. At 900 °C, the out-diffusion of Ge toward the surface region is more apparent in the BH sample, due probably to the formation of $CoGe_2$. As a result, the Ge fraction in the $CoSi_2$ layer for the BH sample becomes higher than that for the BR sample.

IV. CONCLUSION

The characteristics of high-temperature-sputtered $Co/Si_{1-x}Ge_x$ junctions are reported. The resultant silicide films demonstrate a smaller but orientation-free $Co(Si_{1-y}Ge_y)$ grains when subjected to a low-temperature RTA anneal. Ge atoms are found to be incorporated significantly into $Co(Si_{1-y}Ge_y)$ after annealing at 500–600 °C. Retardation of $CoSi_2$ phase by Ge is detected after annealing by RTA at 800 °C, indicating that the mixed Co–Si–Ge region formed at 450 °C during Co sputtering plays an important role for the later silicide reaction. This phenomenon also affects the BH (i.e., $Si_{0.86}Ge_{0.14}$ with 450 °C sputtering temperature) samples annealed at 800 and 900 °C to form $CoSi_2$

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 140.113.38.11 On: Thu, 01 May 2014 07:45:58

with no preferred substrate orientation. This behavior is different from that of the conventional samples with room-temperature-sputtered Co film. Oxygen pileup is found between silicide and $Si_{1-x}Ge_x$ layer due to the possible oxidation of Co during sputtering, which may in turn increase the sheet resistance of high-temperature-sputtered samples. As the RTA temperature increases from 700 to 900 °C, small Ge-rich $Si_{1-z}Ge_z$ grains may precipitate and the Ge fraction decreases gradually. A smaller fraction of Ge is found in the $Si_{1-z}Ge_z$ precipitate at 700 °C on high-temperature-sputtered samples, compared to that of room-temperature-sputtered counterparts. Moreover, from high resolution XRD profiles, the high-temperature-sputtered samples could more effectively inhibit lattice relaxation as compared with room-temperature-sputtered counterparts. The generalized information and relative mechanism about high-temperature-sputtered $Co/Si_{1-x}Ge_x$ silicidation should be useful for SiGe device considerations.

ACKNOWLEDGMENTS

The authors would like to thank Dr. T. C. Chang, Dr. W. F. Wu, and Dr. H. C. Lin for experiment assistance. This work was supported in part by the National Science Council of the Republic of China through Contract No. NSC89-2215-E009-050.

[1] X. Xiao, C. Sturm, S. R. Parihar, S. A. Lyon, D. Meyerhofer, S. Palfery, and F. V. Shallcross, IEEE Electron Device Lett. **EDL-14**, 199 (1993).
[2] G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbe, B. De Fresart, J. M. C. Stork, J. Y. C. Sun, D. L. Harame, and J. M. Burgatz, IEEE Electron Device Lett. **EDL-11**, 171 (1990).
[3] J. M. Stork, E. J. Prinz, and C. W. Magee, IEEE Electron Device Lett. **EDL-12**, 303 (1991).
[4] Q. Z. Hong and J. W. Mayer, J. Appl. Phys. **66**, 611 (1989).
[5] H. K. Liou, X. Wu, and U. Gennser, Appl. Phys. Lett. **60**, 577 (1992).
[6] R. D. Thompson, K. N. Tu, J. Angillelo, S. Delage, and S. S. Iyer, J. Electrochem. Soc. **135**, 3161 (1988).
[7] O. Thomas, F. M. D'Heurle, S. Delage, and G. Scilla, Appl. Surf. Sci. **38**, 27 (1989).
[8] O. Thomas, F. M. D'Heurle, and S. Delage, J. Mater. Res. **5**, 1453 (1990).
[9] W.-J. Qi, B.-Z. Li, W.-N. Huang, and Z.-Q. Gu, J. Appl. Phys. **77**, 1086 (1995).
[10] Z. Wang, Y. L. Chen, H. Ying, R. J. Nemanich, and D. E. Sayers, Mater. Res. Soc. Symp. Proc. **320**, 397 (1994).
[11] A. Buxbaum, M. Eizenberg, A. Raizman, and F. Schäffler, Appl. Phys. Lett. **59**, 665 (1991).
[12] M. C. Ridgway, R. G. Elliman, N. Hauser, J.-M. Baribeau, and T. E. Jackman, Mater. Res. Soc. Symp. Proc. **260**, 857 (1992).
[13] A. Appelbaum, R. V. Knoell, and S. P. Murarka, J. Appl. Phys. **57**, 1880 (1985).
[14] G. Ottaviani, K. N. Tu, P. Psaras, and C. Nobili, J. Appl. Phys. **62**, 2290 (1987).
[15] K. Inoue, K. Mikagi, H. Abiko, and T. Kikkawa, Tech. Dig. Int. Electron Devices Meet. **1995**, 445.
[16] K. Inoue, K. Mikagi, H. Abiko, S. Chikaki, and T. Kikkawa, IEEE Trans. Electron Devices **45**, 2312 (1998).
[17] Y. H. Wu, W. J. Chen, S. L. Chang, A. Chin, S. Gwo, and C. Tsai, IEEE Electron Device Lett. **20**, 200 (1999).
[18] J. U. Bae, D. K. Sohn, J. S. Park, B. H. Lee, C. H. Han, and J. J. Kim, Symposium on Very Large Scale Integrated Technology, 1999.
[19] W. K. Lai, H. W. Liu, M. H. Juang, N. C. Chen, and H. C. Cheng, IEEE Electron Device Lett. **19**, 259 (1998).
[20] F. Lin, G. Sarcona, M. K. Hatalis, A. F. Cserhati, E. Austin, and D. W. Greve, Thin Solid Films **250**, 20 (1994).
[21] M. Glück, A. Schuppen, M. Rösler, W. Heinrich, J. Hersener, U. König, O. Yam, C. Cytermann, and M. Eizenberg, Thin Solid Films **270**, 549 (1995).
[22] F. Wald and S. J. Michalik, J. Less-Common Met. **24**, 277 (1971).
[23] M. C. Ridgway, R. G. Elliman, R. Pascual, J. L. Whitton, and J.-M. Baribeau, Mater. Res. Soc. Symp. Proc. **311**, 155 (1993).
[24] L. P. Chen, C. T. Chou, G. W. Huang, and C. Y. Chang, Appl. Phys. Lett. **67**, 3001 (1995).
[25] P. L. Smith, C. M. Osburn, D. S. Wen, and G. McGuire, Mater. Res. Soc. Symp. Proc. **160**, 299 (1990).
[26] W. M. Chen, S. Pozder, Y. Limb, A. R. Sitaram, and B. Fiordalice, Mater. Res. Soc. Symp. Proc. **429**, 163 (1996).
[27] N. Boutarek and R. Mardar, Appl. Surf. Sci. **73**, 209 (1993).
[28] S. P. Ashburn, M. C. Öztürk, G. Harris, and D. M. Masher, J. Appl. Phys. **74**, 4455 (1993).
[29] Z. Wang, D. B. Aldrich, Y. L. Chen, D. E. Sayers, and R. J. Nemanich, Thin Solid Films **270**, 555 (1995).
[30] H. J. Huang, K. M. Chen, C. Y. Chang, T. Y. Huang, T. C. Chang, L. P. Chen, and G. W. Huang, J. Vac. Sci. Technol. (to be published).
[31] A. Bogen and J. Kuppers, Surf. Sci. **134**, 223 (1983).
[32] C. Cytermann, E. Holzman, R. Brener, M. Fastow, M. Eizenberg, M. Glück, H. Kibbel, and U. König, J. Appl. Phys. **83**, 2019 (1998).

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 140.113.38.11 On: Thu, 01 May 2014 07:45:58