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Dimensional effects on the reliability of polycrystalline silicon thin-film transistors

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Abstract

We found that for unpassivated short-channel TFTs, hot carrier stress-induced degradation phenomena are different with various channel geometries. For device with a wide channel width, the threshold voltage is increased while the subthreshold swing is almost unchanged. The stress-induced oxide-trapped charges are responsible for the degradation. For others with narrow channel widths after stress, on the contrary, the subthreshold swing and I_{min} are increased, the trap density is greatly increased and the trap-enhanced kink effect is also observed. This is due to the generation of stress-induced grain boundary traps near the drain side. Additionally, the stress-induced degradations of passivated TFTs with various geometries are identical. The increased defect density dominates the mechanism since the hot-carrier stress tends to break the passivated Si-H bonds.

1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been intensively studied for application to high-performance large-area active matrix liquid-crystal display (AMLCD) systems and static random access memory (SRAM). For circuit integration, it is essential to miniaturize the dimension of poly-Si TFT to meet the requirement of higher circuit density and higher drive current. However, because of the presence of grain boundaries in the poly-Si and the floating-body effect, as the channel length becomes smaller, poly-Si TFTs are known to suffer from severe short-channel effect and behave differently from their counterparts fabricated on single-crystal silicon substrate. Furthermore, stability of poly-Si TFT becomes worse at shorter channel length, which is the key obstacle to circuit integration.

As the grain-boundary trap density is related to the active channel dimension [1, 2, 3], we expect that the reliability of poly-Si TFTs should also be related to the active channel area. However, until now, little work has done on the influence of channel dimension on the reliability of short-channel poly-Si TFTs. In this paper, we investigate stress effects on short-channel poly-Si TFTs with different geometries and found that channel dimension has a profound influence on reliability.

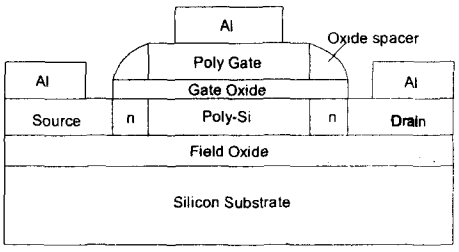

Fig. 1. Polysilicon thin-film transistor structure.

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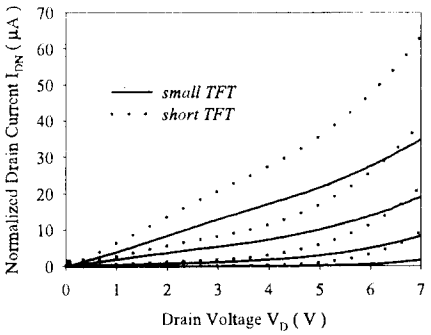


Fig. 2. The normalized I_D-V_D characteristics of *small TFT* and *short TFT*.

2. Experiments

The TFTs used in this study are conventional poly-TFTs with top-gate lightly-doped-drain (LDD) structure; the structure is shown in Fig. 1. The channel length of devices is kept at 1.2 μm, while the channel widths are 20 μm (referred to as *short TFT* hereafter) and 1.2 μm (referred to as *small TFT* hereafter). The process is as follows: First, a 100 nm undoped poly-Si layer was first deposited by low pressure chemical vapor deposition (LPCVD) without solid phase crystallization on an oxidized silicon buffer layer and patterned into individual active device islands. Then, a 50-nm TEOS oxide was deposited by LPCVD to serve as the gate insulator. A second poly-Si film was subsequently deposited and patterned to form the gate electrode. Next, lightly doped source/drain regions were formed by phosphorous (with $1x10^{13}$ cm^{-2} at 55 KeV) implants. A 400-nm self-aligned sidewall spacer was formed by the deposition of an TOES oxide layer and subsequent reactive-ion-etching. Afterwards, self-aligned n^+ source/drain regions were formed by heavy-dose phosphorous (with $5x10^{15}$ cm^{-2} at 70 KeV) implants. Dopant activation was then performed by rapid thermal annealing (RTA) at 750 °C for 20 seconds. An Al film was then deposited and patterned to form the electrodes, followed by nitrogen annealing. Finally, 2-hours NH_3 plasma passivation was applied by plasma enhanced chemical vapor deposition (PECVD).

After device fabrication, the typical parameters are extracted from the I-V characteristics of our devices. The threshold voltage V_{th} is defined as the gate voltage at which $I_D \times L/W$ = 100 nA for V_D = 5V. The trap state density N_t is extracted from the slope of the curve $\ln[I_D/(V_G-V_{FB})]$ versus $(V_G-V_{FB})^{-2}$ when the

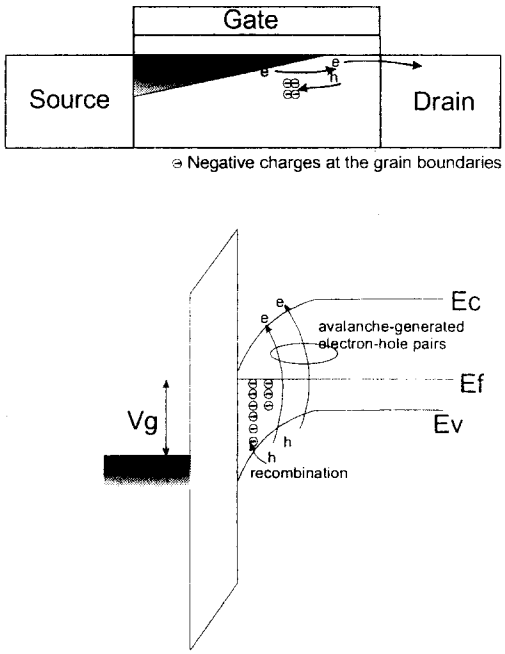


Fig. 3. An illustration to explain the trap-enhanced impact ionization effect.

Table I (a) Typical parameters of unpassivated *short TFT*

	Forward Mode		Reverse mode	
	Before stress	After 10000sec stress	Before stress	After 10000sec stress
V_{th} (V)	3.6	4.7	3.4	4.7
S.S. (V/dec)	1.24	1.30	1.29	1.32
I_{min} (pA)	5.7	5.2	5.3	5.1
Nt ($\times 10^{12}$ cm^{-2})	7.33	7.40	6.81	6.95

Table I (b) Typical parameters of unpassivated *small TFT*

	Forward Mode		Reverse mode	
	Before stress	After 10000sec stress	Before stress	After 10000sec stress
V_{th} (V)	4.56	5.6	4.8	5.3
S.S. (V/dec)	1.06	1.53	1.09	1.58
I_{min} (pA)	0.2	0.35	0.2	0.3
Nt ($\times 10^{12}$ cm^{-2})	5.8	7.5	4.9	8.2

V_D is 0.1V. The I_{min} and the subthreshold swing S.S. are extracted from the I_D-V_G characteristics when the V_D is 0.1volt. In addition, the stress condition is specified as $V_G = V_{th}$ + 1volt and $V_D = V_G$ + 2.5volt.

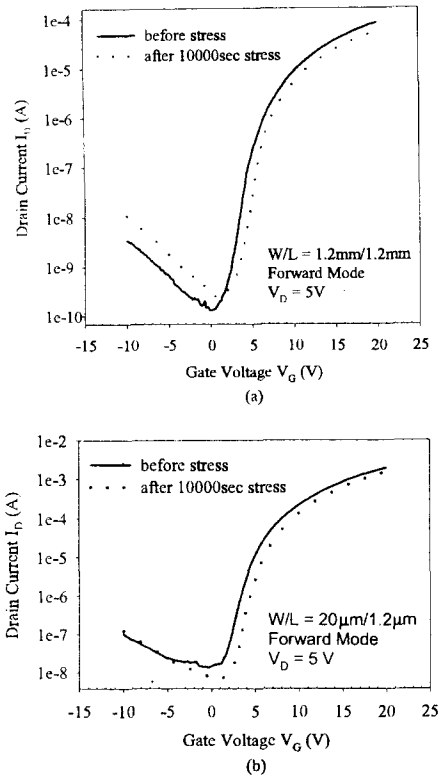


Fig. 4. The ID-VG characteristics of unpassivated (a) *small TFT* and (b) *short TFT* before and after stress.

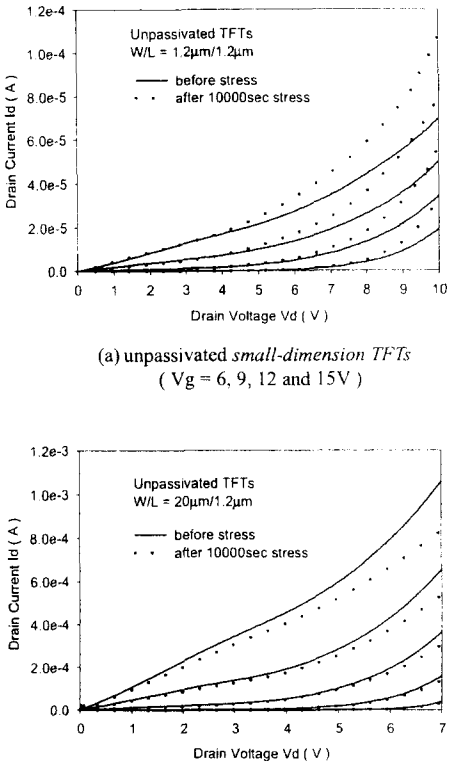


Fig. 5 The output characteristics of (a) unpassivated *small-dimension TFTs* and (b) unpassivated *short-channel TFTs* before and after 10000-sec hot-carrier stress.

3. Results and Discussions

3.1. Unpassivated short-channel TFTs

The normalized I_D-V_D characteristics of unpassivated *short* and *small TFTs* before stress are shown in Fig. 2, where the normalized I_D is define as $I_D \times L/W$. It is apparent that they both exhibit kink effects at large drain voltage. Since the channel lengths of the two devices are identical, it is reasonable to expect that the impact ionization rate should be similar. However, for *short TFT*, the kink effect is more pronounced than *small TFT*. The explanation is as follows, the *short TFT* has a larger N_t value than *small TFT* since larger active area contains more grain boundaries. Moreover, the kink effect is enhanced with the existence of grain boundary traps [4]. The mechanism is explained by Fig. 3. When impact ionization occurs, the avalanche-generated holes are swept away from the drain junction and flow toward the source region. Some of the holes will recombine with electrons trapped at the grain boundaries and therefore destroy the electrical equilibrium. Then, many more electrons are injected from the source to the pinch-off region to restore equilibrium. As a result, the larger the trap state density, the more avalanche-generated holes recombine with the negative charge, and the more pronounced the kink effect.

The typical parameters of unpassivated TFTs before and after 10000-sec hot-carrier stress are listed in Table I. For unpassivated *short TFT*, the threshold voltage is increased after stress while the subthreshold swing S.S. is almost unchanged, impling the generation of oxide trapped electrons after stress. For unpassivated *small TFT*, on the contrary, the subthreshold swing S.S. is increased after stress, indicating the increase of interface trap density of grain boundary trap density.

Table II (a) Typical parameters of passivated *short TFT*

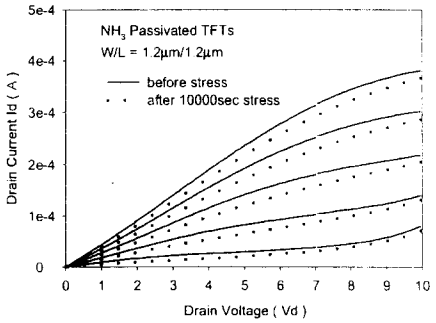
	Forward Mode		Reverse mode	
	Before stress	After 10000sec stress	Before stress	After 10000sec stress
V_{th} (V)	-1.05	-1.32	-1.08	-1.07
S.S. (V/dec)	0.26	0.28	0.28	0.29

Table II (b) Typical parameters of passivated *small TFT*

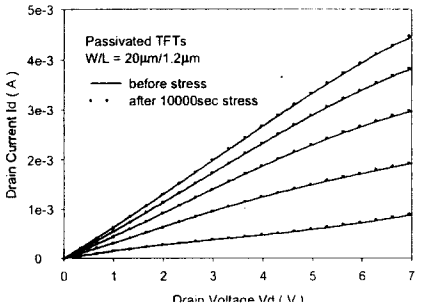
	Forward Mode		Reverse mode	
	Before stress	After 10000sec stress	Before stress	After 10000sec stress
V_{th} (V)	-0.61	-0.52	-0.64	0
S.S. (V/dec)	0.21	0.29	0.20	0.29

The I_D-V_G characteristics of unpassivated *small TFT* before and after stress are depicted in Fig. 4 (a). It is found that the ratio of the leakage current before stress I_{OFF}^{bs} to the leakage current after stress I_{OFF}^{as} remains almost constant independent of increasing gate voltage. This has been reported as the evidence of the increasing grain boundary trap density after stress [5,6]. Consequently, it can be concluded that the stress-induced traps of unpassivated *small TFT* are located in grain boundaries rather than at the silicon/oxide interface. Fig. 4 (b) depicts the I_D-V_G characteristics of unpassivated *short TFT* before and after stress. At positive gate voltages, there is a parallel shift of these characteristics to high absolute gate voltages, showing that the stressing does not create interface states or grain boundary traps which would change the slope of these result. On the other hand, trapping of electron in the gate oxide is responsible for the increased threshold voltage [5]. Unlike the unpassivated *small TFT*, there is strong dependence between the I_{OFF}^{bs} / I_{OFF}^{as} ratio and gate voltage for unpassivated *short TFT*. This indicates that the grain boundary trap generation is not the dominant stress-induced degradation phenomenon.

By comparing the trap density N_t of *small TFT* and *short TFT* listed in Table I, it can be found that, after stress, the former is increased greatly than the latter one. It means that under the same hot-carrier stress condition, the stress-induced degradation of *small TFT* seems to be severer than of *short TFT*. Similar discrepancy is also observed from the I_D-V_D characteristics of the two devices shown in Fig. 5 (a) and Fig. 5 (b). The kink effect of *short TFT* becomes less severe after stress, this is reasonable since the drain current is reduced due to the increased threshold voltage and therefore the kink effect is



(a) passivated *small-dimension TFTs*



(b) passivated *short-channel TFTs*

Fig. 6 The output characteristics of (a) passivated *small-dimension TFTs* and (b) passivated *short-channel TFTs* before and after 10000-sec hot-carrier stress. (Vg = 3, 6, 9, 12 and 15 V)

suppressed. For *small TFT*, on the contrary, the kink effect becomes more pronounced after stress. In spite of the increase of the threshold voltage, the great increase of acceptor-like trap density after stress enhances the kink effect and then dominates the characteristics. The different degradation phenomena of *small TFT* and *short TFT* are probably due to the self-heating effect. It is known that the temperature of device will be increased during stress, since the continued high drain current will heat the device. This effect is severer when the channel width is larger [7]. Consequently, the *short TFT* should have more pronounced self-heating effect than the *small TFT*. It has been reported that increasing temperature will suppress the kink effect [8]. The same condition is found from our devices. Therefore, although the stress voltage is kept constant, the stress current of short TFT is reduced with stress time, The stress-induced damage is thus less pronounced.

3.2. Passivated TFTs

The typical parameters of passivated TFTs are listed in Table II, both the threshold voltage V_{th} and

subthreshold swing S.S. increase after stress. This degradation is due to the increased defect density since the hot-carrier stress tends to break the passivated Si-H bonds. The output characteristics of passivated TFTs are depicted in Fig. 6. By comparing Fig. 5 and Fig. 6, we can find that the kink effect of passivated TFT (with small N_t value) is less severe than it of unpassivated ones (with large N_t value). This is consistent with previous discussion that the kink effect is enhanced with increasing N_t value.

4.Conclusion

Under hot-carrier stress, anomalous inconsistent degradation phenomena are found for unpassivated short-channel TFTs with different geometries. Those with narrower channel width tend to suffer more serious stress-induced degradation. Moreover, their kink effect is more pronounced after stress due to the increase of large amount of grain boundary trap density. The trap density of unpassivated short-channel TFT with wide channel width, on the contrary, remains almost the same after stress. The stress-induced degradation is dominated by the generation of oxide-trapped electron. For passivated short-channel TFTs with different geometries, the degradation phenomena are inconsistent. Since the hot-carrier will break the Si-H bonds, the increasing dangling bonds serve as traps and degrade the device characteristics.

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