Brief Papers

ESD Protection Design on Analog Pin with Very Low Input Capacitance for High-Frequency or Current-Mode Applications

Ming-Dou Ker, Tung-Yang Chen, Chung-Yu Wu, and Hun-Hsien Chang

***Abstract*—An electrostatic discharge (ESD) protection design is proposed to solve the ESD protection challenge to the analog pins for high-frequency or current-mode applications. By including an efficient power-rails clamp circuit into the analog input/output (I/O) pin, the device dimension (W/L) of an ESD clamp device connected to the I/O pad in the analog ESD protection circuit can be reduced to only 50/0.5 (μm/μm) in a 0.35-μm silicided CMOS process, but it can sustain the human body model (HBM) and machine model (MM) ESD level of up to 6 kV (400 V). With such a smaller device dimension, the input capacitance of this analog ESD protection circuit can be significantly reduced to only ~1.0 pF (including the bond-pad capacitance) for high-frequency applications.**

***Index Terms*—Analog pin, electrostatic discharge, ESD, input capacitance, on-chip ESD protection circuit.**

I. Introduction

ELECTROSTATIC discharge (ESD) has been the main reliability concern in semiconductor devices, especially in the scaled-down CMOS technologies [1], [2]. Due to the low breakdown voltage of the thinner gate oxide in deep-submicron CMOS technologies, an efficient on-chip ESD protection circuit should be designed to clamp the overstress voltage across the gate oxide of the internal circuits. A conventional ESD protection design with the two-stage structure for digital input pin is shown in Fig. 1, where a gate-grounded short-channel nMOS is used as the secondary protection device to clamp the overstress voltage across the gate oxide of the input circuits. To provide a high ESD level, a robust device (such as SCR [3], field-oxide device [4], or long-channel nMOS) is used as the main discharge element in the primary protection stage to bypass ESD current on the pad. Between the primary stage and the secondary stage, a resistor R is added to limit the ESD current flowing through the short-channel nMOS in the secondary stage. The primary ESD clamp device must be triggered on to bypass ESD current before the gate-grounded nMOS (ggnMOS) in the secondary stage is damaged by the overstress ESD current. If the primary ESD clamp device has a high turn-on voltage, the resistance of R should be large enough with an order of kΩ [3]. Such two-stage ESD protection design can provide high ESD level for the digital input pins. But the large series resistance and the large junction capacitance in the ESD clamp devices causes a long RC delay to the input signal, therefore this is not suitable for analog pins.

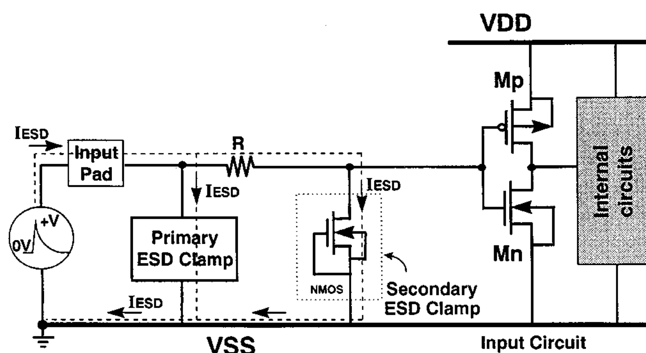

Fig. 1. Schematic diagram of the conventional two-stage ESD protection circuit for digital input pin in CMOS IC's.

For current-mode input signal or high-frequency applications, the series resistance between the input pad and input circuits is forbidden. Therefore, the two-stage ESD protection design in Fig. 1 is no longer suitable for such analog applications. To protect the analog input pin, the typical ESD protection circuit with a single-stage ESD protection design is shown in Fig. 2, where a ggnMOS is used as the ESD clamp device. Due to the lack of a series resistance to limit ESD current toward the ggnMOS, as well as that the ESD robustness of nMOS is seriously degraded by the advanced deep-submicron CMOS technologies [5]–[6], such a ggnMOS is often designed with a larger device dimension and a wider drain-contact-to-poly-gate layout spacing to sustain an acceptable ESD level [6], [7]. To further improve ESD level of the nMOS with a large device dimension, the gate-coupled circuit technique [8]–[10] or the substrate-triggering circuit technique [11] had been designed to uniformly trigger on the multiple fingers of the ESD protection nMOS. Besides, the additional silicide-blocked mask had been included into the deep-submicron CMOS process to increase ESD robustness of the ESD clamp device. The schematic cross-sectional view of a ggnMOS with the silicide-blocked drain region is illustrated in Fig. 3. But the ggnMOS with a larger device dimension and a wider drain-diffusion junction contributes a larger parasitic drain capacitance to the input pad. Such a parasitic junction capacitance is nonlinear and dependent on the input voltage

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M.-D. Ker, T.-Y. Chen, and C.-Y. Wu are with the Integrated Circuits and Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, R.O.C. (e-mail: mdker@ieee.org).

H.-H. Chang is with the Design Service Division, Taiwan Semiconductor Manufacturing Company (tsmc), Hsinchu, Taiwan 300, R.O.C.

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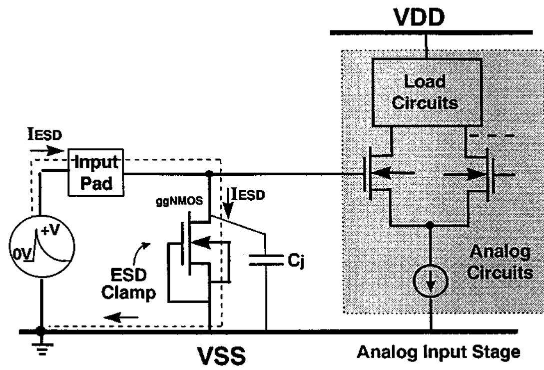

Fig. 2. A schematic diagram of the single-stage ESD protection circuit for analog input pin in CMOS IC's.

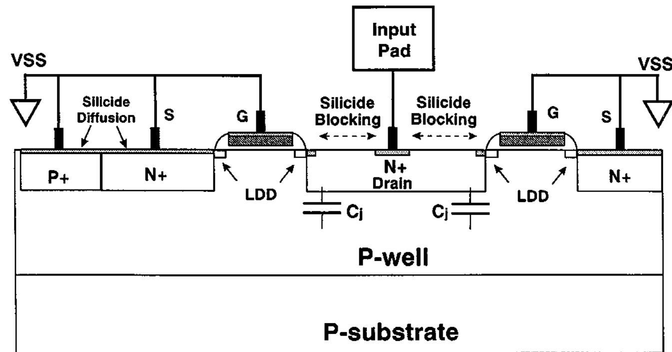

Fig. 3. The schematic cross-sectional view of the ggnMOS with the silicide-blocked drain region.

level. For some high-precision circuit operations, the input capacitance of an analog input pin is required to be kept as a constant as possible within the input voltage swing range. A major distortion source in high-precision analog circuits, especially in the single-ended input implementations, is the voltage-dependent nonlinear input capacitance associated with the ESD clamp devices at the analog input pad. The typical degradation on the circuit performance due to the nonlinear input capacitance of the input ESD clamp devices had been reported in [12], where the input capacitance varies from 4 to 2 pF due to the input voltage swing from 0 to 2 V. This nonlinear input capacitance causes an increase on the harmonic distortion in an analog-to-digital converter (ADC) and therefore degrades the precision of the ADC from 14 bit to become only 10 bit [12]. Thus, it has become an emergent challenge to design an effective ESD protection circuit for high-performance analog pins.

In this paper, a novel ESD protection design with the advantages of small input capacitance, no series resistance, and high ESD level, has been practically implemented in a 0.35-μm CMOS technology to protect the analog pins for high-frequency and high-performance applications.

II. ESD Test on Analog Input / Output Pins

To investigate the ESD robustness of input/output (I/O) pins in IC's, the pin combinations for ESD zapping had been specified in the test standards [13]–[15]. One of the ESD-test pin combinations to verify ESD level for an input (or output) pin is shown in Fig. 4, where the ESD voltage is applied to an input (or output) pin with the VDD or VSS pins relatively grounded. Except for such ESD-zapping pin combinations, an additional analog pin-to-pin ESD stress had been especially specified in the standards for the analog circuits with operational amplifiers or differential input stages to verify the ESD level of the analog pins. The analog pin-to-pin ESD stress for the differential input pins of an operational amplifier is illustrated in Fig. 5, where the positive or negative ESD voltage is applied to the inverting input pin with the corresponding noninverting input pin relatively grounded. During such an analog pin-to-pin ESD stress, all the other pins including both the VDD and VSS pins are floating.

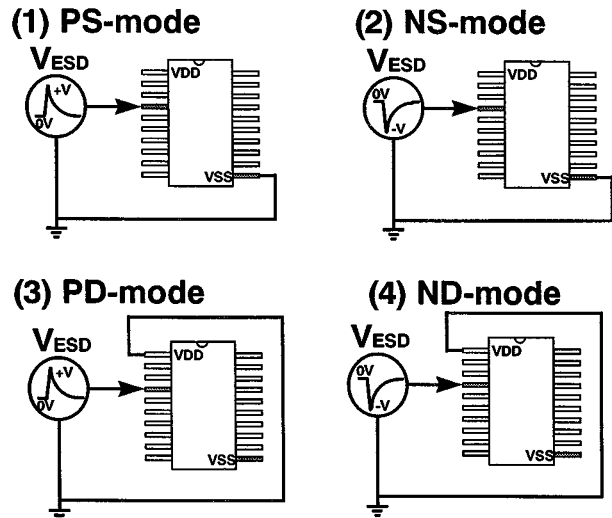

Fig. 4. One of the ESD-test pin combinations on an input (or output) pin of an IC in the human body model (HBM) and machine model (MM) ESD stresses.

The ESD current during such an analog pin-to-pin ESD stress is illustrated in Fig. 6 with the differential input stage of an operational amplifier. Because of the lack of series resistor between the analog input pad and the input circuits, the overstress ESD current easily reaches to the thinner gate oxide of the differential input stage with a common-source circuit structure. If the VSSA power connection between the inverting input pin and the noninverting input pin has a long metal line in the IC layout, the gate oxide of the differential input stage is easily ruptured by the ESD voltage to generate an ESD current discharging path, as the dashed line shown in Fig. 6. The ESD clamp device (such as the large-dimension ggnMOS in Fig. 2) between the inverting input pad and the VSSA power line cannot provide effective ESD protection against this additional analog pin-to-pin ESD stress. Therefore, some advanced designs should be included into the analog ESD protection circuit to overcome this analog pin-to-pin ESD-stress issue.

III. ESD Protection Design for Analog Pins

A. Circuit Configuration and Operation

The proposed ESD protection circuit for analog pins is shown in Fig. 7, whereas its practical layout in a 0.35-μm silicided

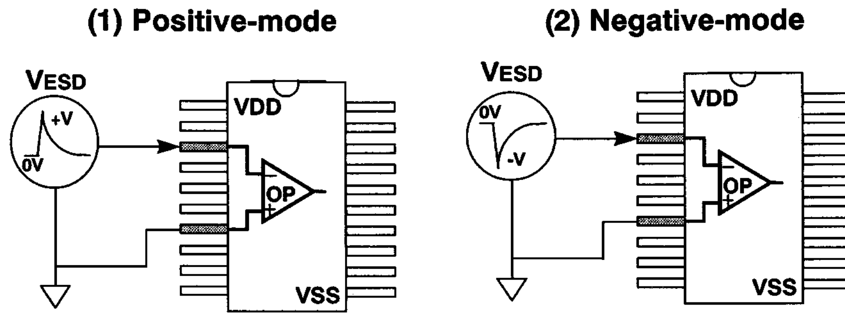

Fig. 5. Pin combination of the additional analog pin-to-pin ESD stress to verify the ESD level of analog circuits with the operational amplifier or differential input stage.

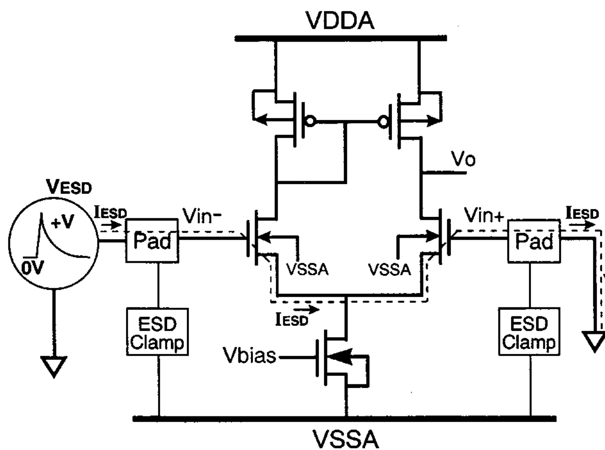

Fig. 6. ESD current path during the analog pin-to-pin ESD stress.

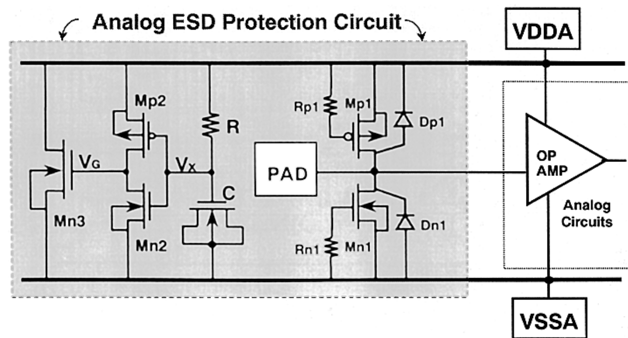

Fig. 7. Proposed ESD protection circuit for analog pins.

CMOS cell library is drawn in Fig. 8. In Fig. 7, the Dp1 (Dn1) is the parasitic junction diode in the drain region of Mp1 (Mn1) device. In order to reduce the input capacitance of the analog pin, the Mn1 and Mp1 are both designed with a much smaller device dimension (W/L) of only 50/0.5 (μm/μm). The HBM ESD level of a standalone nMOS with a device dimension of 50/0.5 (μm/μm) is less than 500 V in the 0.35-μm silicided CMOS process, while the nMOS is zapped in the PS-mode ESD stress (nMOS in the drain-breakdown condition). But, such a small nMOS can sustain an HBM ESD level of 8000 V in the same 0.35-μm silicided CMOS process, while the nMOS is zapped in the NS-mode ESD stress (nMOS in the drain diode forward-bias condition). Therefore, an nMOS has quite different ESD levels between the PS-mode and NS-mode ESD stresses. Similarly, a standalone pMOS with a small device dimension also has a high ESD level in the PD-mode ESD stress but has a much low ESD level in the ND-mode ESD stress.

To avoid the small-dimension Mn1 and Mp1 into the drain-breakdown condition in the PS-mode and ND-mode ESD stresses to cause a much lower ESD level, an efficient ESD clamp circuit between the power rails is co-constructed into the analog ESD protection circuit to increase the overall ESD level. In Fig. 7, the *RC*-based ESD detection circuit [16]–[17] is used to trigger on the Mn3 device, when the pad is zapped in the PS-mode or ND-mode ESD stresses. Because the Mn1 in the PS-mode (Mp1 in the ND-mode) ESD stress is not operated in the drain-breakdown condition, the ESD current is bypassed through the forward-biased drain diode Dp1 in Mp1 (Dn1 in Mn1) and the turned-on Mn3. The Mn3 is especially designed with a larger device dimension ($W/L = 1800$ μm/0.5 μm in Fig. 8) to sustain a high ESD level. Although the large-dimension Mn3 has a large junction capacitance, this capacitance does not contribute to the analog pad. Therefore, the analog pin can sustain a much higher ESD level but only with a very small input capacitance.

When the input pins are zapped in the analog pin-to-pin ESD stress (Fig. 6), the ESD current path along this proposed analog ESD protection circuit is illustrated in Fig. 9. During the pin-to-pin ESD stress, both of the VDDA and VSSA power lines in the IC are floating. The ESD current is first conducted from the zapped pad to the VDDA power line through the junction diode Dp1 in the Mp1 of input ESD protection circuit. Therefore, the VDDA line is charged by the ESD energy. The VSSA line initially has a voltage level near to ground because the VSSA line is connected to a grounded pad through the diode Dn4 in Mn4 of another input ESD protection circuit. The pin-to-pin ESD-stress voltage across the two pins of differential input stage therefore becomes across the VDDA and VSSA power lines. The Mn3 connected between the VDDA and VSSA power lines is turned on by the *RC*-based ESD-detection circuit to bypass the ESD current from VDDA to VSSA. Finally, the ESD current flows out the chip from the VSSA power line to the grounded pad through the forward-biased diode Dn4 in Mn4. With suitable design on the ESD-detection circuit to quickly turn on the Mn3 [17], the pin-to-pin ESD stress can be quickly discharged away from the gate oxide of the differential input stage. The pin-to-pin ESD current

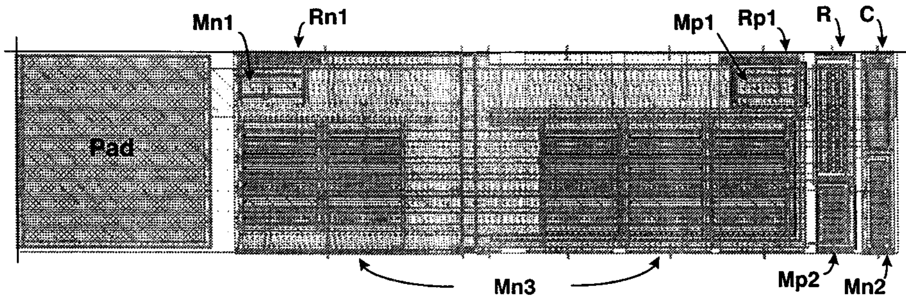

Fig. 8. Layout example of the proposed ESD protection circuit for analog pins in a 0.35-μm silicided CMOS process.

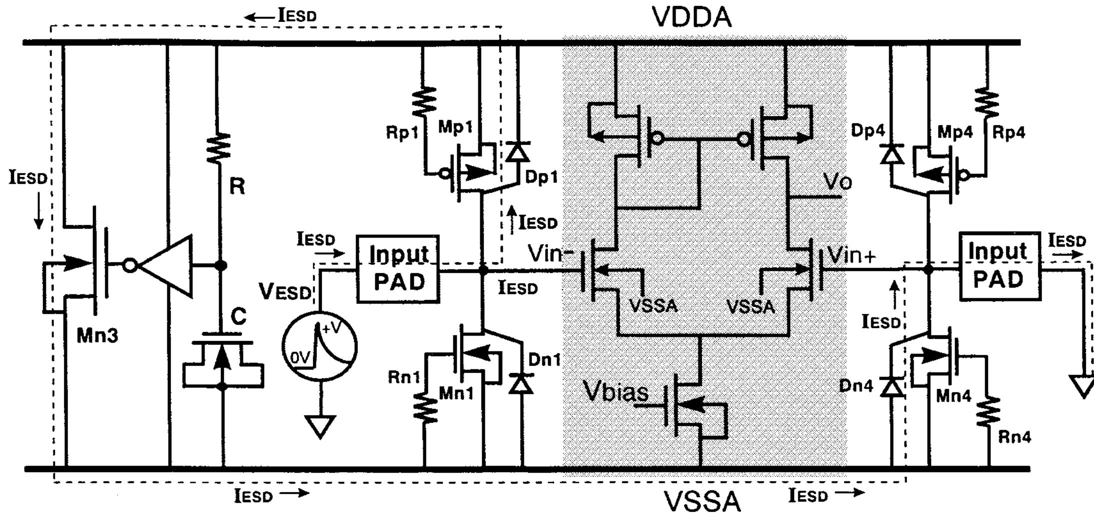

Fig. 9. ESD current path in the proposed analog ESD protection circuit when the input pins are zapped in analog pin-to-pin ESD stress.

discharging path shown in Fig. 9 is therefore quite different from that shown in Fig. 6. By using this design, the gate oxide of the analog differential input stage can be fully protected without adding any series resistance between the input pad and analog input circuits. Therefore, the analog input signal can have the widest bandwidth from the pad to the internal circuits, which are protected by the proposed analog ESD protection circuit.

By using the pure diodes as the input ESD clamp devices, they can also perform the required circuit operation as that of the Mn1 and Mp1 in Fig. 7. But, in the actual ESD zapping events, the turned-on ESD clamp device (Mn3) has a turn-on resistance. When a much higher ESD voltage is applied to the pad, the clamped voltage on the pad may have a somewhat overshooting voltage due to the ESD current flowing through the turn-on resistance of Mn3. Therefore, the clamped voltage on the pad could be slightly higher to close to the gate-oxide breakdown voltage of the input stage. To further protect the thinner gate oxide of the analog input stage, where there is no series resistor connected from the pad to the input gate oxide, the Mn1 and Mp1 are used in this design to limit the overshooting voltage on the pad to its snapback voltage. The short-channel Mn1 has a much lower snapback voltage (~6.5 V) than its drain-breakdown voltage (~8.5 V) in the 0.35-μm CMOS technology. The pure diode in its breakdown region has no snapback behavior as that of the nMOS. Thus, the Mn1 has a safer margin to protect the thinner gate oxide of the analog input stage as compared to the pure diodes.

B. Input Capacitance

The input capacitance of this proposed analog ESD protection circuit can be calculated as

$$C_{\text{in}} = C_{\text{PAD}} + C_n + C_p \tag{1}$$

where the C_{PAD} is the parasitic capacitance of the bond pad. The $C_p(C_n)$ is the drain junction capacitance and the drain-to-gate overlapped capacitance in the Mp1 (Mn1). The drain junction capacitance of a single nMOS or pMOS is strongly bias-dependent. The input capacitance of the previous ESD protection design with a single nMOS in Fig. 2 varies extensively when the input signal has different voltage level. But, the input capacitance of the proposed analog ESD protection circuit (Fig. 7) with a complementary pMOS and nMOS structure can be kept almost constant even if the input signal has a voltage swing from 0 V to VDD (3 V). The total input junction capacitance of the analog ESD protection circuit with different device dimensions are accurately calculated in the frequency domain by using the pin-capacitance measurement simulation [18] in the Star-Hspice CAD tool.

The calculated results are shown in Fig. 10, where the channel widths of Mn1 and Mp1 vary from 50 to 400 μm with a fixed channel length of 0.5 μm under different voltage levels on the

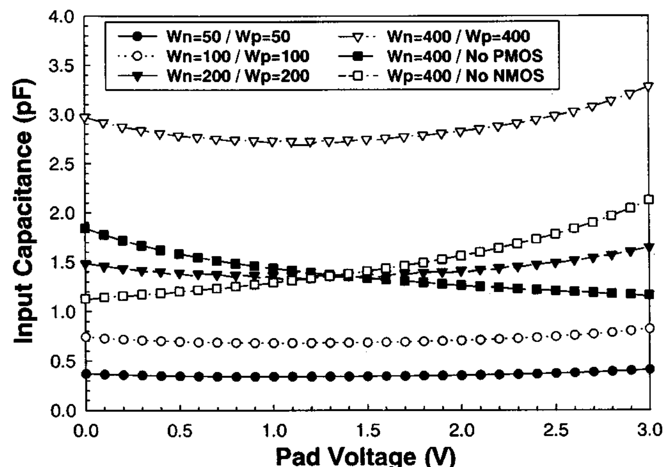

Fig. 10. Input junction capacitance of the analog ESD protection circuit with different device dimensions in Mn1 and Mp1 under different input voltage levels on the pad.

input pad. The drain-contact-to-poly-gate spacing in both Mn1 and Mp1 is drawn as 3.4 μm, whereas the source side spacing is drawn as 1.55 μm. With both device dimensions of 50/0.5 in Mn1 and Mp1, the input capacitance of the proposed analog ESD protection circuit only varies from 0.37 to 0.4 pF when the input voltage swing is from 0 to 3 V. But the input capacitance of the traditional ESD protection circuit in Fig. 2 with a ggnMOS of W/L =400/0.5 (μm/μm) varies from 1.83 to 1.12 pF when the input voltage swing is from 0 to 3 V in an IC with 3-V VDD power supply.

The layout size of the metal bond pad for wire bonding in the 0.35-μm CMOS process is drawn as 96 $\times$ 96 μm^2, which contributes a parasitic $C_{\rm PAD}$ of 0.67 pF. So, the total input capacitance of this analog ESD protection circuit including the bond pad is only about 1.04$\sim$1.07 pF, even if the input signal has a voltage swing from 0 to 3 V.

IV. Experimental Results

The proposed analog ESD protection circuit has been practically fabricated in a 0.35-μm silicided CMOS process to protect the inverting and noninverting input pins of an operational amplifier. The silicide-blocked mask is also used on the device Mn1, Mp1, and Mn3 to improve their ESD robustness, but without using the extra ESD-implanted process modification.

The fabricated analog ESD protection circuits are zapped by the *ZapMaster* ESD tester in both the HBM [13] and MM [14] ESD stresses. The ESD test results of the maximum ESD sustain voltage are summarized in Table I, which includes the analog pin-to-pin ESD stress. The failure criterion is defined as the leakage current at the pad exceeds 1 μA under 5-V voltage bias after any ESD zapping. As shown in Table I, the proposed analog ESD protection circuit can successfully provide the analog pins with an HBM (MM) ESD level of above 6000 V (400 V) in all ESD-stress conditions, without adding any series resistor between the pad and the internal circuits. This verifies the protection effectiveness of the proposed analog ESD protection circuit, especially in the analog pin-to-pin ESD stress.

The conventional ESD protection design in Fig. 2 with a ggnMOS of W/L = 480/0.5 (μm/μm) for analog input pin is

TABLE I
ESD Level of the Proposed Analog ESD Protection Circuit Under Different Pin Combinations in the Human Body Model (HBM) and the Machine Model (MM) ESD Test

	Pin Combination in ESD Test				
	PS-mode	NS-mode	PD-mode	ND-mode	Pin-to-Pin
HBM (V)	6000	- 8000	7000	- 7000	6000
MM (V)	400	- 400	400	- 400	400

also fabricated in the same testchip as a reference. The HBM PS-mode ESD level of the design in Fig. 2 is about 3 kV, but its analog pin-to-pin HBM ESD level is below 500 V. The pin-to-pin ESD damage location is founded on the poly gate of the input stage in the operational amplifier circuit. So, the conventional ESD protection design cannot protect the thinner gate oxide of the differential input stage in deep-submicron CMOS technologies during the pin-to-pin ESD stress.

V. Conclusion

An analog ESD protection circuit with a very low and almost constant input capacitance, high ESD level, and no series resistance has been successfully designed and verified in a 0.35-μm silicided CMOS process. The ESD test results and turn-on verification have shown that the proposed analog ESD protection circuit can effectively protect the analog circuits, especially the differential input stage under the pin-to-pin ESD-stress condition. With a very low and almost constant input capacitance, the proposed analog ESD protection circuit is very suitable to protect both the analog input and output pins against ESD stress for current-mode, high-frequency, or high-resolution circuit applications. This analog ESD protection circuit has been included into the cell libraries and practically applied in many IC products, such as the cable modem IC, data communication IC, video graphic IC, network IC, chip set IC, DVD IC, and so on, which had been manufactured in the tsmc 0.35-μm or 0.25-μm CMOS processes.

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