Characteristics of Polysilicon Oxides Combining N_2O Nitridation and CMP Processes

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***Abstract*—This paper present a high-quality polysilicon oxide combining N_2O nitridation and chemical mechanical polishing (CMP) processes. Experimental results indicate that polyoxide grown on the CMP sample exhibits a lower leakage current, higher dielectric breakdown field, higher electron barrier height, less electron trapping rate, higher charge-to-breakdown (Q_{bd}), and lower density of trapping charge than those of non-CMP samples. In addition, the CMP process enhances nitrogen incorporation at the interface by the N_2O nitridation, ultimately improving the polyoxide quality. Moreover, the CMP process smooths the surface of polysilicon and this planar surface reduces the out-diffusion of the phosphorous during thermal oxidation.**

I. Introduction

TO OBTAIN adequate data retention in nonvolatile memories, polysilicon oxides are required by a low-leakage current, high dielectric strength, and high charge to breakdown [1]–[3]. However, a rough surface at polysilicon-oxide/polysilicon interface and the nonuniform polyoxide thickness produce a high local electric field. This high local electric field causes polyoxide to exhibit a high leakage current and lower dielectric breakdown field than those of silicon dioxide grown from a single crystalline silicon substrate [4]–[7]. As is well known, the integrity of polysilicon oxide heavily depends on the oxidants used for growth or post-oxidation annealing [9]–[15]. Previous investigations have employed a process to improve electric properties of polysilicon oxides grown in N_2O ambient [14], [15]. According to their results, such an improvement is largely owing to the incorporation of nitrogen by using N_2O. The CVD deposition oxide annealed in N_2/N_2O has a relatively smooth surface at the polysilicon-oxide/polysilicon interface [10]–[13]. Such a smooth surface is owing to that the grain boundaries of the bottom polysilicon do not propagate into the polyoxide film like the polyoxides grown by thermal oxide. Another approach is to improve the surface morphology of polysilicon by using an adequately controlled chemical mechanical polishing (CMP) process on bottom polysilicon film [16], [17]. The planar surface morphology, after the CMP process, has been shown to result in an improved integrity of polysilicon oxide. Moreover, polyoxide grown by combining N_2O nitridation and CMP process can have a significant improvement on integrity of polyoxide [17]. However, the actual mechanism has not been clarified.

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TABLE I
LIST OF THE DEVICE TYPES FABRICATED

CMP or Non		Non-CMP				CMP			
Ambient gas		O_2		N_2O		O_2		N_2O	
Temperature (℃)		900							
Thickness (nm)		10	13	11.5	14.7	10.7	13.5	11.6	14
Surface Roughness R.M.S. (nm)		5.0~5.4		4.0~4.4		1.7~2.0		1.7~1.9	
C.E.F. (MV/cm)	(+Vg)	7.24	6.5	7.63	6.77	7.8	6.9	7.98	7.14
	(-Vg)	6.96	6.34	7.2	6.64	7.7	6.16	7.8	6.25
Q_{bd} (C/cm^2)	(+Vg)	0.46	0.18	0.56	0.22	0.76	0.22	1.67	0.77
	(-Vg)	0.15	0.08	0.2	0.09	0.3	0.1	0.46	0.21
Barrier Height (eV)	(+Vg)	2.49	2.15	2.55	2.34	2.95	2.77	2.9	2.76
	(-Vg)	2.65	2.59	2.4	2.2	2.8	2.67	2.82	2.71

In light of above discussion, this work presents high quality polysilicon oxide grown combining N_2O nitridation and CMP process. The electrical integrity of four different polyoxides (grown in N_2O/O_2 and/or CMP/non-CMP processes) is also investigated. In addition, the surface roughness and surface morphology of polyoxide/polysilicon interface are characterized by using AFM and TEM analyses. Moreover, SIMS analysis is performed to investigate depth profiles of phosphorous and nitrogen.

II. Experimental

In this study, n^+polysilicon/polyoxide/n^+polysilicon capacitors were fabricated. Samples were fabricated on p-type (100) silicon wafers which were oxidized to grow 2000 Å silicon dioxide films. A 3000 Å poly-Si film, poly-1, was deposited at 620 °C and doped by $POCl_3$ (with a sheet resistance of 50–70 $\Omega/\square$). Some of the poly-Si films were polished by using the CMP process [16], followed by cleaning in a scrubber and ultrasonic oscillator with $NH_4OH:H_2O_2:H_2O$ (= 1:1:10) solution to remove the particles and metallic contamination. Next, an additional RCA clean process was performed. Polysilicon oxides were then grown in two oxidants: one was in dilute dry O_2 ambient ($N_2:O_2$ = 6:1) at 900 °C and the other in pure N_2O ambient at 900 °C. The samples oxidized in N_2O or O_2 but without CMP process were referred to as non-CMP-N_2O or non-CMP-O_2,

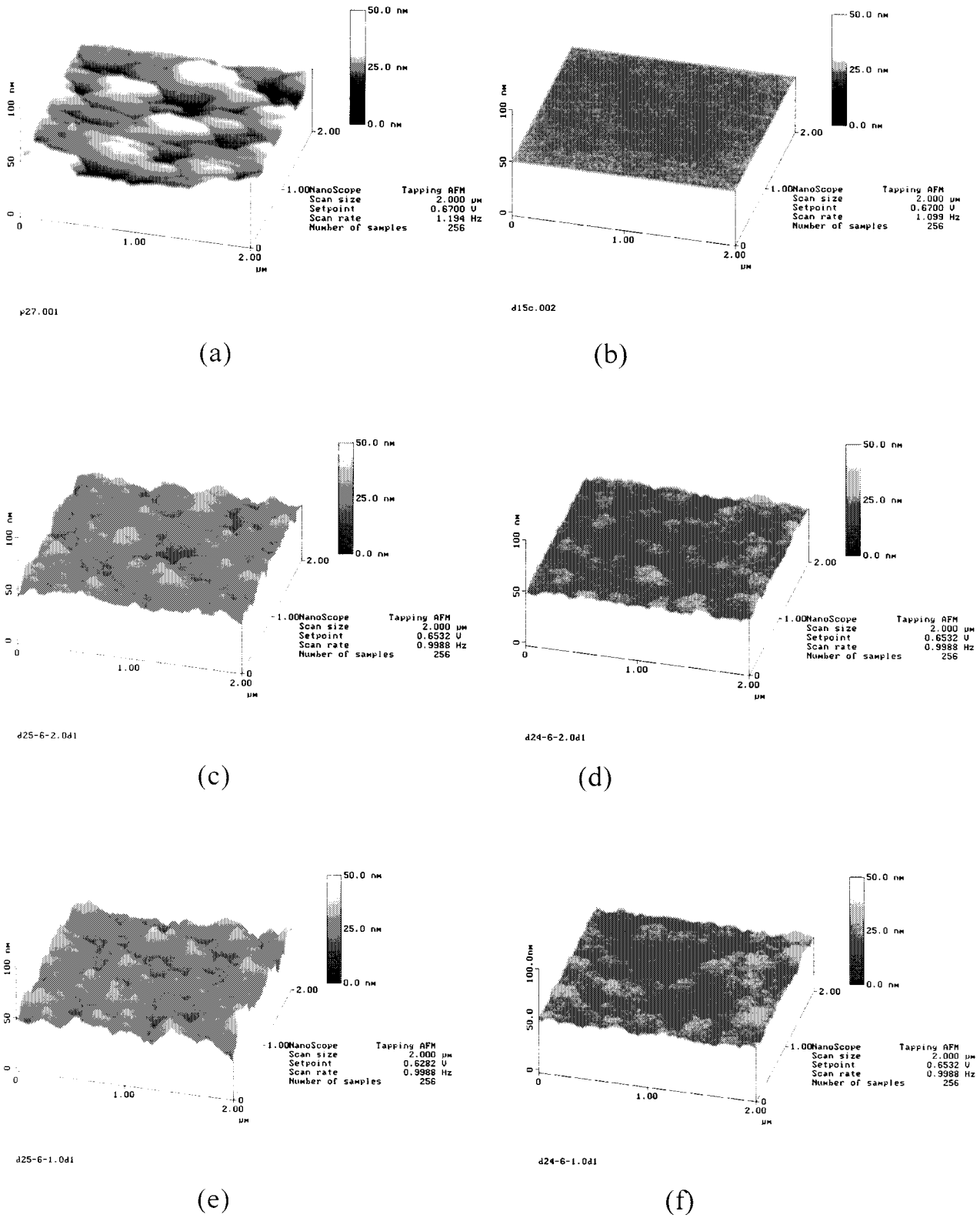

Fig. 1. Surface image measured by AFM for (a) without CMP before oxidation (b) with CMP before oxidation, (c) non-CMP-O_2 after oxidation, (d) CMP-O_2 after oxidation, (e) non-CMP-N_2O after oxidation, and (f) CMP-N_2O after oxidation.

respectively; with the CMP process, they were referred to as CMP-N_2O or CMP-O_2. After oxide growth, poly-2 was deposited and doped to a sheet resistance of 25–35 $\Omega/\square$ by $POCl_3$. poly-2 was defined and etched to form the capacitors. All samples were thermally oxidized to grow a 1000 Å-thick oxide using wet oxidation. Contact holes were opened and, then, alumimun was deposited and patterned to form contacts to the poly-2 electrodes.

Table I lists all of the device types fabricated in this work, along with their measured critical electric field (CEF) (measured

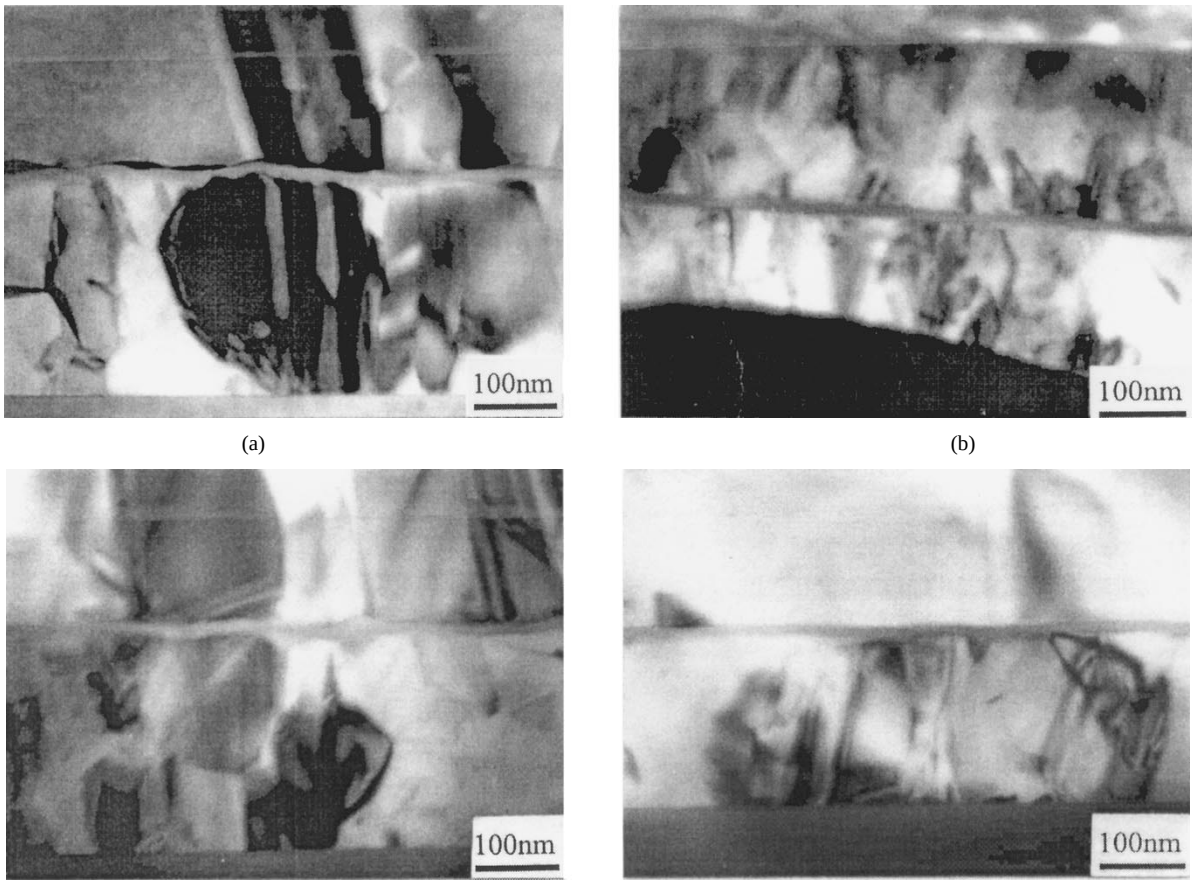

Fig. 2. TEM micrographs of (a) non-CMP-O_2, (b) CMP-O_2, (c) non-CMP-N_2O, and (d) CMP-N_2O.

at the leakage current of 10^{-6} A/cm^2), charge-to-breakdown (Q_{bd}), performed under $+10$ mA for $+Vg$ injection and -10 mA for $-Vg$ injection, and the effective barrier height (ϕ_b), which is given by the slope of $J/(Eox)^2$ versus $1/Eox$ plot [2]. The capacitor area is 6×10^{-4} cm^2. The polysilicon oxide thickness was determined by using Keithley capacitance–voltage (*C–V*) measurement. The surface roughness, RMS, was studied by using atomic force microscope (AFM). To reveal the actual surfaces of our samples, the surface morphology was measured after the polyoxide was stripped in diluted HF solution. Next, electrical characteristics and constant current stress were performed using an HP4156 semiconductor parameter analyzer. The surface morphology of polyoxide was also studied by transmission electron microscope (TEM). Finally, the SIMS depth profiles of phosphorous and nitrogen were investigated.

III. Results and Discussion

Fig. 1(a)–(f) depicts the surface morphology images of polysilcon-oxide/polysilicon interfaces investigated by AFM. To reveal the actual surface of the polysilicon layers after the thermal oxidation, dilute HF solution was used to strip the oxides. Fig. 1(a) and (b) illustrates the original surface without/with CMP before oxidation. Fig. 1(c) and (e) displays the AFM image of the non-CMP polysilicon after oxidation for non-CMP-O_2 and non-CMP-N_2O samples, respectively. For the CMP samples, either with O_2 or N_2O, a smooth and uniform surface was observed, as shown in Fig. 1(d) and (f). For the non-CMP samples, the root-mean-square roughness of polysilcon-oxide/polysilicon interface after oxidation in dilute O_2 ambient (5.0–5.4 nm) was slightly larger than that in N_2O ambient, (4.0–4.4 nm). The original surface without CMP before oxidation was $\sim$4.3 nm. For the CMP samples, polyoxide grown in O_2 and in N_2O have interface roughness in the same level (O_2: 1.7–2.0 nm; N_2O: 1.7–1.9 nm) where the original surface with CMP before oxidation was $\sim$0.15 nm.

Fig. 2(a)–(d) presents cross-section TEM pictures of these four samples. According to these figures, the CMP samples in Fig. 2(b) and (d) have smoother surfaces than those of the non-CMP samples in Fig. 2(a) and (c). In thermal oxidation of poly-Si, grain boundaries are oxidized more rapidly than the center of the grains. The enhanced oxidation of grain boundaries makes V-grooves at the polyoxide/poly-Si interface [5]. For the smoother initial surface morphology (CMP samples), the sizes of grooves are smaller than that of rougher initial surface (non-CMP samples) after oxidation. This is match to the cross-section TEM pictures in Fig. 2.

Fig. 3(a) displays the SIMS depth profiles of phosphorous for CMP and non-CMP samples. The subsequence concentration was computed, divided, and normalized by the counts of Si in this sample. According to this figure, a high amount of phosphorous pile up near poly-2/polyoxide interface (upper part of polyoxide) for both CMP and Non-CMP samples.

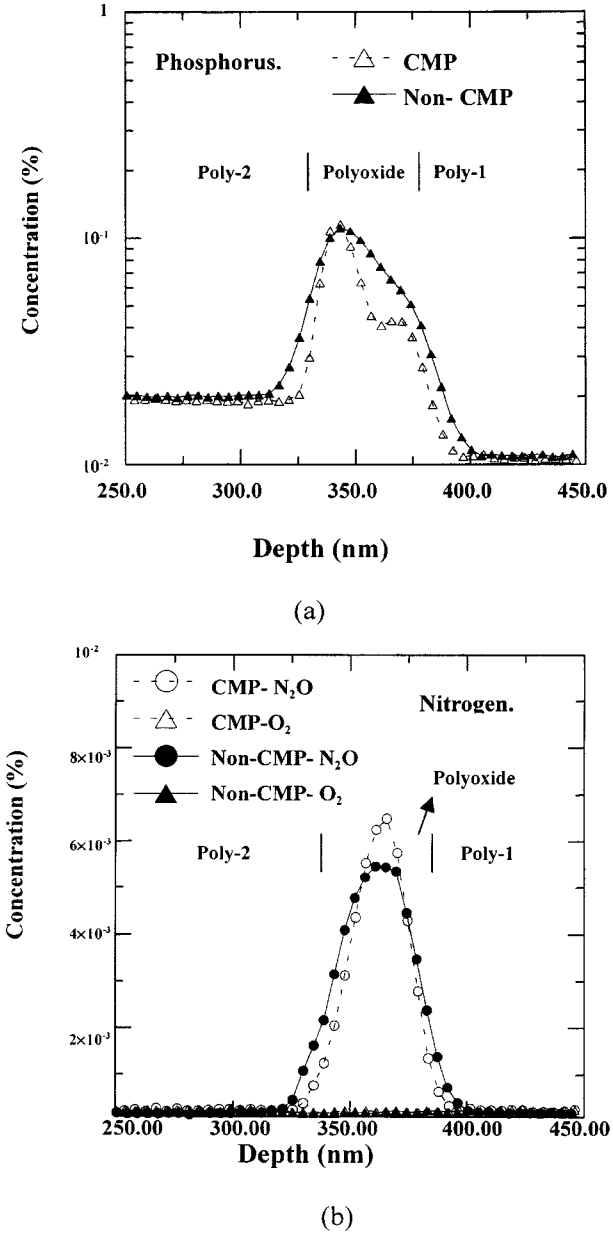

Fig. 3. SIMS depth profile of (a) phosphorus in CMP and non-CMP polyoxides, and (b) nitrogen in non-CMP-N_2O/O_2, CMP-N_2O/ O_2 polyoxides, respectively.

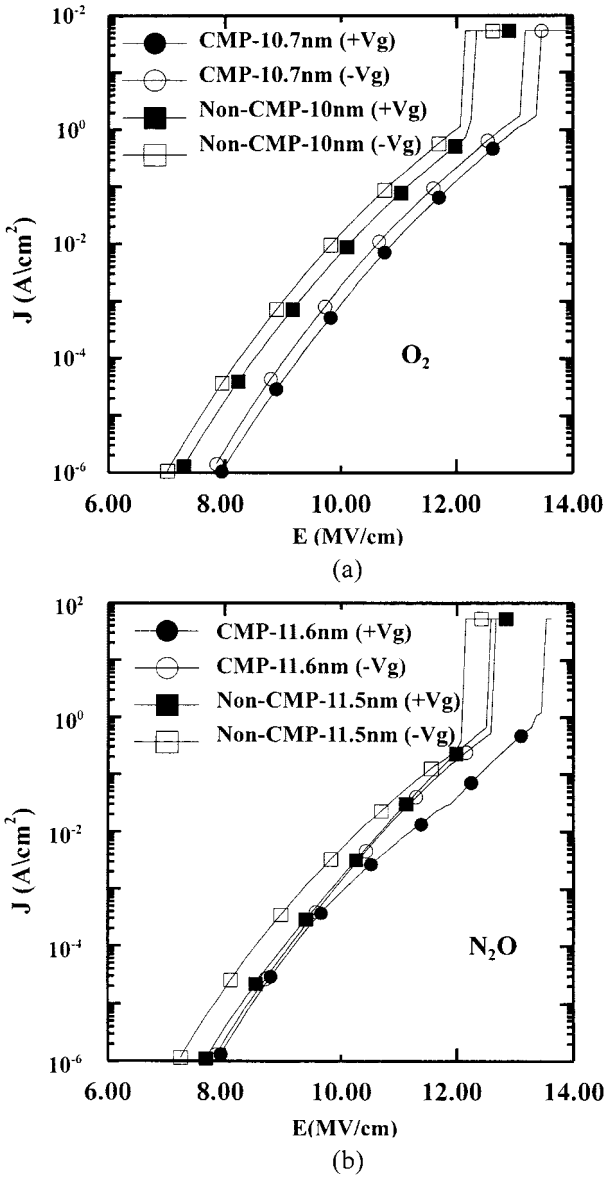

Fig. 4. *J–E* characteristics of polyoxides (a) CMP/ non-CMP-O_2, and (b) CMP/non-CMP-N_2O.

However, the profile of phosphorous near polyoxide/poly-1 (lower part of polyoxide) was more dramatically reduced in CMP sample than that in non-CMP sample. Due to the out-diffusion of phosphorus from poly-1 into polyoxide during the oxidation process, a large amount of phosphorus would pile up at or near the polyoxide/polysilicon interface [18] and the phosphorus precipitates would remain in the polysilicon grain boundary and in the bulk of polyoxide [3]. The interface between oxide and poly is a better sink for phosphor atoms than either the oxide or the polysilicon. So does the grain boundaries among polysilicon grains. A smoother interface has smaller interface area and shallow grain boundary regions, therefore accumulated fewer phosphor atoms. The rougher the surface of the non-CMP samples, the more mount of phosphorous was interfacial accumulated.

Fig. 3(b) depicts the SIMS depth profiles of nitrogen for these four samples. This figure indicates that nitrogen was observably incorporated into the polysilicon oxides after oxidation in N_2O ambient. Moreover, the nitrogen profile of the CMP-N_2O sample exhibits the narrowest and largest peak distribution among these four samples. A previous investigation has suggested that, during the high temperature of thermal oxidation, the oxidant may diffuse deeper through the grain boundary in the rougher (or nonuniform) surface and have a broader and lower nitrogen distribution [17].

Fig. 4(a) and (b) shows the J-E characteristics of polyoxides. In this study, n^+polysilicon/polyoxide/n^+polysilicon capacitors were fabricated. The *J–E* curve is calculated by the initial current–voltage (*I–V*) curve of polyoxide, where $J = I/$(area of capacitors) and $E = V/$(thickness of oxide). Obviously, for both O_2 and N_2O grown polyoxides, CMP samples were conducted at a lower leakage current and a higher breakdown elec-

tric field than those of non-CMP samples under both positive $(+Vg)$ and negative $(-Vg)$ poly-2 injection. This phenomenon is attributed to the high local electric field, which is attributed to the nonuniformities in the polyoxide film thickness and to the asperities at polyoxide/poly-1 interface [1], at the injection rough interface of the non-CMP samples [16]. Consequently, a smoother surface of polyoxide/poly-1 of the CMP sample results in a small localized current density as well as an improved uniformity of localize electric field under the same bias electric field. Furthermore, the CMP sample also has higher current than the non-CMP sample at dielectric breakdown. For both CMP and non-CMP samples, polyoxide exhibits a higher conductance and a lower dielectric breakdown electric field under negative $(-Vg)$ poly-2 injection than that under positive $(+Vg)$ poly-2 injection. This occurrence implies that the interface of polyoxide/poly-1 is superior to the poly-2/polyoxide. A previous study has reported on this phenomenon as well [16], [18]. In addition, due to the outdiffusion of phosphorus from poly-1 into polyoxide during the oxidation process, as confirmed by the SIMS depth profile in Fig. 3(a), a large amount of phosphorus would pile up at or near the polyoxide/polysilicon interface [18] and the phosphorus precipitates would remain in the polysilicon grain boundary and in the bulk of polyoxide. These precipitates act as the electron trapping sites and result in an increase in the leakage current due to the trap-assisted direct tunneling [3], [18]. Besides, combining N_2O nitridation and CMP process leads to an optimized *J–E* characteristics of polysilicon oxide.

Fig. 5(a) and (b) display the effective barrier height of different thickness polyoxide at $+Vg$ and $-Vg$ injection. Clear, all CMP samples have a higher ϕ_b than that of non-CMP samples. Furthermore, for both non-CMP-O_2 and non-CMP-N_2O samples, the ϕ_b of polyoxide under $+Vg$ injection (from polyoxide/poly-1 interface) is smaller than that under $-Vg$ injection (from poly-2/polyoxide interface). This difference is due to the rougher surface morphology of polyoxide/poly-1 than that of poly-2/polyoxide interface [16]. However, for the CMP samples, the ϕ_b of polyoxide under $+Vg$ injection is higher than that under $-Vg$ injection. The reverse situation is true for the Non-CMP samples. This finding implies that the polyoxide/poly-1 interface of CMP samples is smoother than that of Non-CMP samples. The local electric field of smooth interface is less than that of rough interface [2], [7], [12]–[16].

This work also investigated the charge trapping characteristics of polyoxide. Fig. 6(a) and (b) show the gate voltage shifts of these four samples under +10 mA $(+Vg)$ and -10 mA $(-Vg)$ constant current stresses. According to these figures, all of the CMP samples had smaller voltage shifts than those of non-CMP samples under both $+Vg$ and $-Vg$ stresses. This phenomenon suggests that CMP samples trapped fewer electrons than those of non-CMP samples. In addition, a rougher polyoxide/polysilicon interface (i.e. non-CMP) apparently leads to a more conducting area and higher local current density, subsequently causing a higher electron trapping. Furthermore, polyoxide grown in N_2O had smaller voltage shifts than that of grown in O_2 for both CMP and non-CMP samples. We believe that this improvement is due to the incorporation of nitrogen at the polyoxide interface [12]–[15].

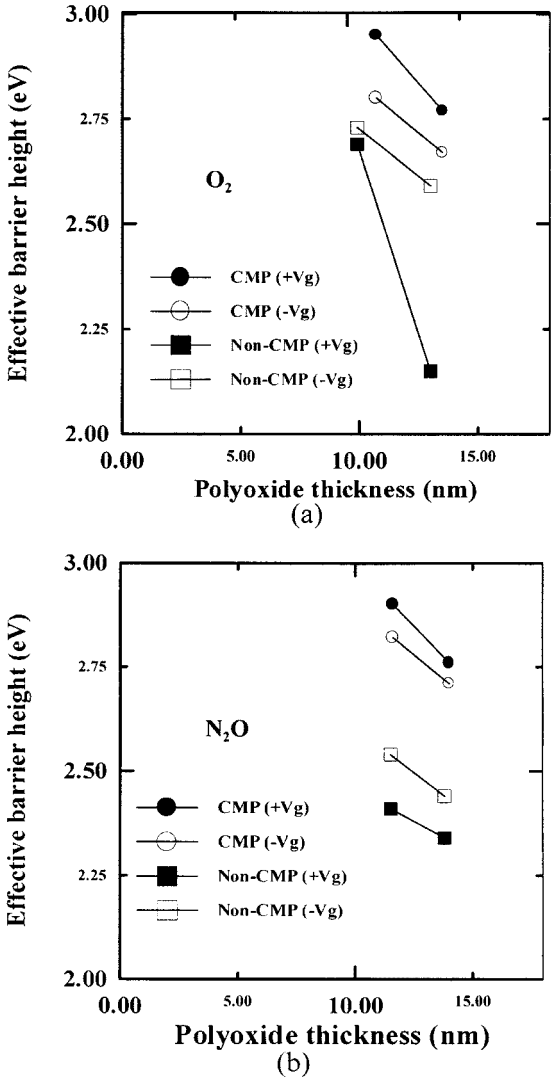

Fig. 5. Effective barrier height (ϕ_b) of polyoxide (a) CMP/non-CMP-O_2, and (b) CMP/non-CMP-N_2O with different thickness.

Fig. 7(a) and (b) illustrates the charge-to-breakdown (Q_{bd}) characteristics of these four samples under $+10$ mA $(+Vg)$ and -10 mA $(-Vg)$ gate injection. According to Fig. 7(a), the non-CMP-N_2O under $+Vg$ gate injection was only slightly better than that of the O_2 sample; it was the same distribution under $-Vg$ gate injection. By using CMP process, the Q_{bd} of oxide grown in N_2O ambient, both under $+Vg$ and $-Vg$ gate injections, were significantly higher than those of O_2 samples, as shown in Fig. 7(b). Notably, the values of the Q_{bd} for CMP samples in Fig. 7(b) are all larger than those counterparts in Fig. 7(a) due to the planar surface by CMP process.

Herein, the centroid of trapped charge (X_t) and trapped charge density (Q_t) in the polyoxide was measured using the bidirectional *I–V* method [8]. Comparing the deviations of Fowler–Nordheim *I–V* characters before and after stresses with both polarities allows us to derive the average location of trapped charges, X_t, and trapped charge density, Q_t, from the following equations:

$$X_t = [\Delta Vg + /(\Delta Vg^+ + \Delta Vg^-)]^* T_{ox} \quad (1)$$

$$Q_t = (\Delta Vg^+ + \Delta Vg^-)^* \varepsilon_{ox}/T_{ox} \quad (2)$$

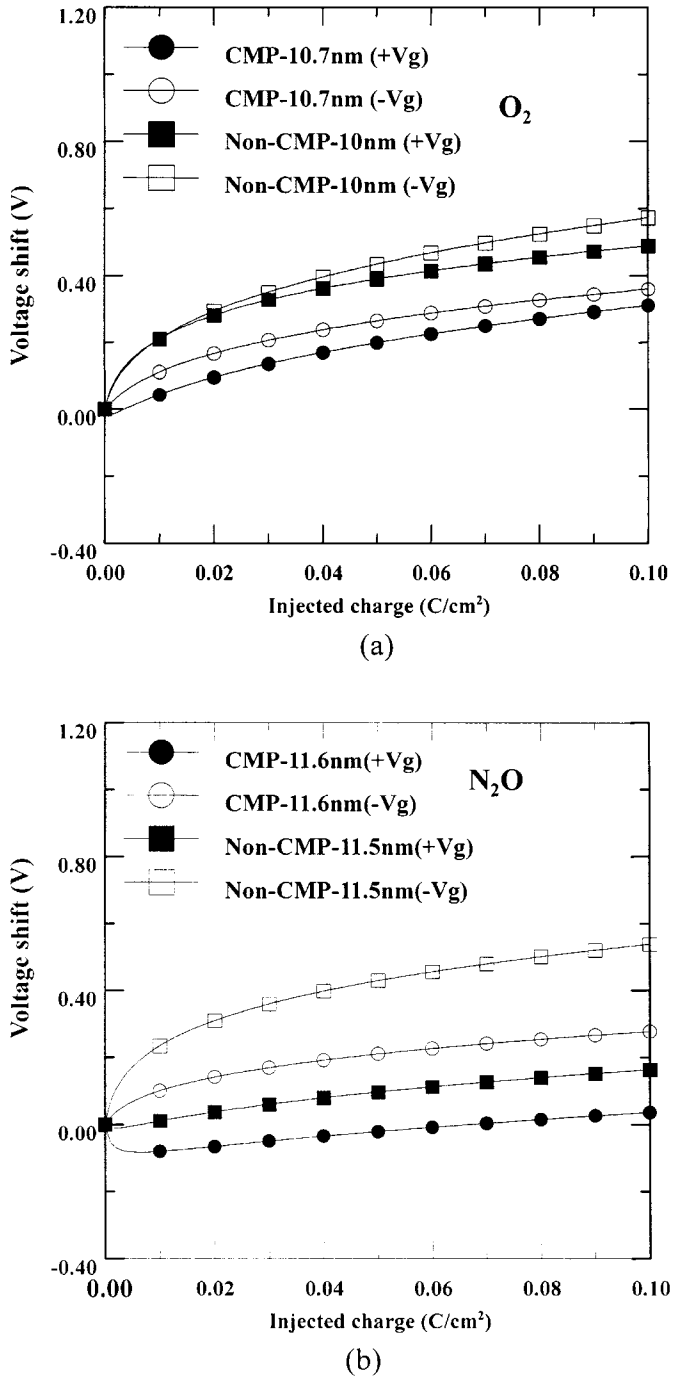

Fig. 6. Charge trapping characteristics under $+Vg$ and $-Vg$ constant current injection of polyoxide (a) CMP/non-CMP-O_2, (b) CMP/non-CMP-N_2O.

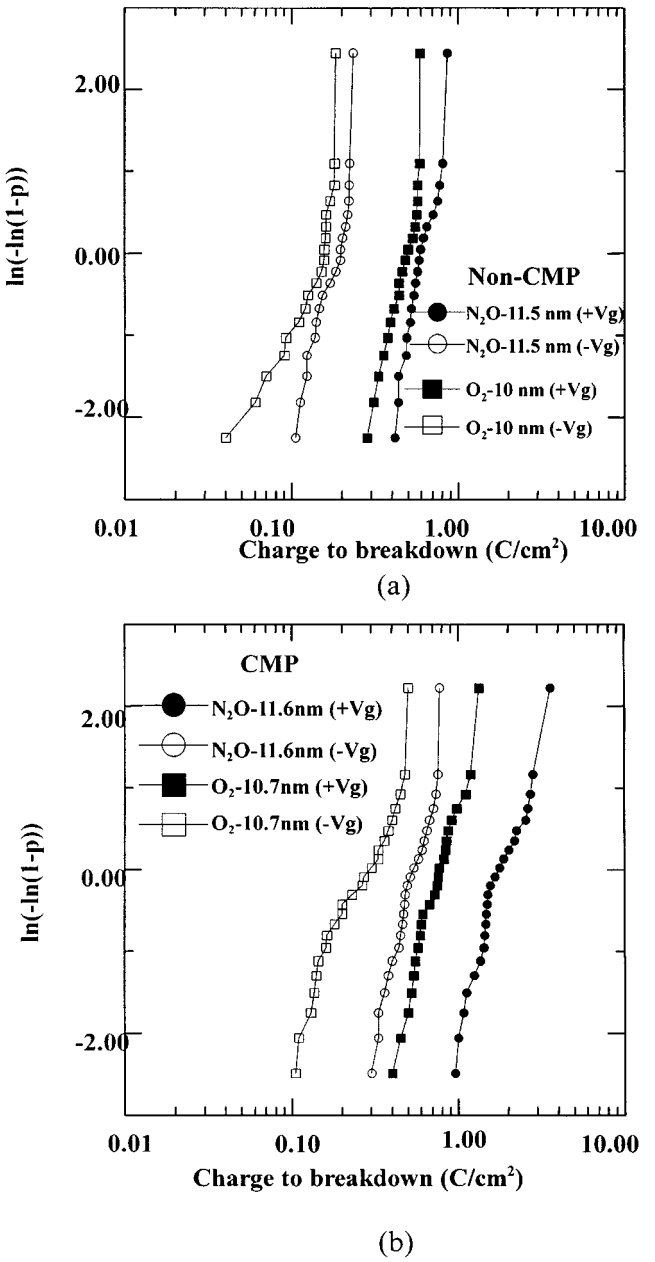

Fig. 7. The charge-to-breakdown (Q_{bd}) characteristics under $+Vg$ (+10 mA) and $-Vg$ (-10 mA) constant current injection of polyoxide (a) non-CMP-O_2/N_2O, and (b) CMP-O_2/N_2O.

where X_t is measured from the poly-2/polyoxide interface; ΔVg^+ denotes the voltage shift when poly-2 is under positive bias; ΔVg^- presents the voltage shift when poly-2 is under negative bias, T_{ox} and ε_{ox} are the thickness of polyoxide and permittivity of the polyoxide, respectively. After the polyoxide capacitors were stressed, the maximum current allowed in the subsequent *I–V* measurement is kept at least an order of magnitude lower than the stress current level in order to avoid the possible re-emission of the trapped charges. In our measurement for trapped centroids, a current density 10 mA/cm^2 was used to stress the polyoxide capacitors and extracted the voltage shift in the current density level of 1 mA/cm^2. Provides for stress times are 20, 50, 100, 200, and 300 s.

Fig. 8(a) and (b) present the centroids of trapping charges (X_t) at various $+Vg$ and $-Vg$ injection times for these four samples. For both N_2O-grown and O_2-grown polyoxides under $+Vg$ and $-Vg$ constant current injection, the X_t of CMP samples are more distant from the injection interface than Non-CMP counterpart, where the electrons were injected from the polyoxide/poly-1 interface under $+Vg$ injection and polyoxide/poly-2 interface under $-Vg$ injection. For N_2O-grown and O_2-grown polyoxides, the effective trapped charges are all negative. Under the constant current injection, the cathode electric field is kept constant and the anode electric field is increased when negative charges are trapped [19]. The

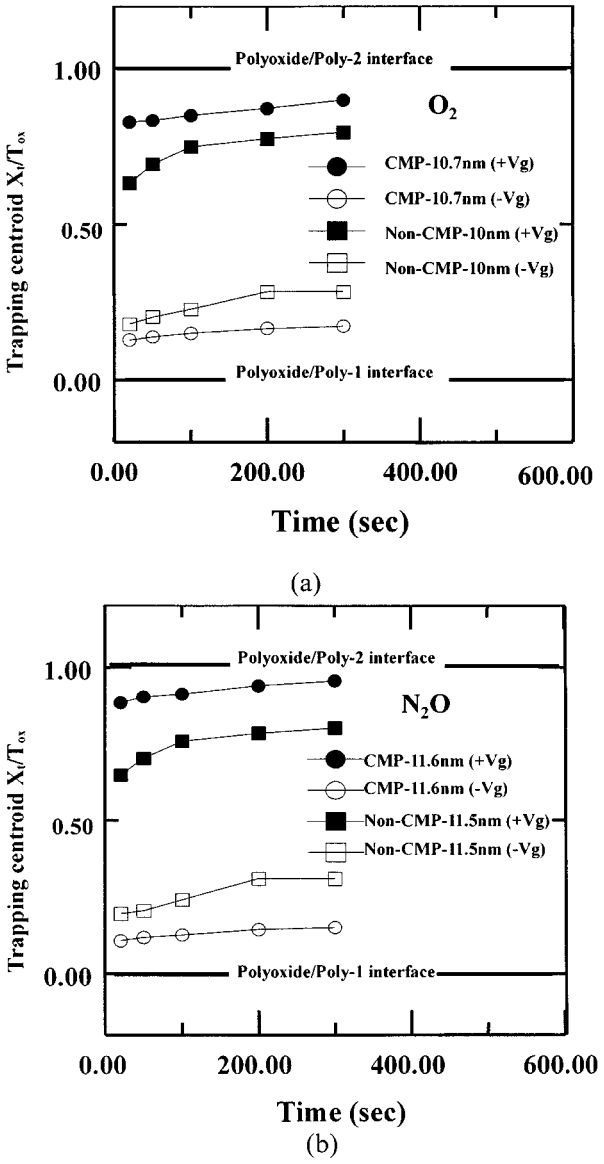

Fig. 8. Centroids of trapping charges (X_t) at various $+Vg$ and $-Vg$ injection times for (a) CMP/non-CMP-O_2 polyoxides, (b) CMP/non-CMP-N_2O polyoxides.

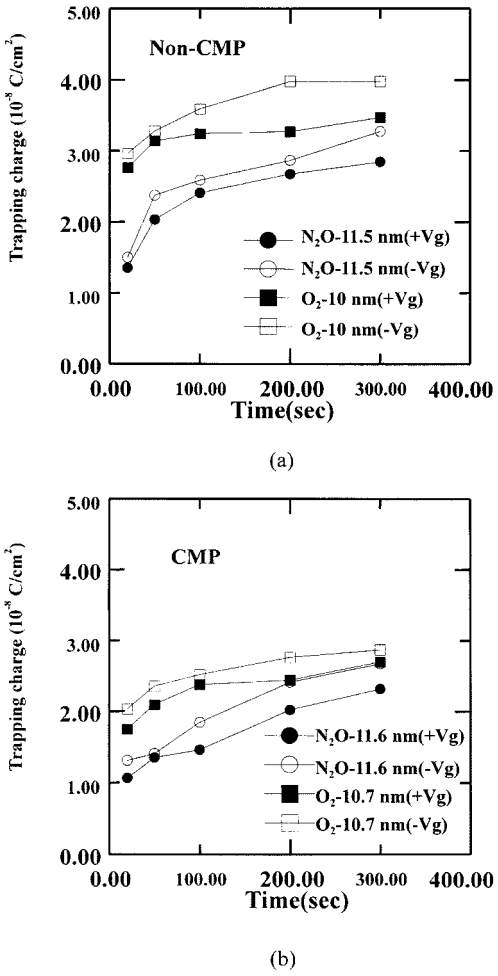

Fig. 9. Trapping-charge densities under $+Vg$ and $-Vg$ constant current injection of polyoxide (a) non-CMP-O_2/N_2O, and (b) CMP-O_2/N_2O.

more charges trapped and the nearest the centroid of trapped is to the cathode, the more the anode electric field is increased [14]. Comparing to the non-CMP samples, CMP samples have lower trapping charges under both $+Vg$ and $-Vg$ injection. This finding implied the smooth interface of CMP samples, therefore, centroids were away from the injection interface [16].

Fig. 9(a) and (b) displays the trapping-charge densities of these four samples under $+Vg$ and $-Vg$ constant current injection. Clearly, for both N_2O-grown and O_2-grown polyoxides, the electron trapping charge density in the CMP samples are less than that in the non-CMP samples under both $+Vg$ and $-Vg$ constant current injection, resulting from the smooth interface by CMP process. Moreover, the electron trapping charge density in the N_2O-grown polyoxide is less than that in the O_2-grown polyoxide for both CMP and non-CMP samples under both $+Vg$ and $-Vg$ constant current injection.

Above results suggest that adding an adequately controlled CMP process not only improves the surface roughness of the poly-1 but also reduces the accumulation of the phosphorous atoms in oxide and in the grain boundary and also improves the incorporate of nitrogen in N_2O ambient. We believe that although incorporating nitrogen at interface can improve the quality of polyoxide, the rough interface and/or high incorporated phosphorous degrade performance for the non-CMP samples under both $+Vg$ and $-Vg$ gate injection. By adding the CMP process, the bumps on the poly-1 surface [1] are removed and a smooth surface can be obtained. This planar surface reduces the accumulation of the phosphorous and improves the incorporation of nitrogen at the interface in N_2O ambient. For both O_2-grown and N_2O-grown polyoxide, CMP samples exhibit a lower leakage current, higher dielectric breakdown field, higher electron barrier height, less electron trapping rate, a much higher charge-to-breakdown (Q_{bd}), and lower density of trapping charge than those of non-CMP samples. Moreover, N_2O-grown polyoxide on the CMP samples has the highest dielectric breakdown field, lowest electron trapping rate, highest charge-to-breakdown, and lowest density of trapping charge. Consequently, combining N_2O nitridation and CMP process leads to an optimized process for polysilicon oxide.

IV. Conclusions

This paper has demonstrated the improved integrity of the polysilicon oxide by using a combination of N_2O nitridation and CMP process. For both O_2-grown and N_2O-grown polyoxide, CMP samples exhibit a lower leakage current, higher dielectric breakdown field, higher electron barrier height, less electron trapping rate, a much higher charge-to-breakdown (Q_{bd}), and lower density of trapping charge than those of Non-CMP samples. For the CMP samples, the electron barrier height (ϕ_b) of polyoxide under $+Vg$ injection is higher than that under $-Vg$ injection which is a reverse situation for non-CMP samples. Moreover, N_2O-grown polyoxide on the CMP samples has the highest dielectric breakdown field, lowest electron trapping rate, highest charge-to-breakdown, and lowest density of trapping charge. Consequently, combining N_2O nitridation and CMP process is a highly promised process for the polysilicon oxide.

References

[1] J. C. Lee and C. Hu, "Polarity asymmetry of oxides grown on polycrystalline silicon," *IEEE Trans. Electron Devices*, vol. 35, p. 1063, July 1988.

[2] L. Faraone, R. D. Vibronek, and J. T. Mcginn, "Characterization of thermally oxidized n^+ polycrystalline silicon," *IEEE Trans. Electron Devices*, vol. ED-32, p. 577, 1985.

[3] S. L. Wu *et al.*, "Investigation of the polarity asymmetry on the electrical characteristics of thin polyoxides grown on N^+ polysilicon," *IEEE Trans. Electron Devices*, vol. 44, p. 153, Jan. 1997.

[4] M. Hendriks and C. Mavero, "Phosphorus doped polysilicon for double poly structures," *J. Electrochem. Soc.*, vol. 138, p. 1466, 1991.

[5] M. C. Jun, Y. S. Kim, and M. K. Han, "Polycrystalline silicon oxidation method improving surface roughness at the oxide/polycrystalline silicon interface," *Appl. Phys. Lett.*, vol. 66, p. 2206, 1995.

[6] P. A. Heimann, S. P. Murarka, and T. T. Sheng, "Electrical conduction and breakdown in oxides of polycrystalline silicon and their correlation with interface texture," *J. Appl. Phys.*, vol. 53, p. 6241, 1982.

[7] L. Faraone and G. Harbeke, "Surface roughness and electrical conduction of oxide/polysilicon interface," *J. Electrochem. Soc.*, vol. 133, p. 1410, 1986.

[8] E. Avni, O. Abramson, Y. Sonnenblick, and J. Shappir, "Charge trapping in oxide grown on polycrystalline silicon layer," *J. Electrochem. Soc.*, vol. 135, p. 182, 1988.

[9] F. C. Jong *et al.*, "Improved flash cell performance by N_2O annealing of interpoly oxide," *IEEE Electron Device Lett.*, vol. 18, p. 343, July 1997.

[10] P. Candelier *et al.*, "Simplified 0.35-μm flash EEPROM process using high-temperature oxide (HTO) deposited by LPCVD as interpoly dielectrics and peripheral transistors gate oxide," *IEEE Electron Device Lett.*, vol. 16, p. 385, Sept. 1995.

[11] J. Kim and S. T. Ahn, "Improvement of the tunnel oxide quality by a low thermal budget dual oxidation for flash memories," *IEEE Electron Device Lett.*, vol. 18, p. 385, Aug. 1997.

[12] C. H. Kao, C. S. Lai, and C. L. Lee, "The TEOS CVD oxide deposited on phosphorus *in situ* doped polysilicon with rapid thermal annealing," *IEEE Trans. Electron Devices*, vol. 44, p. 526, Nov. 1997.

[13] ——, "The TEOS oxide deposisted on phosphorus *in situ*/$POCL_3$ doped polysilicon with rapid thermal annealing in N_2O," *IEEE Trans. Electron Devices*, vol. 45, p. 526, Sept. 1998.

[14] C. S. Lai, T. F. Lei, and C. L. Lee, "The characteristics of polysilicon oxide grown in pure N_2O," *IEEE Trans. Electron Devices*, vol. 43, p. 326, Feb. 1996.

[15] Z. Liu *et al.*, "Effects of N_2O aneal and reoxidation on thermal oxide characteristics," *IEEE Electron Device Lett.*, vol. 13, p. 402, Aug. 1997.

[16] T. F. Lei *et al.*, "Characteristics of polysilicon oxides thermally grown and deposited on the polished polysilicon films," *IEEE Trans. Electron Devices*, vol. 45, p. 912, Apr. 1998.

[17] T. F. Lei, J. H. Chen, M. F. Wang, and T. S. Chao, "Enhancement of integrity of polysilicon oxide by a combination of N_2O nitridation and CMP process," *IEEE Electron Device Lett.*, vol. 20, May 1999.

[18] Y. Mikata, S. Mori, K. Shinada, and T. Usarmi, "Low leakage current poly-silicon oxide grown by two-step oxidation," in *Proc. 1985 IEEE/IRPS*, 1985, p. 32.

[19] I. C. Chen, S. Holland, and C. Hu, "Electrical breakdown in thin gate and tunneling oxide," *IEEE Trans. Electron Devices*, vol. ED-32, p. 413, Feb. 1985.

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