Forward Gated-Diode Measurement of Filled Traps in High-Field Stressed Thin Oxides

Ming-Jer Chen, Ting-Kuo Kang, Huan-Tsung Huang, Chuan-Hsi Liu, Yih J. Chang, and Kuan-Yu Fu

***Abstract*—The forward gated-diode monitoring technique can find its potential applications in assessing the filled traps in MOSFET thin oxides, which are subjected to high-field stressing and then followed by hot-electrons filling scheme. Our measurement of the gate voltage shift associated with the forward current peak produces a power law relation between the filled trap density and the electron stress fluence, indeed in close agreement with that obtained by MOSFET threshold voltage shift.**

***Index Terms*—Gated-diode, hot electron, MOSFET, neutral trap, oxide breakdown, SILC, thin oxide.**

I. Introduction

The high-field Fowler–Nordheim (FN) electron tunneling through thin oxides can produce a variety of defects, among which the most concerned are the neutral electron traps. The principal reasons are that 1) the neutral electron traps can serve as a stepping stone for injected electrons, which gives rise to SILC in low voltage regime [1],[2], and 2) a certain trap density is critically encountered, leading to a breakdown event [3]–[6]. Thus, an essential knowledge of the total neutral trap density N_T created for imposed electron fluence Q_e is crucial to the study of SILC and oxide breakdown. To achieve this goal, Degraeve *et al.* [7], [8] have recently performed two independent experiments while introducing a key physical parameter, namely, filling or occupied fraction p [9], to connect the two. The first experiment is the hot-electrons filling scheme following the high-field stress. This scheme via a back-gate reverse bias can offer hot substrate electrons to climb over the Si/SiO_2 barrier height and fill the neutral traps within the oxide. Measurement of a saturation level in threshold voltage shift can be directly linked to the filled trap density N_{ox}, systematically leading to a power law relation [7], [8]: $N_{ox} \propto Q_e^{0.56\sim0.6}$. The second is the sphere-based Monte Carlo percolation simulation experiment treating N_T as well as its statistics. p is N_{ox} divided by N_T [9] and can be estimated by subsequently fitting intrinsic charge-to-breakdown data in the manufacturing processes [7], [8], [10], [11].

On the other hand, for MOSFET's biased in a reverse gated-diode mode [12], measurement of the reverse current I_r versus gate voltage from accumulation through depletion to inversion can provide information concerning interface states and/or oxide traps. This mode is usually insensitive to oxides having small areas as in miniaturized devices, and the large-area oxides are inevitably required. The same information can be substantially maintained for switching to the forward mode as reflected by a well-defined relation $I_f = I_r \exp(qV_f/2KT)$ [12], where I_f is the forward current measured at a forward bias V_f. Thus, operating in forward mode can not only make the gated-diode monitoring exponentially sensitive but also allow use of small-area oxides. Indeed, the forward gated-diode configuration formed on the stressed MOSFET's has exhibited these abilities [13]–[15]. This work is to extend such sensitive technique to the case of thin oxides that are subjected to FN tunneling stress and then followed by hot-electrons filling scheme. The ultimate objective is to build a power law relation between N_{ox} and Q_e as that in [7], [8].

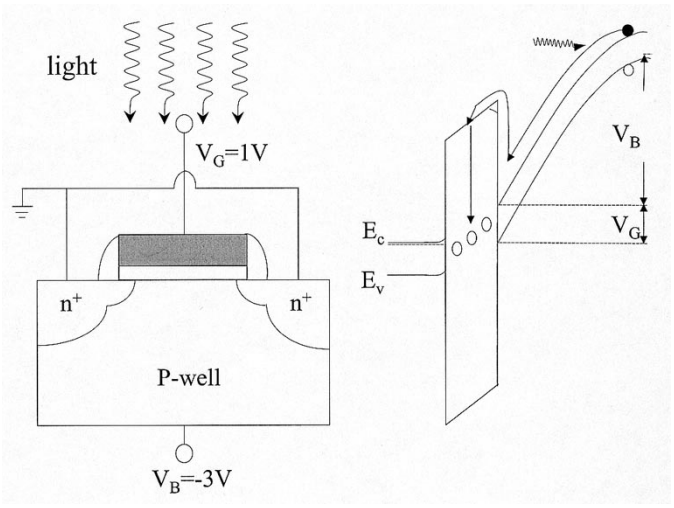

Fig. 1. Experimental setup and energy band diagram to schematically demonstrate the optically induced hot-electrons filling scheme.

II. Experimental

The n-channel MOSFET's under study had the gate width-to-length ratio of 20 μm/ 0.3 μm and the gate oxide thickness of 7 nm. The FN tunneling stress condition was carried out at the oxide field strength E_{ox} of 9.9 MV/cm with the source, drain, and substrate tied to ground, then followed by the optically induced hot- electrons filling scheme [16]. Fig. 1 shows schematically this scheme in terms of 1) the photogeneration technique via a tungsten lamp to produce electron seed in substrate, and 2) a negative back-gate bias of -3 V to make substrate electrons hot such as to surmount the Si/SiO_2 barrier height and fill the traps. During measuring the gated-diode forward current in the drain, the drain was connected to -0.2 V bias, the substrate was tied to ground, and the source was kept open.

Fig. 2 plots the measured forward current versus gate voltage for $Q_e = 0.22$ C/cm^2 with filling or illumination time as parameter. It can be observed that the current peak in depletion region shifts toward the positive gate voltage for increasing illumination time and gradually tends to saturate. Fig. 3 shows the corresponding voltage shift ΔV_G associated with the current peak versus illumination time. Detrapping and Coulombic repulsion [9], which limit only part of the neutral traps available for filling, are responsible for the saturating behavior in Fig. 3. Assuming that the occupied traps are distributed uniformly within the oxide as adopted elsewhere [7], [8], [16], the saturated voltage shift $\Delta V_{G(sat)}$ can be directly linked to the filled trap density through $\Delta V_{G(sat)} = qt_{ox}^2 N_{ox}/2\varepsilon_{ox}$ where t_{ox} is the oxide thickness and ε_{ox} is the oxide permittivity. The resulting N_{ox} for different Q_e is depicted in the inset of Fig. 3, showing a power law relation

$$N_{ox} = \eta Q_e^{0.5} \tag{1}$$

where $\eta = 1.62 \times 10^{18}$ cm$^{-2}C^{-0.5}$ for N_{ox} in 1/cm^3 and Q_e in C/cm^2. The carrier separation technique has measured the substrate hole current, yielding hole generation coefficient of 6.8×10^{-4} at the same stress field E_{ox} of 9.9 MV/cm. Thus, we have $N_{ox} = 6.21 \times$

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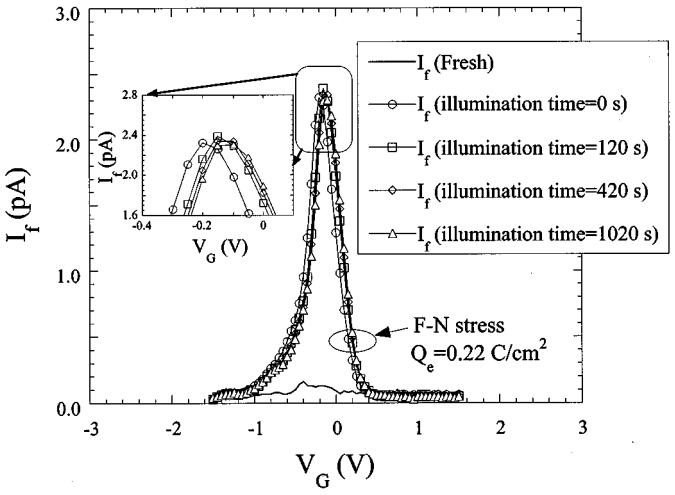

Fig. 2. Measured forward gated-diode current versus gate voltage from one n-MOSFET sample. The gate oxide area was 3 μm^2. For the selected illumination time following Q_e of 0.22 C/cm^2, the filling scheme was interrupted and the test setup was switched to the forward gated-diode configuration. The *I–V* near the current peak is magnified for clear viewing.

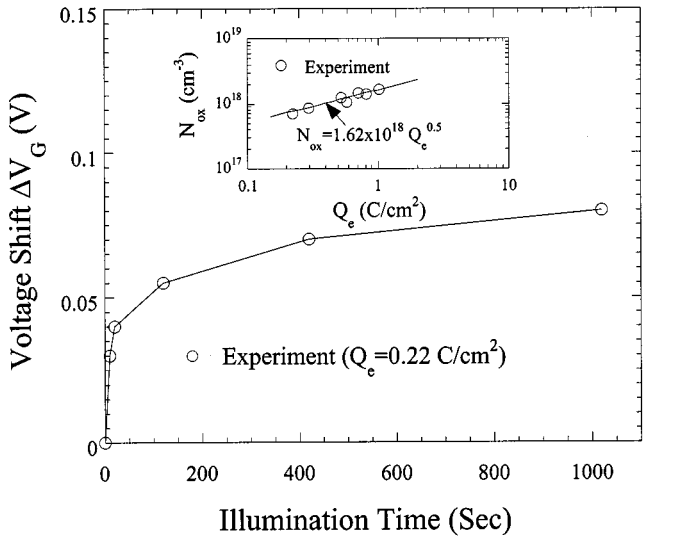

Fig. 3. Gate voltage shift versus illumination time corresponding to Fig. 2. The inset shows the estimated trap density N_{ox} versus Q_e from seven n-MOSFET samples. Each sample represents a specific Q_e. A power law relation is drawn by best fitting data points.

$10^{19}Q_p^{0.5}$ for hole fluence Q_p in C/cm^2, which is quite close to the published expression $N_{ox} = 5.3 \times 10^{19}Q_p^{0.56}$ [7], [8] with respect to the power exponent and the prefactor.

The above hot-electrons filling scheme has also been performed on the fresh devices, evidencing no noticeable voltage shift in the measured forward current versus gate voltage before and after the scheme. This means that no extra neutral traps can be generated *singly* due to filling action. Additionally, Fig. 2 clearly reveals that the current peaks for different illumination times following FN stress (including the zero illumination time) are almost unchanged, indicating that no significant interface states can be created under the influence of the illumination induced hot electrons.

III. Conclusion

The forward gated-diode technique has demonstrated its new merit of producing a power law relation between the filled trap density and the electron stress fluence. This relationship is found to agree closely with that obtained by MOSFET threshold voltage shift.

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