Robust Ultrathin Oxynitride Dielectrics by NH_3 Nitridation and N_2O RTA Treatment

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***Abstract*—In this paper, a method to grow robust ultrathin ($E_{OT} = 28$ Å) oxynitride film with effective dielectric constant of 5.7 is proposed. Samples, nitridized by NH_3 with additional N_2O annealing, show excellent electrical properties in terms of very low bulk trap density, low trap generation rate, and high endurance in stressing. This novel dielectric appears to be very promising for future ULSI devices.**

***Index Terms*—EEPROM, flash memory, NH_3, N_2O, oxynitride, RTA.**

I. Introduction

THE CONTINUOUS scaling of thermal SiO_2 as the gate dielectric has run into difficulties, where high leakage currents are inevitable due to direct tunneling when oxide thickness is less than 25 Å [1]. Recently, ultra-thin silicon nitride gate dielectrics are proposed to replace the conventional oxide to meet the need for increased capacitance and while maintain a low gate leakage. Moreover, in EEPROM and flash memory devices, the thickness of the tunnel oxide is limited by the stress-induced-leakage-current (SILC) after many write/erase (WE) cycles. Ultrathin nitride or oxynitride films [2]–[4] have been reported with good performance in SILC. Hence, it becomes the most promising candidate to replace thermal SiO_2 film as the tunneling dielectric to improve WE endurance. However, the Si_3N_4/Si interface is not yet as good as the SiO_2/Si interface and the density of interface defects is also relatively high. An additional N_2O treatment can reduce this interface state and bulk trap densities [5]. In this paper, an ultrathin oxynitride is grown by nitridizing the silicon substrate in NH_3 and with an additional N_2O treatment is proposed. Excellent electrical and reliability characteristics are found for this oxynitride film.

II. Experimental

Samples were fabricated on 4-in p-type (100)-oriented silicon wafers with resistivity of 14–21 Ω-cm. All the wafers were first cleaned by standard RCA clean method. A 15 Å Si_3N_4 film was first grown by NH_3 (flow rate is 105 sccm, pressure is 500 mtorr) nitridation of the Si substrate in LPCVD system at 850 °C for 1 h. All samples were immediately annealed in a N_2O rapid thermal annealing (RTA) treatment at 800, 900, and 1000 °C, respectively. Polycrystalline Si films with a thickness of 3000 Åwere deposited by LPCVD. The poly-Si film was doped with $POCl_3$ at 900 °C for 30 min. A 5000 Å Al film was deposited on the wafer by a thermal coater. The gate of metal-oxide-semiconductor (MOS) capacitor was defined by lithography, and then Al and poly-Si films were etched by wet etch chemistry. A 5000 Å Al film was also deposited on backside of wafers after stripping the oxide on the backside. Finally, all the samples were sintered at 400 °C for 30 min in an N_2 ambient to form a good ohmic contact. The gate dielectrics of MOS capacitors with area of 10^{-4} cm^2 were measured. The thickness of ultrathin Si_3N_4 film was determined by using spectroscopic ellipsometer. The equivalent oxide thickness (E_{OT}) was calculated by high frequency capacitance–voltage (C–V) of 0.1 MHz at operating range of $-3 \sim 2$ V in strong accumulation region without considering quantum mechanical effects. The physical thickness was doubly checked by TEM to obtain the dielectric constant. The electrical properties and reliability characteristics of MOS capacitors were measured by using the Hewlett-Packard (HP) 4156B semiconductor parameter analyzer.

III. Results and Discussion

The resultant equivalent oxide thickness (E_{OT}) of oxynitride film for a 15 Å nitride annealed in a N_2O ambient at 800, 900, and 1000 °C is 28, 31, and 33 Å, respectively. The thickness of oxynitride film increases as the RTA temperature increases. Physical thickness of 800 °C sample measured by TEM (not shown) is 40 Å. The effective dielectric constant of 5.7 was obtained for this sample. Fig. 1 shows J–V characteristics for pure thermal oxide and these samples after treatment at different RTA temperature. It is found that samples with $E_{OT} = 28$ Å (annealed at lowest temperature of 800 °C) shows a lower leakage current than pure thermal oxide with $T_{OX} = 29$ Å and exhibits the lowest leakage current at voltage of $0 \sim 1$ V among three samples. This leakage increases as the RTA temperature increases even with a thicker $E_{OT} = 31$ Å for 900 °C sample or 33 Å for 1000 °C sample. This result can be attributed to the fact that more positive trapped charges are generated due to more nitrogen incorporation at high temperature annealing in N_2O ambient [6], [7]. These positive charges will assist tunneling in the low field.

Fig. 2 shows the quasistatic and high frequency of C–V curves for the sample with $E_{OT} = 28$ Å. The interface state density of this sample was deduced as low as 6×10^{10} eV^{-1} cm^{-2}. This implies that Si_3N_4 film annealed at 800 °C in N_2O gas by using RTA system can produce a good interface

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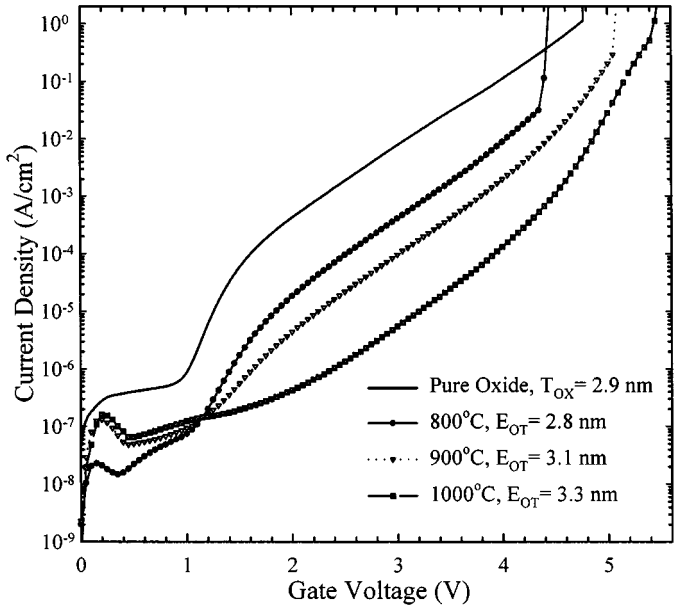

Fig. 1. J–V characteristics of pure thermal oxide and 15 Å Si_3N_4 films annealed at various temperature.

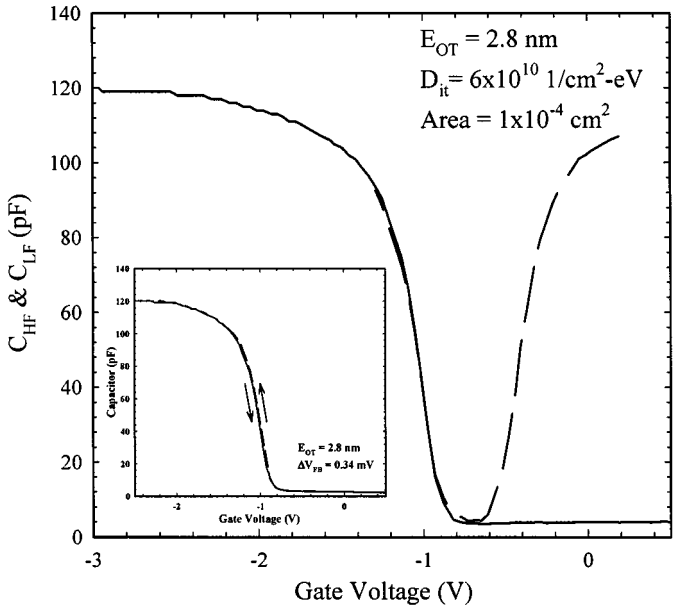

Fig. 2. Quasistatic and high frequency of C–V curves and inset shows hysteresis curves of a 15 Å Si_3N_4 film annealed at 800 °C.

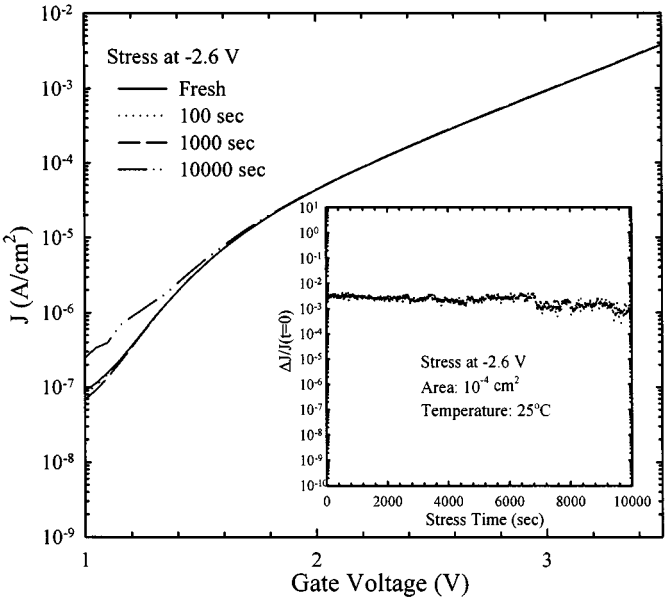

Fig. 3. SILC under constant voltage stress and inset shows $\Delta J/J(t = 0)$ versus stress time plots of a 15 Å Si_3N_4 film annealed at 800 °C.

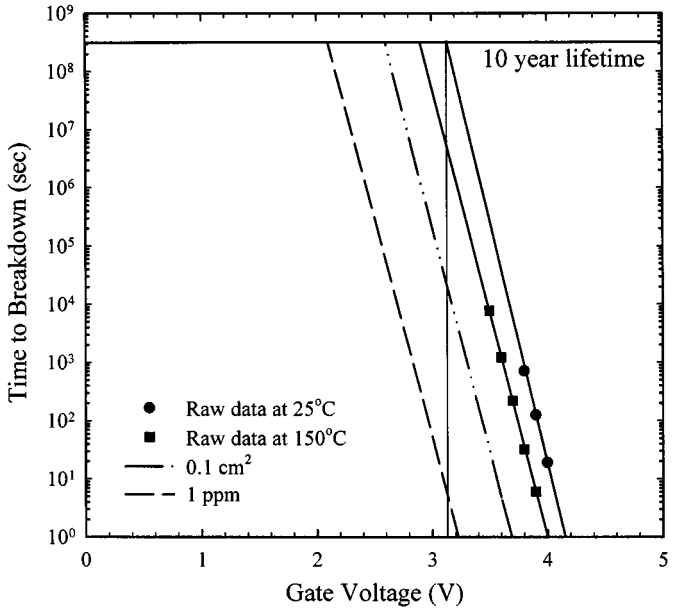

Fig. 4. Illustration of loss in the maximum operating voltage by temperature acceleration, scaling to effective area, and calculation of 1 ppm failures for 15 Å Si_3N_4 film annealed at 800 °C.

quality. Hysteresis of the high-frequency C–V characteristics of this oxynitride film was shown in the insert by the amount of flat-band voltage shift between opposite sweep directions. Negligible amount of hysteresis ($\Delta V_{\rm FB} = 0.34$ mV) is observed, indicating very low bulk or interface trap densities in the film. Fig. 3 shows the result after constant voltage stress at -2.6 V for sample with $E_{\rm OT}$ =28 Å annealed at 800 °C. No significant SILC was observed after 10 000-s stressing. In the insert, the sample after 10 000-s stressing shows gate current ($\Delta J/J(t = 0)$, where $\Delta J = [J(t) - J(t = 0)]$) for constant voltage stressing. In Fig. 4 the cumulative impact of area scaling, 1 ppm failure rate, and temperature acceleration in ten years is evaluated [8], [9]. For $E_{\rm OT}$ =28 Å annealed at 800 °C, figures drawn well fit to the measured time-to-breakdown ($T_{\rm BD}$) at room temperature and 150 °C. The area scaling is calculated by assuming a Weibull distribution (63% value) with a random distribution of breakdown sites [10]. The 150 °C-data have been a scaling of 10^{-4} cm^2 to 0.1 cm^2, and finally the 1 ppm-line was calculated from the 150 °C-data. The maximum operating voltage could be as high as 2.1 V in these conditions.

Although this oxynitride with $E_{\rm OT}$ of 28 Å has demonstrated, ultrathin $E_{\rm OT}$ dielectric films should be developed. The oxynitride with $E_{\rm OT}$ of 15 Å or less can be also achieved by reducing the temperature and/or time of NH_3 nitridation or using diluted N_2O RTA annealing process.

IV. Conclusion

In this letter, we reported a very promising method to obtain a robust ultra-thin oxynitride by NH_3 nitridation and with a N_2O RTA treatment. This oxynitride film exhibits excellent reliability properties in terms of low leakage currents, low interface state density and high reliability during stressing. This novel dielectric appears to be very promising for future ULSI devices.

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