standards (e.g. 15kHz in the IS-54) in a multi-standard receiver. Also, we have utilised this property to achieve the design of a fully integrated 60Hz notch filter. The filter is based on the circuit of Fig. 2a and requires a relatively small total capacitance of 100pF and a total resistance of 420kΩ.

Applications and simulation results: The lowpass filter of the circuit shown in Fig. 2a is designed to be used for implementing the channel-select filter in the baseband chain of a multi-standard direct conversion wireless receiver. A fourth-order channel-select filter was implemented by cascading two of the filters in Fig. 2a. The filter is designed to accommodate the following wireless standards: IS-54, GSM, IS-95, and WCDMA with bandwidths of 15kHz, 10kHz, 700kHz and 2.1MHz, respectively. Digital tuning provided by 8bit R-2R ladders is used to precisely select the desired channel within each standard while four different capacitors were used to switch between the different standards. Moreover, the bandpass filter of the circuit in Fig. 2b is shown to be an excellent candidate for use as a baseband filter in a frequency-hopping receiver with a low IF centre frequency of 3MHz, as is the case in bluetooth receivers [5]. Low power fully differential versions of both filters were submitted for fabrication in a 1.2μm standard CMOS technology available through MOSIS. Simulation results obtained from the extracted files of the filters agree very well with the theory presented. The supply voltages were set to ±1.5V and the standby current was 950μA for the fourth-order lowpass filter and 550μA for the bandpass filter. Simulation results of the fourth-order channel-select filter covering all four wireless standards are shown in Fig. 3. Also, it has been found that the centre frequency of the bandpass filter can be tuned by > 100% in steps of < 0.5%.

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Effect of coplanar probe pad design on noise figures of 0.35 μm MOSFETs

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The effects of different coplanar ground-signal-ground (GSG) probe pads on the noise figure characteristics of submicron MOSFETs are presented. Devices with top-level metal as probe pads shielded by grounded bottom-level metal possess the most appropriate probe pad structure for characterising the noise performance of MOSFETs. Equivalent circuits of the probe pads are used to explain the different noise behaviours.

Introduction: With the dramatic advancement in Si VLSI technologies, on-chip silicon radio frequency integrated circuits (RFIC) have recently emerged as attractive candidates for use in rapidly

growing wireless communication applications [1 – 3]. The successful design of Si RFICs requires accurate device parameters. One approach has been to use HP8510C and Cascade coplanar probe technology to measure the on-wafer S-parameters. However, parasitics, including the effects of probing pads, connections and substrate resistance, greatly influence the measured device characteristics, and need to be de-embedded using a correction procedure [4].

Experiments: A commercial CMOS technology with triple metal interconnects was used to fabricate 0.35μm NMOSFETs. The two-port S-parameters of the MOSFETs and open dummy devices were measured using an HP85122A modelling system and Cascade Microtech coplanar GSG probes. The noise figures were characterised by an ATN NP5B noise measurement system. Open dummy devices with different GSG probe pads were used to de-embed the pad parasitic and determine the intrinsic S-parameters and noise performance. The lump elements of the equivalent models of the GSG probe pads were then extracted and used to explain the different noise characteristics of the devices.
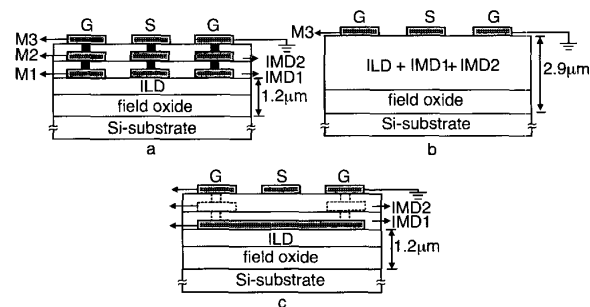

Fig. 1 *Cross-section diagrams of coplanar GSG probe pads with different structures*

a Metal 1 GSG probe pads
b Metal 3 GSG probe pads
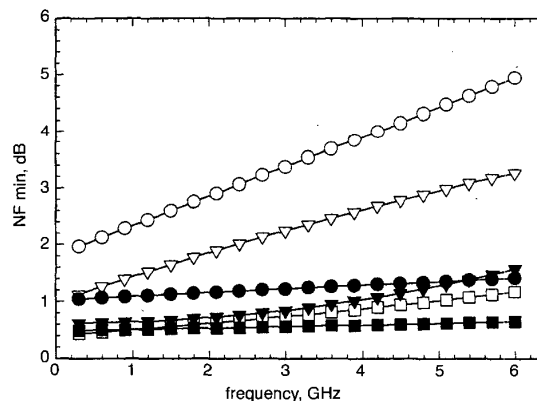*c* Metal 3 GSG probe pads with grounded metal 1 layer

Fig. 2 *Noise figures of MOSFETs before and after de-embedding with different GSG probe pad structures as a function of frequency*

$W = 120μm$, Finger = 10, $V_d = 2V$, $V_g = 1V$
○ device A
▽ device B
□ device C
● device A, de-embedded
▼ device B, de-embedded
■ device C, de-embedded

Results and discussion: Figs. 1a, b and c show the cross-sections of the devices with the coplanar GSG probe pads on metal 1, metal 3 and metal 3 with grounded metal 1 shielding, respectively. The cross-section was obtained by cutting along the GSG pads. For convenience, the devices in Figs. 1a, b and c are denoted by device A, B, and C. Fig. 2 demonstrates both noise figures (NFs) of the MOSFETs with different GSG probe pads before and after noise de-embedding. Before noise de-embedding, device A shows the

largest noise figure and much stronger frequency dependence, while device C shows the smallest NF and slight frequency dependence. There was a great improvement in the noise figure of the device when metal 1 grounded shielding was used. The results are similar to those of BJTs [5]. After the probe pad parasitics were de-embedded, the NFs of the three devices improved and became much closer to that of other devices. The dependence of the NFs on frequency also decreased especially for device C. The small difference between the de-embedded NFs is presumably caused by imperfect de-embedding. This requires further study of the de-embedding procedures [6 – 8]. The NFs of devices A, B and C before de-embedding at 2.4 GHz were 3.1, 2.0 and 0.7dB, and those after de-embedding were 1.2, 0.8 and 0.5dB, respectively. Device C exhibited the best noise performance and the smallest difference in NF before and after de-embedding. The results also demonstrate that device C, metal 3 with grounded metal 1 shielding, has the most appropriate pad structure for obtaining the intrinsic noise figure characteristics of MOSFETs. Moreover, the intrinsic NF of a MOSFET having the same pad structure as device C can be approximately obtained without any de-embedding procedure as the frequency is < 3GHz.
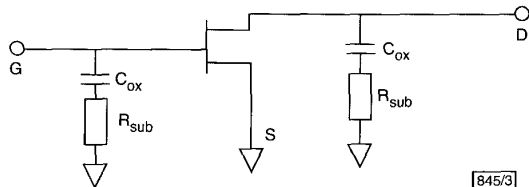

Fig. 3 *Equivalent circuit model of MOSFET with GSG probe pads*

To explain the different NF behaviours before de-embedding the pad parasitics, we used parasitic equivalent circuits of the dummy GSG probe pads, similar to those of [9]. Fig. 3 shows a simplified equivalent model of the MOSFET with GSG probe pads and Table 1 the extracted equivalent circuit parameters, parasitic oxide capacitance (C_{ox}) and parasitic substrate resistance (R_{sub}). The value of R_{sub} falls from 244.8Ω in the case of device B to 11.8Ω in the case of device C, and are lightly dependent on the frequency because a certain amount of parasitic substrate capacitance (C_{sub}) neglected in Fig. 3 exists in the substrate. Since the noise characteristics relate to the resistive impedance, we believe that a reduction in the value of R_{sub} for device C results in an improvement in the noise performance and makes the least difference before and after de-embedding.

Table 1: Extracted equivalent circuit parameters

Device	A	B	C
C_{ox} [fF]	192	78.8	138.3
R_{sub} [Ω]	234.8	244.8	11.8

Conclusions: The effect of substrate parasitic resistance on the noise figure performance of MOSFETs has been evaluated by measuring the noise figures of devices with different coplanar GSG probe pad structures. The equivalent parasitic circuit models of the different GSG probe pads were proposed. The improvement in the noise figure of a device with grounded metal 1 shielding is probably be due to the reduction in the parasitic substrate resistance. The top level metal used in modern deep submicron CMOS technology is recommended for realising the GSG probe pads and bottom level metal as the grounded shielding to obtain the best noise figure performance.

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Light-sensitive CMOS ring oscillator

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A simple light-sensitive CMOS ring oscillator, the oscillation frequency of which depends on the chip ambient illumination, is presented. An experimental 21-stage ring oscillator fabricated in 0.5µm CMOS changes the pulse frequency from 50Hz in total darkness to 2MHz in extreme bright ambient at $V_{dd} = 1$V.

Introduction: A standard CMOS ring oscillator (RO) consists of a self-oscillating chain of odd number inverters connected in a feedback loop. As a voltage-controlled oscillator, it is commonly used for analysing CMOS gate dynamic characteristics [1]. Recently, Boyle *at al.* proposed a modified current-controlled RO circuit operating as on-chip temperature sensor [2].

In this letter, we describe a light-sensitive RO circuit the oscillation frequency of which depends on the average ambient illumination.

Circuit description: An electrical schematic diagram of the novel light-sensitive inverter forming the RO chain is shown in Fig. 1. Two P^+/N_{well} photodiodes (PDs) control the charging and the discharging time of the input gate capacitance of both the PMOSTs and MMOSTs. For instance, when the input voltage is high, the PMOST is quickly turned off by the forward-biased PD D_1. The charging time of the NMOST gate is much longer, since it is controlled by the D_2 inverse leakage current $I_r = I_{dark} + I_{photo}$, where I_{dark} is the diode dark current and I_{photo} is the light generated photo-current. As a consequence, the PMOST is turned off before the NMOST gate potential achieves the threshold voltage V_{th}.