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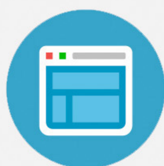

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Evaluation of *in situ* formed W–Ti and $MoSi_2$ as a diffusion barrier to Al for $CoSi_2$ silicided contact

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A simple metallization process to form a shallow $CoSi_2$ silicided contact and W–Ti diffusion barrier simultaneously has been developed. The process starts with depositions of a Co–Ti alloy layer and an overlying W layer on silicon wafers using a dual e-beam evaporation system; this is followed by a single-step annealing treatment in a normal flowing-nitrogen furnace. On the other hand, bilayer self-aligned shallow $MoSi_2/CoSi_2/Si$ silicided contact can be derived from the W/Co–Mo/Si system by a two-step annealing treatment performed in the same environment. I–V characteristics for silicided p^+n diodes with the diffusion barriers formed *in situ* were measured after they had been finished with Al deposition and post-Al annealing at temperatures from 350 to 600 °C in N_2. For comparison, $Al/CoSi_2/p^+n$ and Al/p^+n structures were also investigated. It turns out that the integrity of $Al/W\text{–}Ti/CoSi_2/p^+n$ and $Al/MoSi_2/CoSi_2/p^+n$ silicided contacts can be preserved up to 550 and 500 °C, respectively, for a 20 min annealing, while that of $Al/CoSi_2/p^+n$ can be kept only up to 450 °C.

I. INTRODUCTION

Metal silicides are necessary for the gates, interconnects, and source/drain contacts in scaled-down very large scale integration (VLSI) to reduce series resistance and contact resistance.[1] Among the metal silicides, cobalt disilicide ($CoSi_2$) has many merits and has been under intensive study.[2–5] The merits of $CoSi_2$ include low resistivity (15–20 $\mu\Omega$ cm), high eutectic temperature (1195 °C), low formation temperature, and easy epitaxial silicide growth on silicon.[6,7] Furthermore, cobalt is inert to nitrogen in which Co–silicide is formed. However, $CoSi_2$ still has its exclusive drawbacks, such as a liability to form cobalt oxide when Co on silicon is annealed in a conventional flowing-nitrogen furnace, reaction between $CoSi_2$ and aluminum at a low temperature of 400 °C,[8] and larger volume consumption of Si substrate (3.64 Å of Si per Å of Co when $CoSi_2$ is formed).[9] The trouble with the oxidation of Co in flowing nitrogen can be overcome by applying a passivating film of molybdenum or tungsten over the Co film, which is to be silicidized,[10] or by appropriate control of wafers loading into furnace, annealing temperature, and the thickness of Co film.[11]

The problems pertinent to some silicides, which consume a larger amount of Si substrate and react with Al at a lower temperature, can be solved at the same time by a two-metal alloy scheme.[12] The two-metal alloy is usually composed of a noble (or near noble) metal and a refractory metal. Due to the layered phase separation and the different silicidation temperature of the two metals, reaction between silicon and the alloy leads to formation of the noble-metal silicide on Si substrate and accumulation of the refractory metal at the top. The amount of silicon consumed can be controlled by varying the composition of the alloy and limiting the reaction temperature so that only a certain amount of noble-metal silicide is formed. On the other hand, the refractory metal can act as a diffusion barrier between the silicide and aluminum, which is used to connect the device outwards. In this scheme, however, all the annealings were performed in vacuum or in purified He system,[13–17] which is not practical.

In this work, practical schemes to overcome or relieve the above-mentioned problems simultaneously with resort to metallization of the W/Co–Ti/Si[18] and W/Co–Mo/Si[19] systems will be outlined first. Surely, the heat treatments are performed in conventional flowing-nitrogen (N_2) furnace. During annealing of the W/Co–Ti/Si system, all the Ti is segregated into the overlying W film to form W–Ti alloy, while all the Co in the alloy is segregated to the Si substrate to form $CoSi_2$ contact. The W–Ti formed *in situ* is found to be more stable than a pure refractory metal like tungsten with regard to resistance to oxidation in N_2 furnace at high temperature. Furthermore, W–Ti is a conventional diffusion barrier between aluminum and silicon.[20] On the other hand, during silicidation of the W/Co–Mo/Si system, the overlying W not only passivates the Co–Mo from being oxidized but also consumes some Co from the alloy. Shallow contact is also feasible by etching away the W–Co alloy before further annealing at a higher temperature to form the bilayer silicided contact of $MoSi_2/CoSi_2/Si$. The $MoSi_2$ formed *in situ* can act as a diffusion barrier between $CoSi_2$ and Al since it reacts with Al at a higher temperature of 530 °C.[8]

The evaluation of the W–Ti and $MoSi_2$ formed *in situ* as diffusion barriers will be performed by I–V characteristics measurements on $Al/W\text{–}Ti/CoSi_2/p^+n$ and $Al/MoSi_2/CoSi_2/p^+n$ diodes after post-Al annealing. Diodes of $Al/CoSi_2/p^+n$ without any diffusion barrier and of Al/p^+n (Al directly in contact with Si) are also tested for comparison. On the other hand, Auger electron spectroscopy (AES), scanning electron microscopy (SEM), sheet resistance measurement, and visual inspection are also

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used to confirm the failure mechanism for each diode's structure involved.

II. EXPERIMENTAL

All the metals were deposited using a dual electron-beam evaporation system on *p*-type (100)Si wafers with resistivity of 4–11 Ω cm. After finishing with all the cleaning steps, the wafers were dipped in 20:1 HF for 10 s, then rinsed in de-ionized water for 1 min and kept in methanol before being loaded into the film deposition system. The base pressure was 4.0×10^{-6} Torr prior to the metal depositions on Si wafers placed on cold substrate holders. Deposition of the Co–Mo or Co–Ti alloy was carried out using two independent e-beam guns to evaporate each metal simultaneously at the desired rates. Second layer of metal (tungsten) was deposited without breaking the vacuum. Rutherford backscattering spectrometry (RBS) was used to determine the atomic composition of the as-deposited alloys. W(400 Å)/$Co_{55}Mo_{45}$(540 Å) and W(400 Å)/$Co_{63}Ti_{37}$(370 Å) were deposited on the Si substrates, which were then annealed in normal flowing-nitrogen furnace to form $MoSi_2/CoSi_2$/Si and W–Ti/$CoSi_2$/Si, respectively. In addition, Mo(400 Å)/Co(380 Å)/Si was used to form $CoSi_2$/Si silicided contacts for comparison. Detailed silicidation processes for the different systems will be described in Sec. III A.

Aluminum of 7500 Å in thickness was then deposited on the silicided p^+n diodes for *I–V* characteristics measurement, while aluminum of 3000 Å in thickness was deposited on the blank silicided contacts for study of failure mechanisms by AES depth profiling, SEM, sheet resistance measurement, and visual inspection. Post-Al annealing was performed at temperatures from 350 to 600 °C in N_2.

III. RESULTS AND DISCUSSION

A. Formation of W-Ti/$CoSi_2$/Si, $MoSi_2$/$CoSi_2$/Si, and $CoSi_2$/Si contacts

Simultaneous formation of W–Ti diffusion barrier and shallow $CoSi_2$ silicided contact was derived from the W/Co–Ti/Si system via a single-step annealing at 760 °C for 30 min. The AES depth profile in Fig. 1 shows that the Co in the alloy was entirely segregated to form Co–silicide in contact with Si substrate, while the Ti was segregated into the overlying W layer to form W–Ti alloy. The x-ray diffraction (XRD) analysis confirms the Co–silicide as $CoSi_2$ and shows the existence of W signals indicating that Ti is dissolved in W without forming any compound. In Fig. 1, it is observed that high concentration of oxygen exists only on the shallow surface region. In fact, the W–Ti alloy is more stable than W and other W alloy regarding the resistance to oxidation at high temperatures as compared with metallization of the W/Co/Si[10] and W/Co–Mo/Si[19] systems where W and W–Co were seen to be significantly oxidized at even lower temperatures in the same N_2 environment. Thus, the W–Ti alloy derived from the W/Co–Ti/Si system can be retained. A $CoSi_2$ layer of 678 Å thickness (3.52 Å of $CoSi_2$ is formed per Å of Co)[9] is formed and the composition of W–Ti alloy is 90.6% W

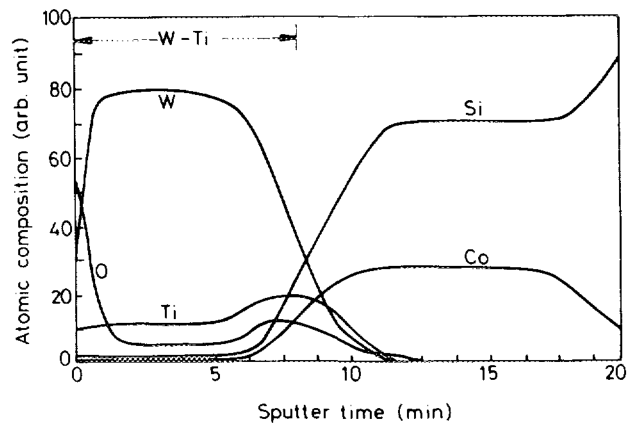

FIG. 1. AES depth profile for the system of W(400 Å)/$Co_{63}Ti_{37}$(370 Å)/Si annealed at 760 °C for 30 min.

to 9.4% Ti by weight. This composition is nearly equal to that of Ti:W (10:90) adopted by Phate *et al.*[20] If the W–Ti or its oxide derived from W/Co–Ti over silicon oxide after annealing is to be removed for patterning, an additional photolithographic process is needed. However, because the etching solutions for selectively removing the W–Ti alloy on silicon oxide will attack photoresist more or less, a positive photoresist pattern has to be generated before the metal deposition. Lift-off of the metals over photoresist was performed by dipping the wafers in ultrasonic agitated acetone before annealing.

For the system of W/Co–Mo/Si, bilayer self-aligned $MoSi_2/CoSi_2$/Si silicided contact can be accomplished by resorting to a two-step annealing, which is intervened by a selective etching. The first annealing was performed at 600 °C for 60 min where some Co was alloyed with the overlying W layer. After selective etching with a solution of $NH_4OH+H_2O_2+2H_2O$ at 70 °C, the wafer was further annealed at a higher temperature of 800 °C. Two separate layers of tetragonal $MoSi_2$ and contact $CoSi_2$ will finally be obtained as shown by the AES depth profile in Fig. 2. In this system, a $MoSi_2$ layer of 744 Å thickness is formed

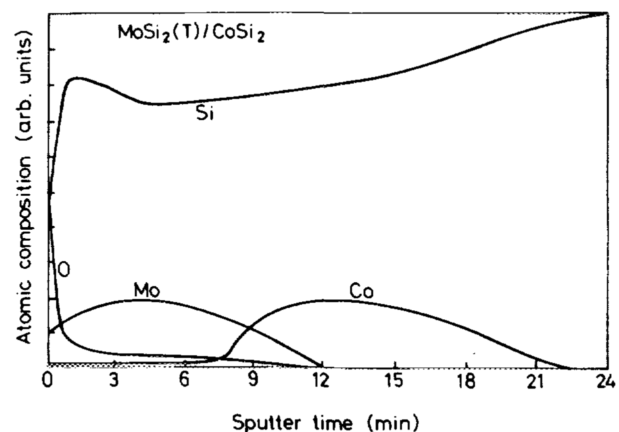

FIG. 2. AES depth profile for the system of W(400 Å)/$Co_{55}Mo_{45}$(540 Å)/Si finished with two-step annealing at 600 °C for 60 min and 800 °C for 20 min.

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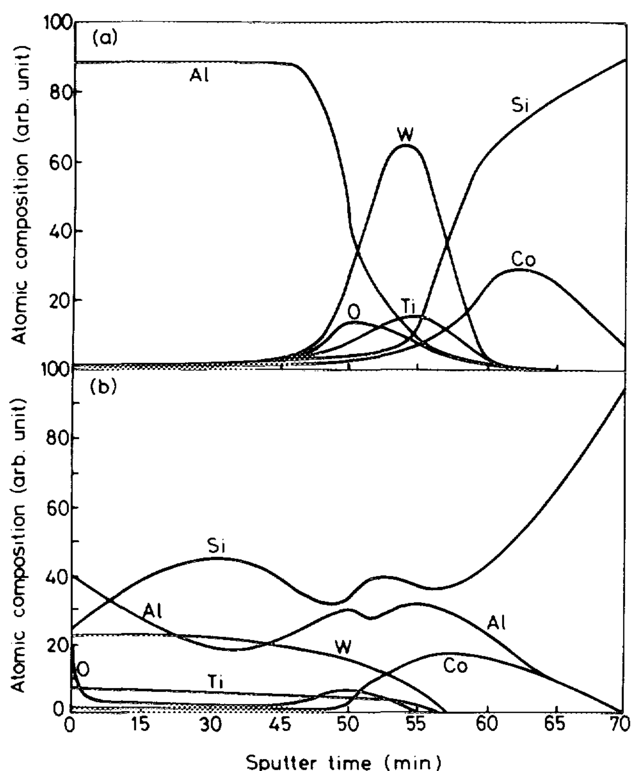

FIG. 3. AES depth profiles for the Al/W-Ti/$CoSi_2$/Si structure after 20 min annealing at (a) 550 °C, and (b) 600 °C.

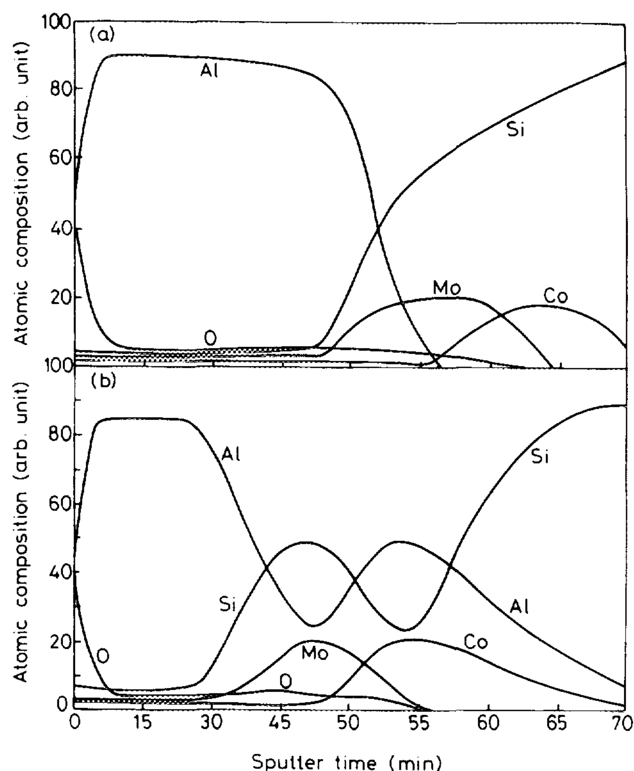

FIG. 4. AES depth profiles for the Al/$MoSi_2$/$CoSi_2$/Si structure after 20-min annealing at (a) 500 °C, and (b) 550 °C.

in situ since no Mo is alloyed with W at the temperature of the first anealing[21] and all of the Mo is transformed into silicide (2.59 Å of $MoSi_2$ is formed per angstrom of Mo).[9] The two-step annealing for silicide formation is self-aligned because no silicide lateral growth is observed at 600 °C and the materials derived from the W/Co–Mo over silicon oxide can also be removed by the selective etching; no additional mask is needed to generate silicide or metal pattern.

The single silicide contact of $CoSi_2$ on Si was formed from the Mo(400 Å)/Co(380 Å)/Si system. The system was annealed at 550 °C for 20 min followed by selectively etching away the Mo and its oxide over the contact area. The Mo film and its oxide together with the underlying Co over the silicon oxide were also removed at the same time. Further annealing was subsequently performed at 750 °C. A $CoSi_2$ layer of 1338 Å thickness is formed.

B. Evaluation of W–Ti and $MoSi_2$ as diffusion barrier to $CoSi_2$

1. AES depth profiles

For the W–Ti/$CoSi_2$/Si system with aluminum metallization, the integrity of the structure can be preserved up to 550 °C as shown by the AES depth profile in Fig. 3(a). As the temperature is raised to 600 °C, Al penetrates to Si substrate [Fig. 3(b)]. The bilayer $MoSi_2$/$CoSi_2$ silicided contact can resist Al invasion into the system up to 500 °C [Fig. 4(a)]. At 550 °C, Al is seen to penetrate into Si substrate [Fig. 4(b)]. For a single layer of $CoSi_2$ in contact

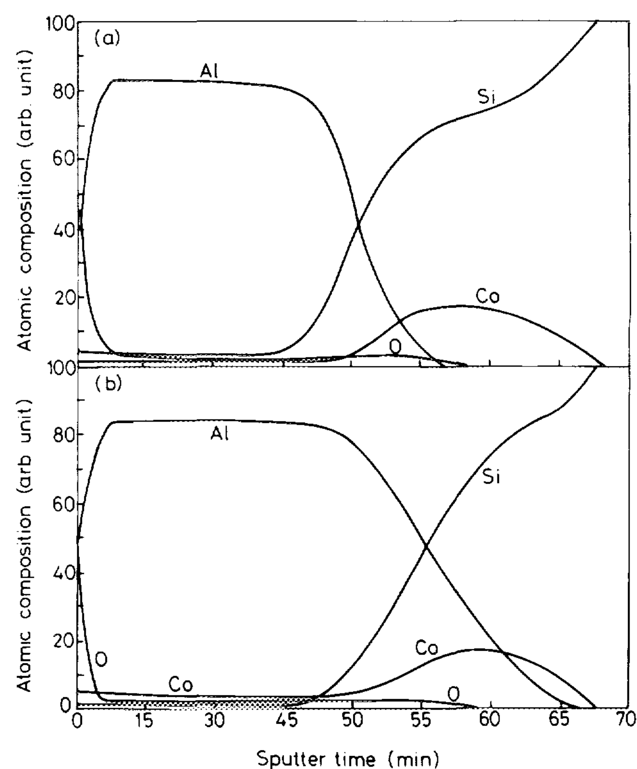

FIG. 5. AES depth profile for the Al/$CoSi_2$/Si structure after 20-min annealing at (a) 450 °C, and (b) 500 °C.

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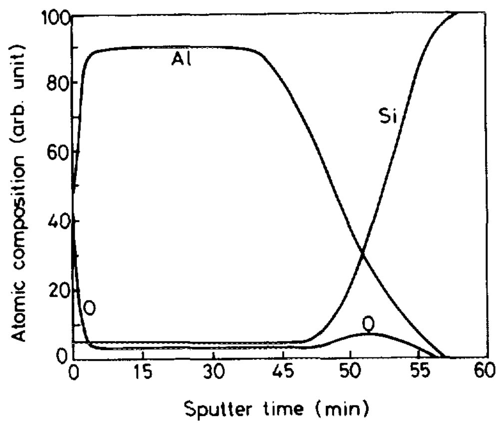

FIG. 6. AES depth profile for the Al/Si structure after 20-min annealing at 400 °C.

with Si, the maximum temperature at which $CoSi_2$ can resist the invasion of Al is 450 °C [Fig. 5(a)]. At 500 °C, it is seen that Al has almost reached the Si substrate [Fig. 5(b)]. Based on the results of AES depth profiling, we conclude that W–Ti is more stable than $MoSi_2$ and $CoSi_2$ with regard to the capability as a diffusion barrier to Al, while $MoSi_2$ is superior to $CoSi_2$. On the other hand, for Al directly in contact with Si substrate, Si is seen to be dissolved in Al at 400 °C (Fig. 6). The content of Si in Al increases with annealing temperature.

2. Sheet resistance measurement

The sheet resistance after deposition of Al is about 148 mΩ/sq. for all the systems built up with and without silicide. Figure 7 shows the resistance versus annealing temperature for the various systems. The sheet resistance of Al on W–Ti/$CoSi_2$/Si remains at a stable low value up to 550 °C, while it increases abruptly at 600 °C. The resistance increases evidently at 550 °C for Al on $MoSi_2$/$CoSi_2$/Si.

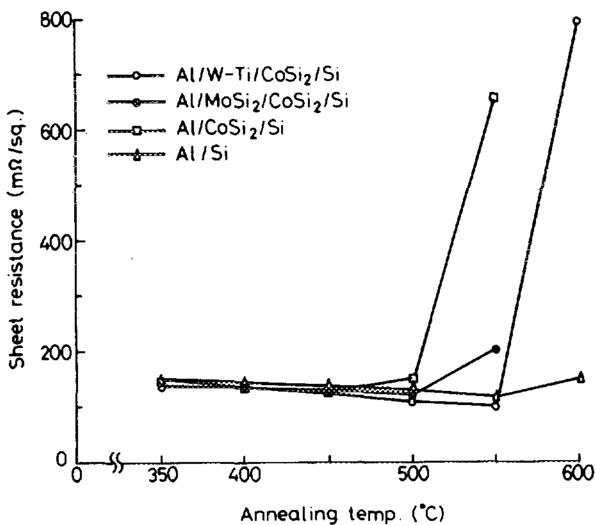

FIG. 7. Sheet resistance after 20-min post-Al annealing at temperatures from 350 to 600 °C for the Al/W-Ti/$CoSi_2$/Si, Al/$MoSi_2$/$CoSi_2$/Si, Al/$CoSi_2$/Si, and Al/Si structures.

For Al on $CoSi_2$/Si the value slightly increases at 500 °C, and then increases abruptly at 550 °C. The temperatures at which the sheet resistance abruptly increases for each system, except the Al/Si, roughly correspond to the temperatures at which Al penetrates into Si substrate as revealed in the AES depth profiles, i.e., 600 °C for Al/W–Ti/$CoSi_2$/Si, 550 °C for Al/$MoSi_2$/$CoSi_2$/Si, and 500 °C for Al/$CoSi_2$/Si. The increase of sheet resistance is apparently due to the reaction between Al and silicide and the agglomeration of Al on the surface. Usually, compounds of good conductor have a higher resistivity than the conductor itself. For the aluminum contacting Si substrate, the sheet resistance decreases slightly all the way from 350 to 550 °C, then inreases at 600 °C. In fact, the sheet resistances for the other systems also decrease slightly before breakdown of the respective structure because of recrystallization and grain growth of the Al film. For the Al and Si binary alloy system, the lowest eutectic temperature is 577 °C;[22] above this, Al film will become liquid and coalesce into island due to surface tension.

3. SEM micograph

Morphology of the silicides (or silicon when Al is directly in contact with Si) surface is observed by plan-view SEM micrographs after selectively stripping away the Al and W–Ti on all the related structures by phosphoric acid. Figure 8 shows the micrographs of the $CoSi_2$ surface for the Al/W–Ti/Co–Ti/$CoSi_2$/Si system. The initial morphology of silicide [Fig. 8(a)] can be preserved up to 550 °C [Fig. 8(b)]. At 600 °C, the $CoSi_2$ surface is devastated and looks like a beehive presumably due to drastic Al reaction with W–Ti and the underlying $CoSi_2$ as confirmed by the AES depth profile in Fig. 3(b). For the Al/$MoSi_2$/$CoSi_2$/Si system, the initial silicide surface [Fig. 9(a)] becomes slightly corrugated at 500 °C [Fig. 9(b)], and it becomes very rough at 550 °C [Fig. 9(c)]. The rough morphology at 550 °C is related to the AES depth profile in Fig. 4(b), where Al is seen to penetrate through the silicides to the Si substrate. In the Al/$CoSi_2$/Si system, the surface of $CoSi_2$ does not change at 450 °C [Fig. 10(a)] but pits are observed occasionally at 500 °C [Fig. 10(b)]. At 550 °C, it looks like a beehive [Fig. 10(c)]. When Al is directly in contact with Si substrate, the silicon surface is marked with pinholes at 450 °C [Fig. 11(a)], and is dispersed with large-area indents at 550 [Fig. 11(b)] and 600 °C [Fig. 11(c)].

4. Visual inspection

Degradation of each system can roughly be checked by visually inspecting the surface of aluminum on the silicides and silicon substrate. The temperatures at which the aluminum is seen to slightly discolor are 500 °C for Al/$MoSi_2$/$CoSi_2$/Si and 450 °C for Al/$CoSi_2$/Si, while the Al on W–Ti/$CoSi_2$/Si keeps shining up to 550 °C. The Al surface will discolor evidently and becomes rough at 600 °C for Al/W–Ti/$CoSi_2$/Si, 550 °C for Al/$MoSi_2$/$CoSi_2$/Si, and 500 °C for Al/$CoSi_2$/Si. These temperatures also roughly correspond to the temperatures at which the

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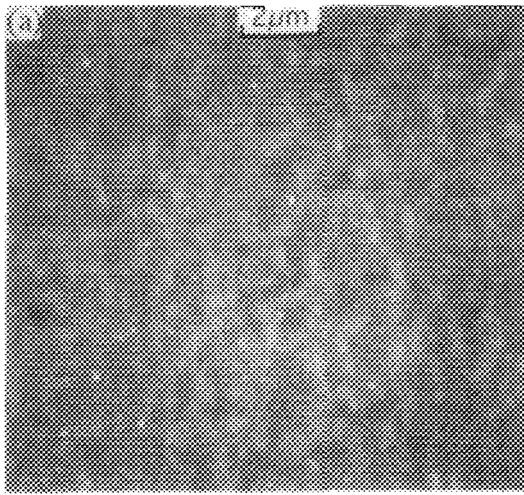
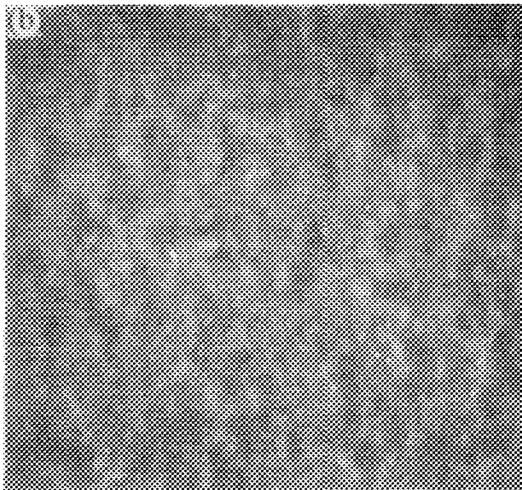




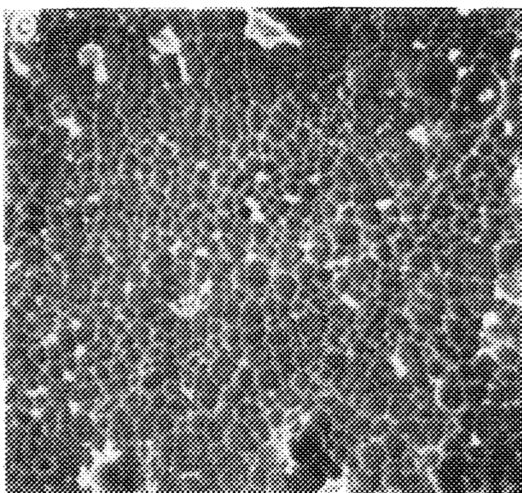
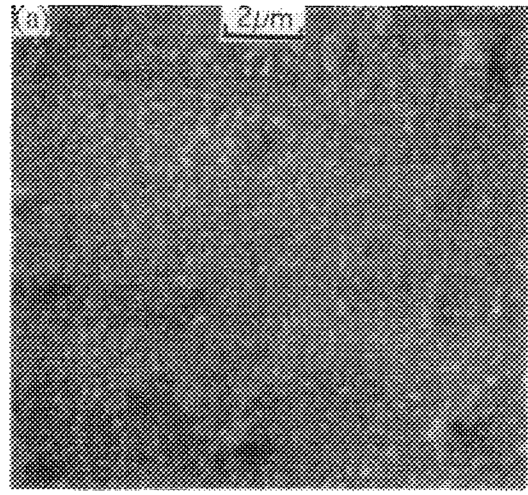
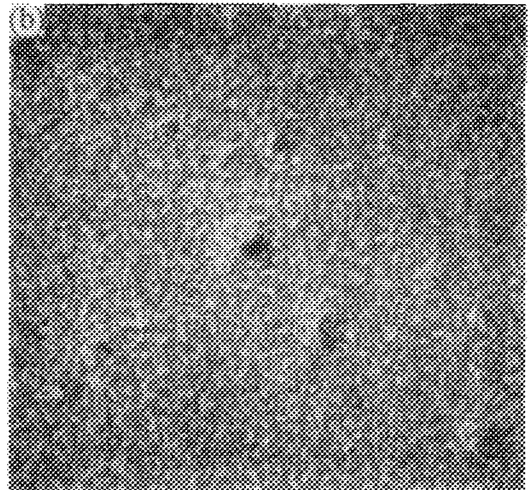


FIG. 8. SEM micrographs of the silicide surface for the Al/W–Ti/$CoSi_2$/Si structure after removal of Al and W–Ti layers: (a) as-Al-deposited; post-Al annealing for 20 min at (b) 550 °C, and (c) 600 °C.





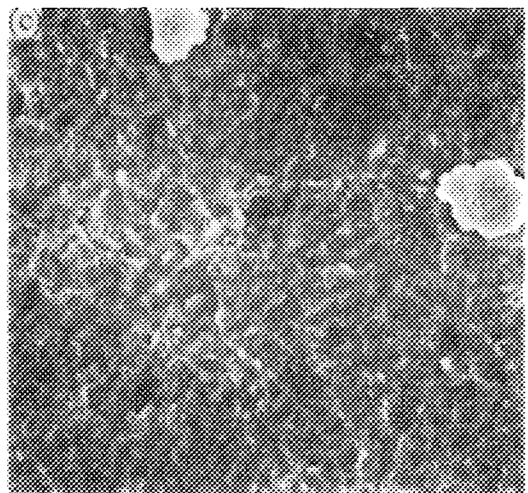


FIG. 9. SEM micrographs of the silicide surface for Al/$MoSi_2$/$CoSi_2$/Si structure after removal of Al layer: (a) as-Al-deposited; post-Al annealing for 20 min at (b) 500 °C, and (c) 550 °C.

respective sheet resistance shows an abrupt increase, and the silicides suffer severe corrosion by Al as shown by the AES depth profiles. The metallic luster of Al on Si becomes slightly rustic at 550 °C; the surface dicolors severely and also looks bubbly at 600 °C.

5. *I–V* characteristics

Silicided p^+n junction diodes using various silicidation schemes described in the previous section were fabricated and their current–voltage characteristics were investigated with respect to the effect of post-Al metallization anneal-

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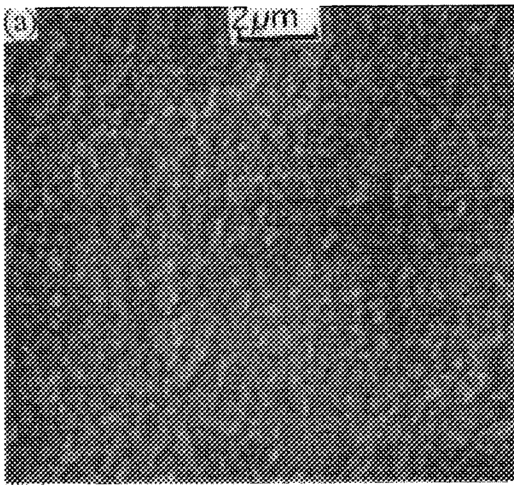
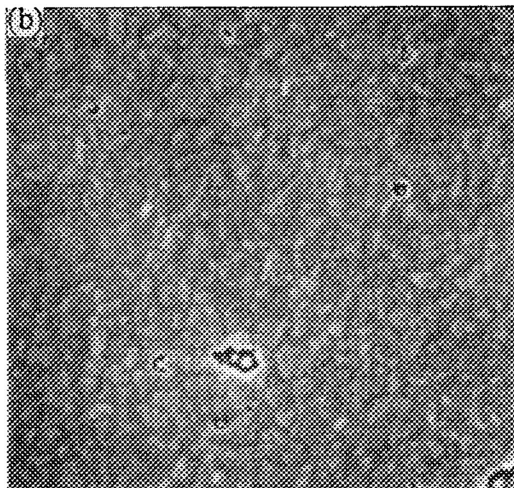




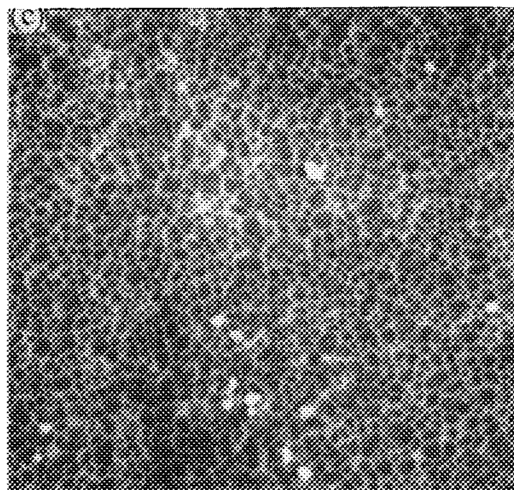
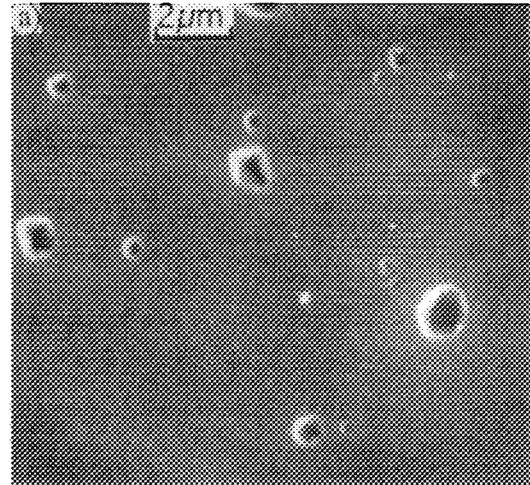
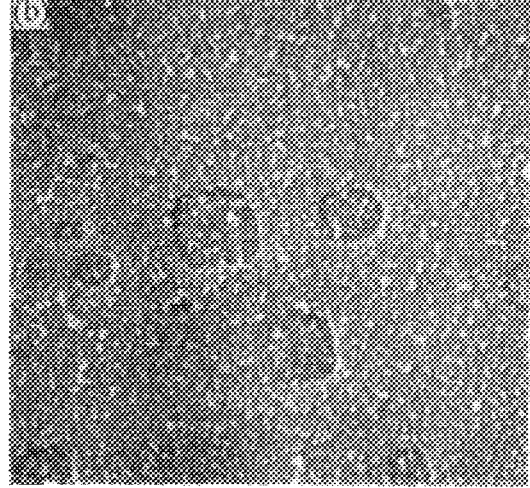


FIG. 10. SEM micrographs of the silicide surface for the Al/$CoSi_2$/Si structure after removal of Al layer. A 20-min post-Al annealing is performed at (a) 450 °C, (b) 500 °C, and (c) 550 °C.





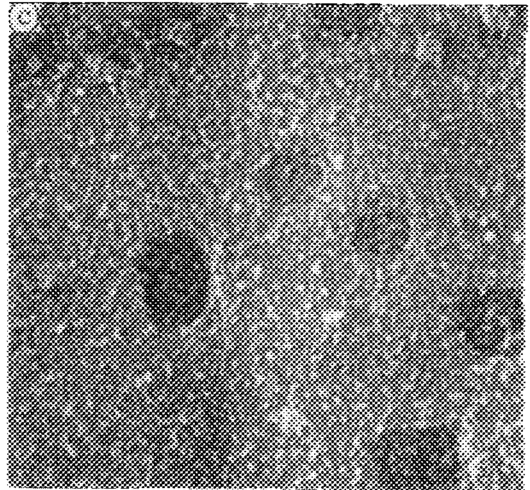


FIG. 11. SEM micrographs of the silicon surface for Al/Si after removal of Al layer. A 20-min post-Al annealing is performed at (a) 450 °C, (b) 550 °C, and (c) 600 °C.

ing. The starting material is n-type (100)Si wafers with 10 Ω cm resistivity. The diodes area is defined to be 0.0047 cm^2. Channel stopper, guard ring, and n^+ contact on the backside were built to the diodes. Boron difluoride (BF_2^+) was implanted at an energy of 50 keV to a dose of 1.0×10^{15} cm^{-2} and activated at 950 °C for 20 min. The depth of p^+n junction was measured to be 0.26 μm by spreading resistance profiler. I–V characteristics of the di-

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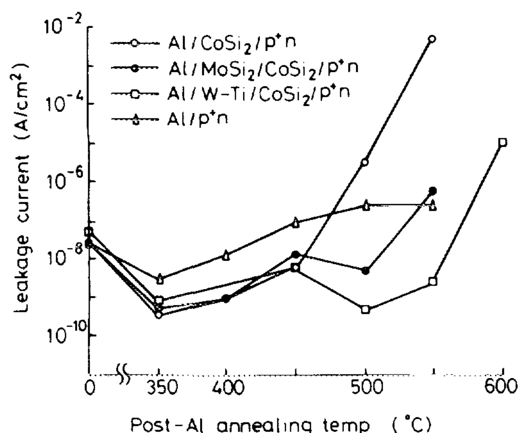

FIG. 12. Reverse leakage current density at -5 V for shallow p^+n diodes with various silicided contacts vs post-Al annealing temperature. The Al/p^+n diodes without silicide are also included for comparison.

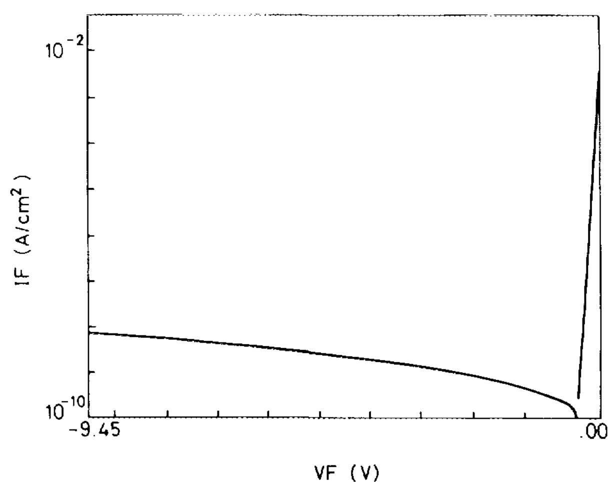

FIG. 13. A typical I–V characteristic for the $Al/W\text{–}Ti/CoSi_2/p^+n$ diode after a post-Al annealing at 550 °C for 20 min.

odes finished with silicidation, Al deposition, and post-Al annealing were then measured. Aluminum of 7500 Å in thickness is applied to each silicided and unsilicided p^+n junction diode.

The reverse leakage at -5 V for different silicided diodes is illustrated in Fig. 12. Without post-Al annealing, the leakage current density is 25–53 nA/cm^2 and the forward ideal factor is 1.17–1.45 for all diodes. The larger leakage may be due to the stress caused by the aluminum deposition on cold substrate. After annealing, the leakage lowers and the forward ideality factor becomes closer to unity. Before breakdown of the initial structure for each system, the leakage decreases to 0.4–6.0 nA/cm^2. The temperatures at which drastic increase of leakage occurs are 500 °C for $Al/CoSi_2/p^+n$, 550 °C for $Al/MoSi_2/CoSi_2/p^+n$, and 600 °C for $Al/W\text{–}Ti/CoSi_2/p^+n$ diodes. Breakdown of the diode occurs supposedly because diffusion barrier and silicide are corroded by reaction with Al. Al spiking into Si substrate will be caused by Si being dissolved in Al film when Al reaches the Si substrate locally. Without any silicide contact, the lowest leakage is 2–3 nA/cm^2 at 350 °C for the Al/p^+n diode, and the leakage increases with increasing annealing temperature. At 400 °C, it will be more than 10 nA/cm^2. However, no abrupt increase of leakage is observed for the Al/p^+n diode up to an annealing of 600 °C presumably due to a deeper junction from the Si surface compared with the silicided diodes where some silicon beyond the junction is consumed by the silicides. The I–V characteristics for the $Al/W\text{–}Ti/CoSi_2/p^+n$ diodes as illustrated in Fig. 13, confirms that this metallization system is able to sustain a post-Al annealing at 550 °C for 20 min without causing any performance degradation; the reverse leakage at -5 V is 2–3 nA/cm^2 and the forward ideal factor is 1.04. If the allowable reverse leakage at -5 V for a p^+n shallow junction is arbitrarily defined as 6.0 nA/cm^2, the upper limit of post-Al annealing temperatures would be 550 °C for $Al/W\text{–}Ti/CoSi_2/p^+n$, 500 °C for $Al/MoSi_2/CoSi_2/p^+n$, and 450 °C for $Al/CoSi_2/p^+n$. These results are consistent with those of sheet resistance measurements, SEM micrographs, and AES depth profiles. An Al/Si contact without any silicide or diffusion barrier is not suitable for a shallow junction if processing temperature higher than 400 °C after Al deposition is required.

The proposed mechanism for W–Ti as a diffusion barrier is that a very stable and insoluble TiO_2 is formed on the surface to impede Al corrosion.[23] The other effect of Ti in W is that it can be precipitated at the tungsten's grain boundary and thus block the fast-diffusion path for aluminum and silicon. It is apparent that W–Ti is a more efficient diffusion barrier than W. Furthermore, nitrogen may be incorporated into the W–Ti film during silicidation of the W/Co–Ti/Si system in the N_2 environment. It is believed that nitrogen improves the barrier properties of the W–Ti film by stuffing the grain boundaries, thereby substantially reducing the rate of interdiffusion.[24] The sustainable temperature of 550 °C for the *in situ formed* W–Ti as diffusion barrier in this work is better than those deposited by sputtering without nitrogen incorporation.[24,25]

IV. SUMMARY

Based on the results of AES depth profiles, sheet resistance measurements, SEM micrographs, visual check, and I–V characteristics measurements, we conclude that by employing the *in situ* formed W–Ti alloy layer as a diffusion barrier between aluminum and $CoSi_2$, the $Al/W\text{–}Ti/CoSi_2/p^+n$ diode is able to sustain an annealing treatment at 550 °C for 20 min without causing any performance degradation. The sustainable annealing temperature for the self-aligned $Al/MoSi_2/CoSi_2/p^+n$ diode is 500 °C. For the $Al/CoSi_2/p^+n$ diode without any diffusion barrier, it can stand up to 450 °C. Direct Al contact to the shallow p^+n junction without any intervening silicide or diffusion barrier keeps well only up to 350 °C.

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