JVSTB Journal of Vacuum Science & Technology B

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Citation: Journal of Vacuum Science & Technology B **18**, 1929 (2000); doi: 10.1116/1.1305273
View online: http://dx.doi.org/10.1116/1.1305273
View Table of Contents: http://scitation.aip.org/content/avs/journal/jvstb/18/4?ver=pdfcov
Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

Effects of composition and N_2 plasma treatment on the barrier effectiveness of chemically vapor deposited WSi_x films

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(Received 1 May 1998; accepted 21 April 2000)

This work investigates the thermal stability of chemically vapor deposited amorphous WSi_x layers used as a diffusion barrier between Cu and Si substrate, in which the WSi_x layers were deposited to a thickness of about 50 nm using the SiH_4 reduction of WF_6 at various SiH_4/WF_6 flow ratios. For 30 min annealing in nitrogen ambient, the effectiveness of the WSi_x layers as barriers between a copper overlayer and a p^+-n junction diode decreases as the Si/W atomic ratio, x, increasing from 1 to 1.3. This composition change is obtained by raising the SiH_4/WF_6 flow ratio from 3 to 50. As deposited, all films are x-ray amorphous. Their resistivity increases roughly linearly with x. The barrier capability of WSi_x layers can be significantly improved by an *in situ* N_2 plasma treatment. The N_2 plasma treatment produces a very thin layer of WSiN (about 5 nm) on the surfaces of WSi_x layers. In particular, the Cu/WSiN/WSi_x/p^+-n junction diodes with the WSi_x layers deposited with a SiH_4/WF_6 flow ratio of 3 were able to remain intact up to at least 600 °C. © *2000 American Vacuum Society*. [S0734-211X(00)03204-2]

I. INTRODUCTION

Copper (Cu) has been extensively studied as a potential metallization material for future ultralarge scale integrated circuits because of its low electrical resistivity, superior electromigration resistance,[1–3] and possibility of deposition by electroplating as well as the chemical vapor deposition (CVD) method.[4–6] Moreover, copper has a better thermal conductivity, higher melting point, and less potential of hillocks' formation than the conventionally used Al alloys.[7] However, Cu metallization is faced with many challenges in practice, such as the lack of a stable self-passivated oxide, poor adhesion to dielectric layers, difficulty of dry etching, and the formation of Cu–Si compounds at low temperatures (about 200 °C).[8] In addition, copper diffuses fast in silicon and causes deep-level trapping;[9] it also drifts through oxide layers under accelerated electric field.[10,11] Therefore, a diffusion barrier between Cu and its underlying layers is considered as a prerequisite for practical applications of Cu metallization.

Various materials have been studied as diffusion barriers between Cu and its underlying layers. Sputter deposited nitride-based diffusion barriers, such as TiN,[12,13] WN,[14,15] TaN,[16–18] MoN,[19,20] and TiWN,[21,22] have attracted extensive attention for a long time. However, these barriers are generally polycrystalline, and grain boundaries in the barriers provide fast paths for Cu diffusion. Typically, the atomic diffusivities in the amorphous phase are orders of magnitude below those of the corresponding polycrystalline phase.[23,24] Thus, the amorphous diffusion barrier is of great interest. In this work, we used chemically vapor deposited amorphous WSi_x (CVD–WSi_x) layers as a diffusion barrier between Cu and Si substrate. The effects of composition on the barrier capability of the amorphous CVD–WSi_x layers were studied using electrical measurements as well as material analyses. We found that the barrier effectiveness depended on the composition of the amorphous WSi_x layers. To improve the barrier capability of the WSi_x layers, we formed a very thin WSiN layer on the surfaces of WSi_x layers using an *in situ* N_2 plasma treatment. The resultant WSiN/WSi_x barrier bilayer was proven to possess a much improved barrier capability against Cu diffusion.

II. EXPERIMENT

The thermal stability of barrier layers was evaluated by measuring the leakage current of thermally annealed Cu/barrier/p^+-n junction diodes. The starting materials used for the diodes fabrication were *n*-type, (100) oriented silicon wafers with 4–7 Ω cm nominal resistivity. After Radio Corporation of America standard cleaning, the wafers were thermally oxidized to grow a 500 nm oxide layer. Diffusion regions with area sizes of 500×500 and $1000\times1000\ \mu m^2$ were defined on the oxide covered wafers using the conventional photolithographic technique. The p^+-n junctions with a junction depth of about 0.3 μm were formed by BF_2^+ implantation at 40 keV to a dose of $3\times10^{15}\ cm^{-2}$ followed by furnace annealing at 900 °C for 30 min in N_2 ambient.

After the junctions were formed, the wafers were divided into three groups for the preparation of the following devices: Cu/p^+-n, Cu/WSi_x/p^+-n, and Cu/WSiN/WSi_x/

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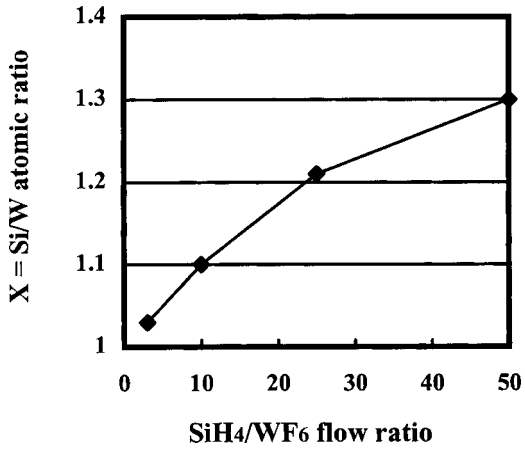

FIG. 1. Si/W atomic ratio, x, of WSi_x films deposited at various SiH_4/WF_6 flow ratios. The films were deposited at a temperature of 250 °C, total gas pressure of 12 mTorr, and WF_6 flow rate of 2 sccm.

p^+-n junction diodes, in which the WSi_x layers were deposited by the CVD method to a thickness of about 50 nm using the SiH_4 reduction of WF_6 at various SiH_4/WF_6 flow rates. In this study, the WSi_x layers were deposited using a load-locked cold wall CVD system with the following deposition conditions: substrate temperature 250 °C, total gas pressure 12 mTorr, WF_6 flow rate 2 sccm, and SiH_4 flow rate ranging from 6 to 100 sccm. For the formation of $WSiN/WSi_x$ barrier bilayers, an *in situ* N_2 plasma treatment was performed on the surfaces of CVD–WSi_x layers without breaking the vacuum. The N_2 plasma treatment was performed with the following conditions: N_2 flow rate 80 sccm, total gas pressure 25 mTorr, plasma power 100 W, and treatment time 300 s. Finally, Cu metallization was applied to all samples.

To investigate the thermal stability of the variously metallized junction diodes, the samples were thermally annealed in N_2 flowing furnace for 30 min at a temperature ranging from 200 to 700 °C. Reverse bias leakage current measurements on the thermally annealed diodes were used to evaluate the barrier capability. An HP-4145B semiconductor parameters analyzer was used for the measurement, and at least 30 diodes were measured in each case. Unpatterned samples of WSi_x/Si, $Cu/WSi_x/Si$, and $Cu/WSiN/WSi_x/Si$ multilayer structures were also prepared for material analysis. Sheet resistance of the multilayer structures was measured using a four point probe. Auger electron spectroscopy (AES) was used to determine the composition of WSi_x films. Rutherford backscattering spectroscopy (RBS) was used to determine the Si/W atomic ratio. Scanning electron microscopy (SEM) was employed to observe the surface morphology and microstructure. X-ray diffraction (XRD) analysis was used for phase identification.

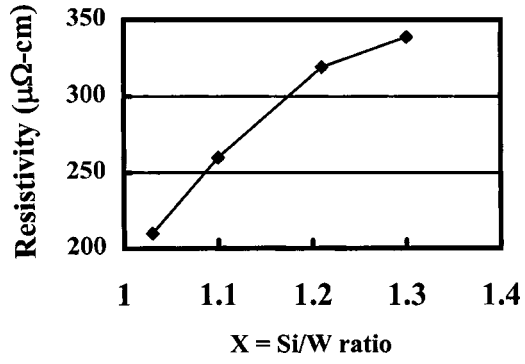

FIG. 2. Resistivity of WSi_x films vs x. The WSi_x films were deposited at a substrate temperature of 250 °C, total gas pressure of 12 mTorr, and WF_6 flow rate of 2 sccm.

III. RESULTS AND DISCUSSION

A. Properties of CVD–WSi_x films

Before investigating the thermal stability of $Cu/WSi_x/p^+-n$ junction diodes, properties of CVD–WSi_x films, including the Si/W atomic ratio, electrical resistivity,

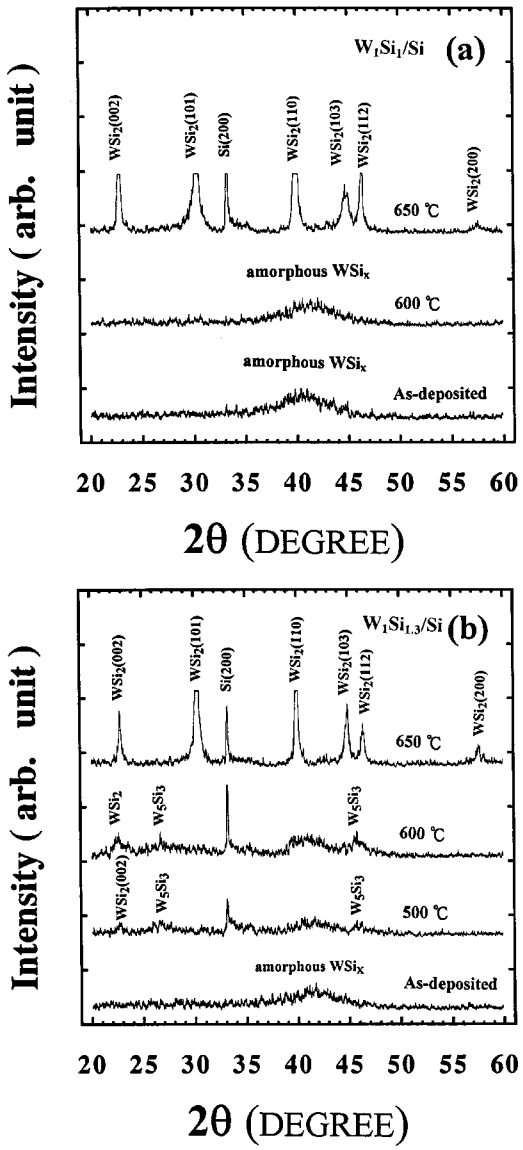

FIG. 3. XRD spectra of (a) W_1Si_1/Si and (b) $W_1Si_{1.3}/Si$ samples before and after annealing at various temperatures. The W_1Si_1 and $W_1Si_{1.3}$ layers are 150 nm thick.

TABLE I. Crystalline phases of CVD–WSi_x films after annealing for 30 min in N_2 ambient at various temperatures.

Annealing temperatures	Si/W atomic ratio x		
	1.0	1.1	1.3
As-deposited	Amorphous	Amorphous	Amorphous
400 °C	Amorphous	Amorphous	Amorphous
500 °C	Amorphous	Amorphous	Weak WSi_2, weak W_5Si_3
600 °C	Amorphous	Weak WSi_2, weak W_5Si_3	Weak WSi_2, weak W_5Si_3
650 °C	WSi_2	WSi_2	WSi_2
800 °C	WSi_2	WSi_2	WSi_2

and crystalline phase were investigated. Figure 1 shows the Si/W atomic ratio of WSi_x layers deposited with various SiH_4/WF_6 flow ratios, as determined by RBS measurements. We found that the Si/W atomic ratio, x, in the WSi_x layer increased from 1.0 to 1.3 as the SiH_4/WF_6 flow ratio was increased from 3 to 50. The resistivity of the WSi_x films also increased with increasing SiH_4/WF_6 flow ratio, as shown in Fig. 2; it increased from 210 to 340 $\mu\Omega$ cm as the SiH_4/WF_6 flow ratio was increased from 3 to 50. The increase in resistivity is presumably due to increasing amount of Si incorporated in the WSi_x layer. Similar results were reported by Kottke *et al.* that higher flow ratios of SiH_4/WF_6 resulted in WSi_x films of higher resistivities and Si/W atomic ratios, although the WSi_x films in their study were deposited at a substrate temperature of 360 °C and a SiH_4/WF_6 flow ratio of 94 to 438, and the resultant WSi_x layers were nonstoichiometric silicon-rich (Si/W atomic ratios larger than 2.0).[25]

The phase of the WSi_x layers was identified by XRD analysis using a 30 keV copper-$K\alpha$ radiation. Figures 3(a) and 3(b) show XRD spectra for the 150-nm-thick films with $x=1$ and 1.3 on silicon substrates before and after annealing at various temperatures. For $x=1$, the as-deposited films were amorphous and the amorphous state remained unchanged even after annealing at 600 °C for 30 min in N_2 ambient [Fig. 3(a)]. It has been reported that the absence of grain boundaries in the amorphous barrier layer contributes to the excellent barrier property, because fast diffusion paths of the grain boundaries are prevented.[26] In this work, the nature of amorphous phase makes the W_1Si_1 layers very attractive in barrier application. Diffraction peaks of WSi_2 phase appeared in the W_1Si_1 samples after annealing at 650 °C for 30 min in N_2 ambient [Fig. 3(a)], indicating silicidation of the layer.

For the $W_1Si_{1.3}$/Si samples, the as-deposited films were also amorphous [Fig. 3(b)]. Weak peaks of tungsten silicides were detected after annealing at 500 °C, and the diffraction peaks slightly intensified after annealing at 600 °C, indicating the grain growth of tungsten silicides. Similar results were reported that Si-rich ($x>2.0$) CVD films converted to tungsten silicides after annealing at 500 °C.[27–29] We found that the crystallization temperature of amorphous CVD–WSi_x layers decreased with increasing Si/W atomic ratio x. Table I summarizes the crystalline states of different CVD–WSi_x films after annealing at various temperatures, as determined by XRD analysis.

B. Composition effects on the barrier capability of CVD–WSi_x films

1. Electrical measurements

Figure 4 illustrates the statistical distributions of reverse bias current density measured at -5 V for the Cu/p^+-n, $Cu/W_1Si_1/p^+-n$, and $Cu/W_1Si_{1.3}/p^+-n$ junction diodes annealed at various temperatures; both layers of W_1Si_1 and $W_1Si_{1.3}$ were 50 nm thick. Since copper reacts with Si at low temperatures (200 °C),[9,10] diodes without a barrier layer between Cu and Si substrate failed after annealing at 200 °C for 30 min [Fig. 4(a)]. With a 50-nm-thick WSi_x barrier layer between Cu and Si substrate, the junction diodes of $Cu/W_1Si_1/p^+-n$ and $Cu/W_1Si_{1.3}/p^+-n$ were able to retain their electrical integrity up to 500 and 450 °C, respectively [Figs. 4(b) and 4(c)]. The barrier capability of amorphous WSi_x layers decreased with increasing Si/W atomic ratio, and the decrease in thermal stability of the $Cu/W_1Si_{1.3}/p^+-n$ junction diodes correlated with the lower crystallization temperature of the amorphous $W_1Si_{1.3}$ layers.

2. XRD analyses

The drastic increase in sheet resistance of the $Cu/WSi_x/Si$ samples was attributed to the formation of high resistivity η''-Cu_3Si precipitates, as confirmed by XRD analyses shown in Fig. 5. The XRD spectra of as-deposited samples did not reveal the broadband of amorphous WSi_x layers presumably because the WSi_x layers were only 50 nm thick and were covered with 300-nm-thick Cu overlayers. Strong diffraction peaks of Cu_3Si appeared in the XRD spectra of $Cu/W_1Si_1/Si$ and $Cu/W_1Si_{1.3}/Si$ samples annealed at 600 and 500 °C, respectively. It is clear that the stability of the WSi_x layers in contact with Cu decreases with increasing Si/W atomic ratio. Furthermore, by comparing the XRD spectra of $Cu/W_1Si_1/Si$ samples [Fig. 5(a)] with those of W_1Si_1/Si samples [Fig. 3(a)], we found that the crystallization temperature of WSi_x layers in the $Cu/W_1Si_1/Si$ samples is about 50 °C lower than that in the W_1Si_1/Si samples. This discrepancy is presumably due to the presence of Cu overlayers for the $Cu/W_1Si_1/Si$ samples. It was reported that the crystallization temperature of $W_{80}Si_{20}$ film on SiO_2 dropped from 800 to 650 °C when the $W_{80}Si_{20}$ film was in contact with a polycrystalline copper layer.[30] It was also reported that the formation temperature of tantalum (Ta) silicide in Ta/Si system dropped from 700 to 650 °C when the Ta film was in contact with a polycrystal-

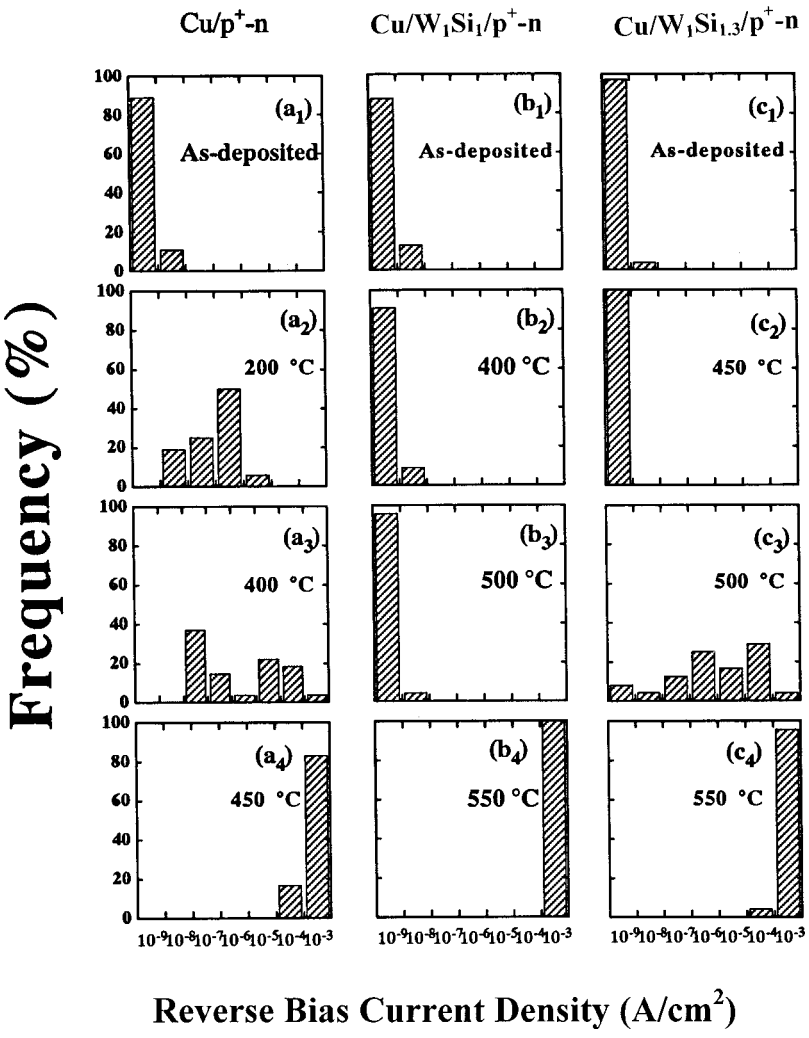

FIG. 4. Histograms showing statistical distributions of reverse bias current density for (a) Cu/p^+-n, (b) Cu/W_1Si_1/p^+-n, and (c) Cu/$W_1Si_{1.3}$/p^+-n junction diodes annealed at various temperatures. The WSi_x layers are 50 nm thick.

line copper layer.[31] In this work, the W_1Si_1/Si samples remained stable up to 600 °C with no detection of tungsten silicide formation [Fig. 3(a)], while diffraction peaks of tungsten silicide phases were detected for the Cu/W_1Si_1/Si samples annealed at the same temperature [Fig. 5(a)]. This suggests that the accelerated crystallization for W_1Si_1 layers was related to the contact with polycrystalline Cu overlayers. The accelerated crystallization is presumably due to the penetration of Cu atoms through W_1Si_1 layers via localized defects, forming Cu_3Si phase and promoting silicidation at the W_1Si_1/Si interface.[31] Table II summarizes the silicides formed on thermally annealed Cu/Si and Cu/WSi_x/Si samples.

3. SEM observations

SEM was used to investigate the surface and cross-sectional morphology of thermally annealed Cu/barrier/p^+-n junction diodes. Figure 6 shows SEM micrographs for the as-deposited as well as 500 °C annealed Cu/W_1Si_1/p^+-n and Cu/$W_1Si_{1.3}$/p^+-n junction diodes. The barrier structure remained unchanged for the Cu/W_1Si_1/p^+-n diodes after annealing at 500 °C [Fig. 6(b)]; however, large localized Cu_3Si protrusions were observed on the Cu/$W_1Si_{1.3}$/p^+-n diodes after annealing at the same temperature [Fig. 6(d)]. Failure of the 500 °C annealed Cu/$W_1Si_{1.3}$/p^+-n diodes is likely associated with these localized Cu_3Si protrusions, which were presumably caused by the diffusion of Cu atoms through the weak points (such as vacancy-accumulated voids and grain boundaries of crystallized $W_1Si_{1.3}$ layers) in the $W_1Si_{1.3}$ barrier layers.

Based on the earlier results, we concluded that the higher the Si/W atomic ratio in WSi_x films is, the lower the crystallization temperature of the WSi_x films becomes (Fig. 3). Accordingly, WSi_x films of higher Si content are not suitable for diffusion barrier application. Moreover, failure of WSi_x barrier layer in the Cu/WSi_x/Si structure was closely related to the presence of Cu_3Si phase, indicating that the barrier failure was due to the interdiffusion of Cu and Si through the WSi_x barrier at elevated temperatures. This suggests that the thermal stability of Cu/WSi_x/p^+-n diodes can be improved if the barrier structure of WSi_x can be modified so as to suppress or retard the interdiffusion of Cu and Si.

C. Effects of N_2 plasma treatment

It was reported that a very thin (4 nm) layer of WSiN formed on the surface of WSi_x by electron cyclotron reso-

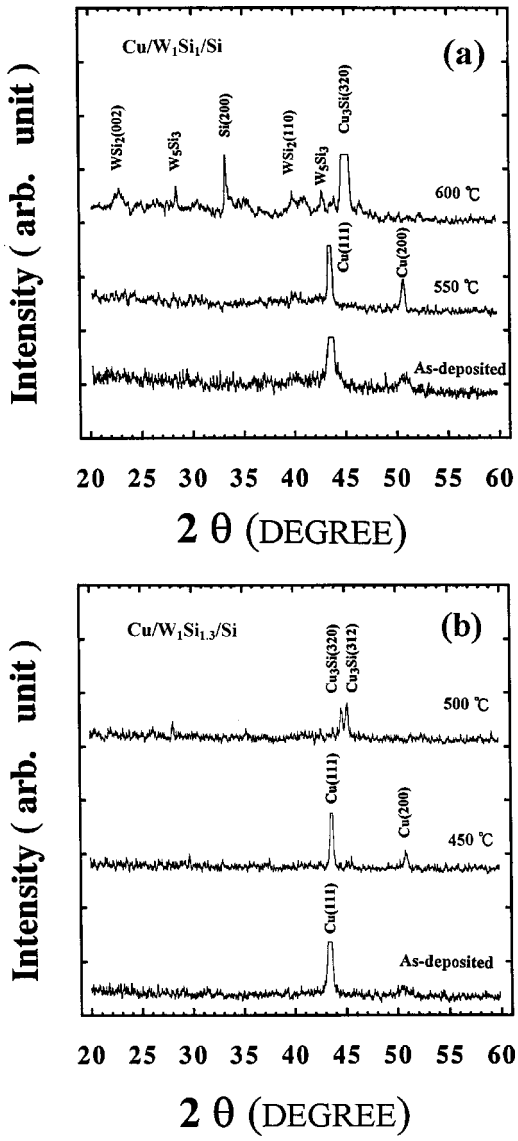

FIG. 5. XRD spectra of (a) $Cu/W_1Si_1/Si$ and (b) $Cu/W_1Si_{1.3}/Si$ samples annealed at various temperatures. The WSi_x layers are 50 nm thick.

nance N_2 plasma nitridation was able to function as an excellent barrier to dopant diffusion.[32] It was also reported that a WN_x layer about 2 nm thick was formed on the chemically vapor deposited tungsten (CVD–W) surface using a capacitively coupled plasma nitridation, and that the WN_x layer

TABLE II. Silicides formed on Cu/Si and $Cu/WSi_x/Si$ samples.

Annealing temperatures (°C)	Layered structure		
	Cu/Si	$Cu/W_1Si_1/Si$	$Cu/W_1Si_{1.3}/Si$
200	Cu_3Si	×[a]	×
450	Cu_3Si	×	×
500	Cu_3Si	×	Cu_3Si, W_5Si_3
550		Cu_3Si	Cu_3Si, W_5Si_3
600		Cu_3Si, W_5Si_3, WSi_2	Cu_3Si, W_5Si_3, WSi_2
650		Cu_3Si, WSi_2	Cu_3Si, WSi_2

[a]"×" indicates no observation of silicide phase.

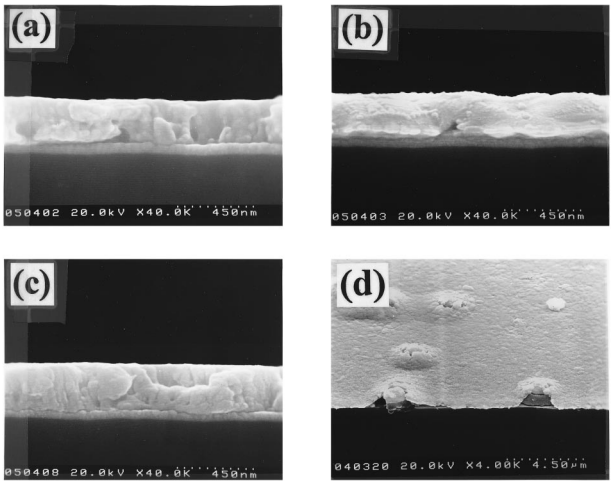

FIG. 6. Cross-sectional view SEM micrographs of $Cu/W_1Si_1/p^+-n$ diodes (a) as-deposited sample and (b) 500 °C annealed sample; SEM micrographs of $Cu/W_1Si_{1.3}/p^+-n$ diodes; (c) cross-sectional view of as-deposited sample; and (d) oblique view of 500 °C annealed sample.

effectively suppressed the increase in resistance of thermally annealed Al/CVD–W/Si interconnects.[33] In addition, we found in a previous study that the barrier effectiveness of a 450-nm-thick selective CVD–W film in the structure of Al/CVD–W/Si can be significantly improved by exposing the W film in an *in situ* N_2 plasma prior to the Al metallization.[34,35] In this study, we insert a very thin WSiN layer between Cu and WSi_x layers to make a structure of $Cu/WSiN/WSi_x/p^+-n$ junction diodes so as to suppress the undesirable interdiffusion between Cu and Si, and thus improve the thermal stability of the junction diodes. The very thin WSiN layer (shown latter in Fig. 8) was formed via an *in situ* N_2 plasma treatment on the surfaces of WSi_x layers.

1. Electrical measurements

Figure 7 shows the statistical distributions of reverse bias current density for the $Cu/WSiN/W_1Si_1/p^+-n$ and $Cu/WSiN/W_1Si_{1.3}/p^+-n$ junction diodes annealed at various temperatures. All the $Cu/WSiN/W_1Si_1/p^+-n$ junction diodes retained their integrity after annealing at temperatures up to 600 °C, and a large majority of the diodes still remained stable even after annealing at 650 °C [Fig. 7(a)]. This is more than 100 °C improvement in thermal stability over the $Cu/W_1Si_1/p^+-n$ junction diodes [Fig. 4(b)], and is attributed to the very thin (about 5 nm) WSiN layer formed on the WSi_x surfaces by the N_2 plasma treatment, as confirmed by the AES depth profiles shown in Fig. 8. It turned out that the very thin WSiN layer suppressed the diffusion of Cu, thus, the formation of Cu_3Si was retarded and the accelerated crystallization of WSi_x layers was suppressed, which in turn resulted in the improvement of thermal stability for the junction diodes.

For the $Cu/WSiN/W_1Si_{1.3}/p^+-n$ junction diodes, the devices remained stable after annealing at temperatures up to 500 °C, deteriorated slightly after annealing at 550 °C, and failed completely upon annealing at 600 °C [Fig. 7(b)]. This

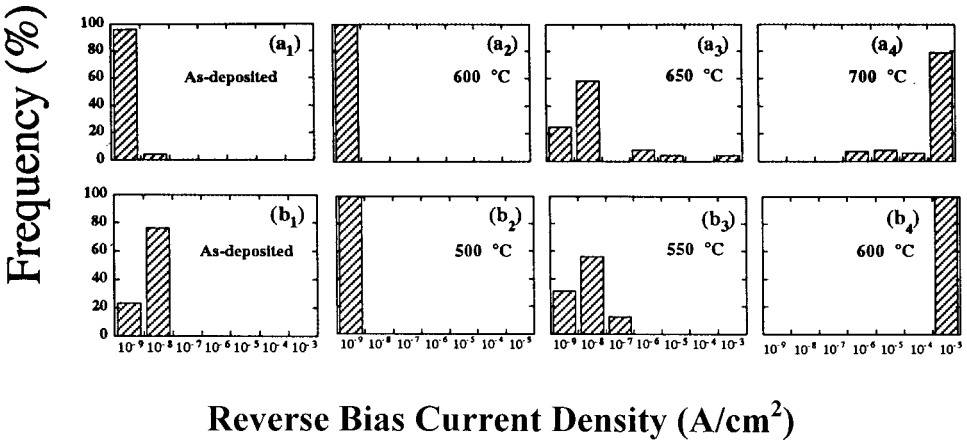

FIG. 7. Histograms showing statistical distributions of reverse bias current density for (a) Cu/WSiN/W_1Si_1/p^+-n and (b) Cu/WSiN/$W_1Si_{1.3}$/p^+-n junction diodes annealed at various temperatures. The WSi_x layers are 50 nm thick.

is an obvious improvement over the Cu/$W_1Si_{1.3}$/p^+-n junction diodes without N_2 plasma treatment [Fig. 4(c)]. However, it is clear that the barrier capability of WSiN/$W_1Si_{1.3}$ bilayer is inferior to that of WSiN/W_1Si_1 bilayer. Failure of the WSiN/WSi_x barrier bilayers might be correlated with the crystallization temperature of WSi_x layers, which decreased with increasing Si/W atomic ratio in the WSi_x layers (Fig. 3).

2. Sheet resistance measurements and XRD analyses

The normalized change in sheet resistance of annealed sample is defined as

$$\frac{\Delta R_S}{R_S}\% = \frac{R_{S_{\text{after anneal}}} - R_{S_{\text{as-deposited}}}}{R_{S_{\text{as-deposited}}}} 100\%.$$

Figure 9 shows the change in sheet resistance of Cu/WSi_x/Si and Cu/WSiN/WSi_x/Si samples annealed at various temperatures. All WSi_x layers were 50 nm thick. The thermal stability of the Cu/W_1Si_1/Si samples reached 550 °C; however, a drastic increase in sheet resistance was found after annealing at 600 °C [Fig. 9(a)], implying failure of the Cu/W_1Si_1/Si structure. For the Cu/$W_1Si_{1.3}$/Si samples, the sheet resistance remained unchanged only up to 450 °C, and it increased drastically after annealing at 500 °C. The Cu/WSi_x/Si structure with a WSi_x barrier layer deposited at higher SiH_4/WF_6 flow ratios was obviously less thermally stable. The sheet resistance for all samples of Cu/WSiN/WSi_x/Si remained stable up to 650 °C, as shown in Fig. 9(b). Comparing these results with those of Cu/WSi_x/Si samples shown in Fig. 9(a), we found that the barrier effectiveness of WSi_x layers was improved significantly by forming a thin layer of WSiN on the surfaces of WSi_x via an *in situ* N_2 plasma treatment.

Figure 10 shows the XRD spectra of the Cu/WSiN/W_1Si_1/Si samples after annealing at various temperatures. Instead of the formation of various silicides for the 600 °C annealed Cu/W_1Si_1/Si samples [Fig. 5(a)], no silicide phase was detected for the Cu/WSiN/W_1Si_1/Si samples annealed at 600 °C. This indicates that the accelerated crystallization of WSi_x layers in contact with a polycrystalline Cu overlayer was suppressed by the presence of a thin WSiN layer sandwiched between the Cu and WSi_x layers. It has been reported that a uniform ultrathin (<1 nm) WSiN barrier layer can be formed at the interface of WN/poly-Si by thermal annealing, and the WSiN layer was able to suppress the silicidation reaction between W and poly-Si up to 800 °C.[36] In this study, the very thin but much chemically and thermally stable WSiN layer contributed to retarding the diffusion of copper and suppressing the accelerated crystallization of WSi_x; thus, the barrier effectiveness of the amorphous CVD–WSi_x layers is significantly improved.

3. SEM observations

Figure 11 shows SEM micrographs for the Cu/WSiN/W_1Si_1/p^+-n junction diodes before and after thermal annealing at various temperatures. The barrier structure remained unchanged after annealing at temperatures up to 600 °C [Fig. 11(b)]. After annealing at 650 °C, some of the diodes were degraded while the others remained intact [Fig. 7(a)]. For the diodes that remained intact after annealing, the cross-sectional SEM micrograph shows that the barrier structure remained unchanged [Fig. 11(c)]. Upon annealing at 700 °C, many large openings were found on the diodes' surfaces, and the fully developed Cu_3Si precipitates exhibiting a feature of inverted pyramid shape bounded by Si {111} planes were also observed [Fig. 11(d)]. Thus, failure of the WSiN/W_1Si_1 barrier bilayers was likely associated with these highly localized precipitates, which were presumably caused by the diffusion of Cu through the weak points (such

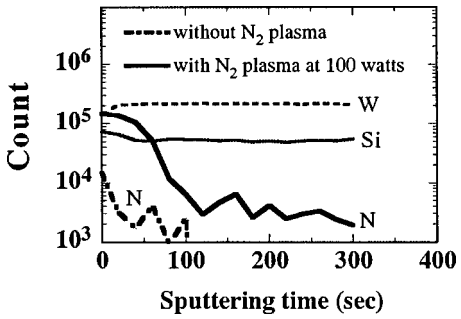

FIG. 8. AES depth profiles of WSi_x/Si samples with and without N_2 plasma treatment showing the difference in nitrogen distribution; the sputtering rate was determined to be about 0.1 nm/s.

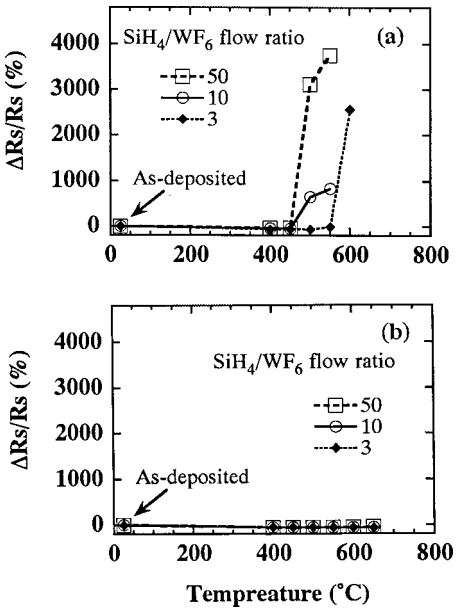

FIG. 9. Change in sheet resistance vs annealing temperature for (a) $Cu/WSi_x/Si$ and (b) $Cu/WSiN/WSi_x/Si$ samples with the WSi_x layers deposited at various SiH_4/WF_6 flow ratios.

as stress-induced microcracks and grain boundaries of the crystallized W_1Si_1 layer) in the thermally annealed barrier layers. The results of SEM observations further confirm that the thermal stability of the $Cu/WSi_x/Si$ structure can be improved significantly by forming a thin layer of WSiN on the surfaces of WSi_x via an *in situ* N_2 plasma treatment. The thermal stability temperatures of WSi_x-based barrier layers determined by various techniques of measurement and/or analysis are summarized in Table III.

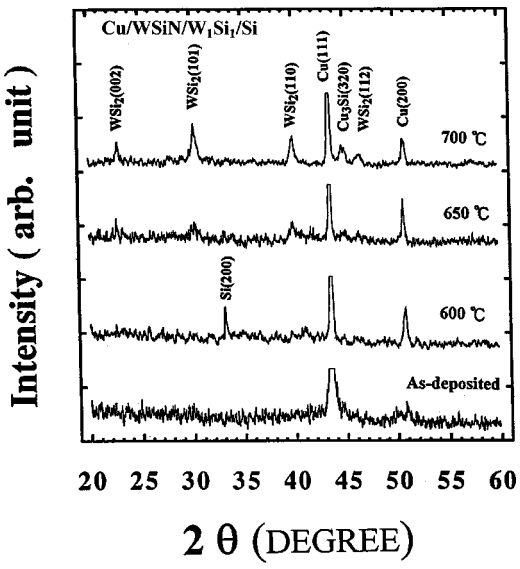

FIG. 10. XRD spectra of $Cu/WSiN/W_1Si_1/Si$ sample annealed at various temperatures.

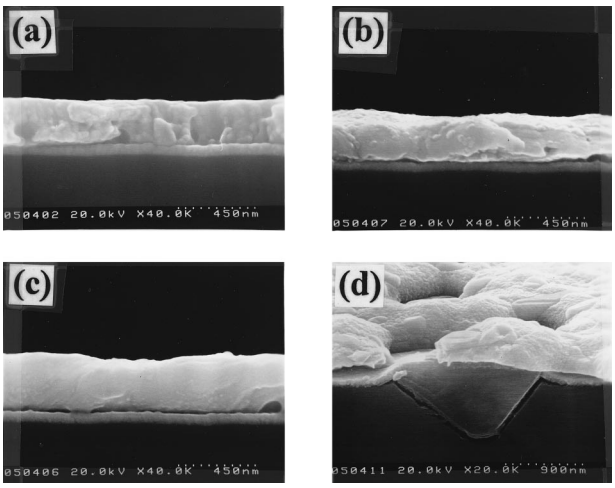

FIG. 11. Cross-sectional and oblique view SEM micrographs for the $Cu/WSiN/W_1Si_1/p^+-n$ junction diodes (a) as-deposited, and (b) 600, (c) 650, and (d) 700 °C annealed.

IV. SUMMARY

The thermal stability of thin amorphous CVD–WSi_x layers, with and without N_2 plasma treatment, was investigated with respect to the capability of diffusion barrier between Cu and Si substrate. We found that the barrier effectiveness depended on the composition of WSi_x films. The amorphous WSi_x films deposited with higher flow ratios of SiH_4/WF_6 have higher Si/W atomic ratios as well as lower crystallization temperatures; thus, the barrier effectiveness of the WSi_x films was lowered. For the 50-nm-thick W_1Si_1 layers deposited with a SiH_4/WF_6 flow ratio of 3, the $Cu/W_1Si_1/p^+-n$ junction diodes were able to sustain a 30 min thermal annealing at temperatures up to 500 °C without causing degradation to the electrical characteristics. The thermal stability was lowered to 450 °C for the $Cu/W_1Si_{1.3}/p^+-n$ junction diodes using the $W_1Si_{1.3}$ barrier layers deposited with a SiH_4/WF_6 flow ratio of 50. The barrier capability of WSi_x films can be efficiently improved by an *in situ* N_2 plasma treatment. The N_2 plasma treatment produced a very thin layer of WSiN on the surfaces of WSi_x layers, and the $WSiN/WSi_x$ bilayers not only suppressed the diffusion of Cu efficiently, but also prevented the accelerated crystallization of WSi_x layers in case of direct contact with the Cu overlayers, resulting in improvement on barrier capability. With an *in situ* N_2 plasma

TABLE III. Thermal stability temperatures of WSi_x-based barrier layers determined by different techniques of measurement/analysis.

Measurement and/or analysis methods	Barrier layers			
	W_1Si_1 (°C)	$W_1Si_{1.3}$ (°C)	$WSiN/W_1Si_1$ (°C)	$WSiN/W_1Si_{1.3}$ (°C)
Reverse current	500	450	600	500–550
Sheet resistance	550	450	650	650
XRD	550	450	600	600
SEM	500	450	600–650	500–550

treatment applied to the W_1Si_1 barrier, the $Cu/WSiN/W_1Si_1/p^+-n$ junction diodes were able to remain intact up to at least 600 °C.

ACKNOWLEDGMENT

This work was supported by the National Science Council (ROC) under Contract No. NSC87-2215-E-009-72.

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