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Improvement of Polysilicon Oxide Integrity Using NF_3-Annealing

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We report a method to improve the polysilicon oxide integrity by using NF_3-annealing. Incorporating with stronger Si–N and Si–F bonds at the polysilicon/ polyoxide interface, significant improvements are found in terms of roughness, breakdown strength, charge-to-breakdown, and stress-induced-leakage-current.

KEYWORDS: polyoxide, NF_3-annealing, nitrogen, fluorine, SILC

1. Introduction

For nonvolatile memories such as erasable-programmable read-only memory (EPROM), electrical-erasable programmable read-only memory (EEPROM), and Flash, thermal oxides grown on n^+ polysilicon (polyoxides) have been used as the interdielectrics. Requirements of the polyoxides include low leakage current and high electric breakdown field (E_{bd}) to achieve a long charge retention time. However, polyoxides exhibit lower E_{bd} and higher leakage current than oxides grown on single crystal silicon due to surface roughness caused by the enhanced oxidation at polysilicon grain boundaries. Recent studies show that the reliability of MOS and polyoxide capacitors can be improved by introducing proper amounts of fluorine.[1–3] It also reported that the N_2O-grown and N_2O-annealing polyoxides have better electrical performance than O_2-grown polyoxide, which attributes to the nitrogen incorporation at the polysilicon/polyoxide interface.[4,5] Therefore, in this paper, NF_3-annealing is proposed to achieve the advantages of both nitrogen and fluorine simultaneously. By using optimized NF_3 flow-rate, it can be expected to improve the polyoxide integrity. As compared to the ion-implantation, this method provides a low cost and high throughput for mass production.

2. Experimental

The n^+-polysilicon/polyoxide/n^+-polysilicon capacitors were fabricated on the p-type (100) silicon wafers. First, a 100 nm-thick buried oxide was thermally wet oxidized at 1000°C. Then the polysilicon layer (bottom polysilicon) with a thickness of 300 nm was deposited and subsequently doped with $POCl_3$ at 875°C to obtain a sheet resistance of 40–60 Ω/□. The p-glass was stripped off and then an 83 Å polyoxide was grown at 900°C in dilute ($N_2 + O_2$) ambient. After that, a 300 nm-thick top polysilicon layer was deposited, followed by annealing in the diluted NF_3 gas. Samples were annealed in NF_3 at 600°C with pressure of 260 mTorr for different time, 10 to 30 minutes in a low-pressure chemical-vapor-deposition (LPCVD) system. After optimization, the flow rates for N_2 and NF_3 are set at 200 and 3 sccm, respectively. Then top polysilicon was doped by $POCl_3$ as the n^+-polysilicon gate electrode at 875°C for 1 hour. After defining the top gate pattern, a passivation oxide was deposited by plasma enhanced chemical vapor deposition (PECVD) and contact holes were opened. Finally, Aluminum was sputtered, patterned, and sintered at 350°C for 40 minutes.

3. Results and Discussion

Figure 1 shows curves of current density vs electric field. The electric field is defined as V_g/T_{ox}, where V_g is the gate voltage. The breakdown field, E_{bd}, increases with the introduction of NF_3-annealing, which reaches a maximum of 15 MV/cm for 20 minutes case. The inset in Fig. 1 shows the root-mean-square roughness measured by the atomic force microscope (AFM) of bottom polysilicon with different NF_3-annealing time. The value of surface roughness decreases as introduction of NF_3 and reaches to a minimum for 20-min annealing. These results show that 20-min annealing is the optimized condition to obtain the smoothest surface of the bottom polysilicon, and results in a highest E_{bd} in return. For a longer annealing time, i.e., 30-min, excessive fluorine and/or nitrogen atoms break the Si–O–Si bonds and create non-bridging oxygen defects. Figure 2 shows gate voltage shift under constant current stressing at 100 μA/cm^2 for these four samples. NF_3-annealing samples show a smaller charge trapping-rate than control sample. This implies NF_3-annealing samples have better immunity to electron trapping than control.

As considering the reliability of polyoxide in nonvolatile memories, charge-to-breakdown (Q_{bd}) is to guaranty long read/write cycles. In the conventional polyoxide fabrication, Q_{bd} values are very small (in the range of 0.01 to 0.1 C/cm^2)

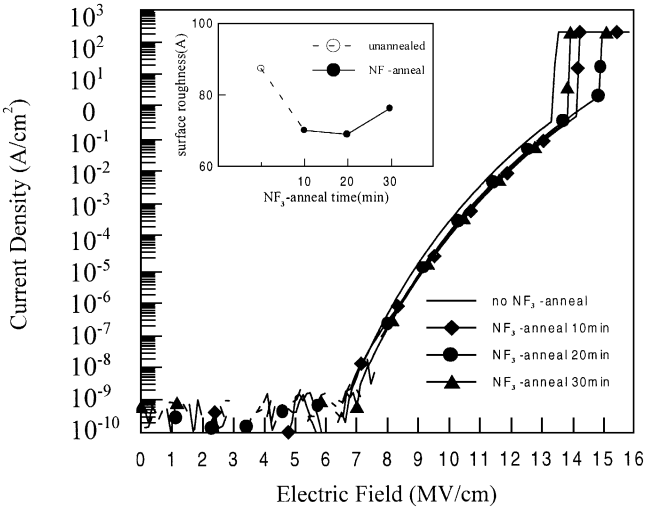

Fig. 1. The J-E characteristics of polyoxides with/without NF_3 annealed for positive top-gate bias. The inset is surface roughness for these four samples.

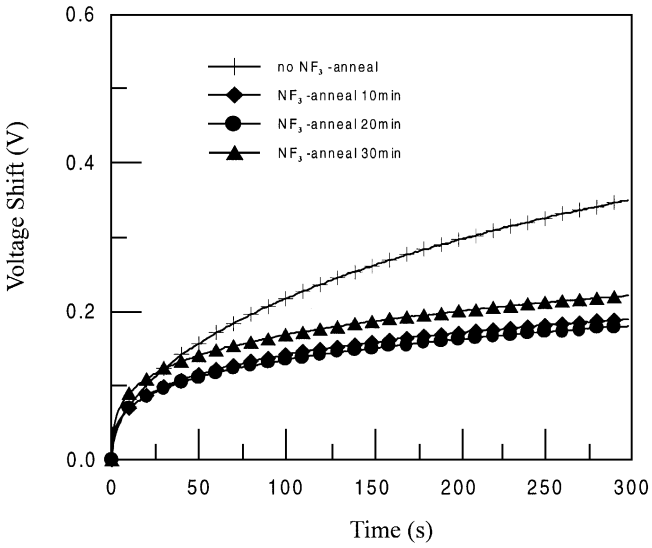

Fig. 2. The curves of gate voltage shifts versus stress time under a constant current stressing at 100 μA/cm^2.

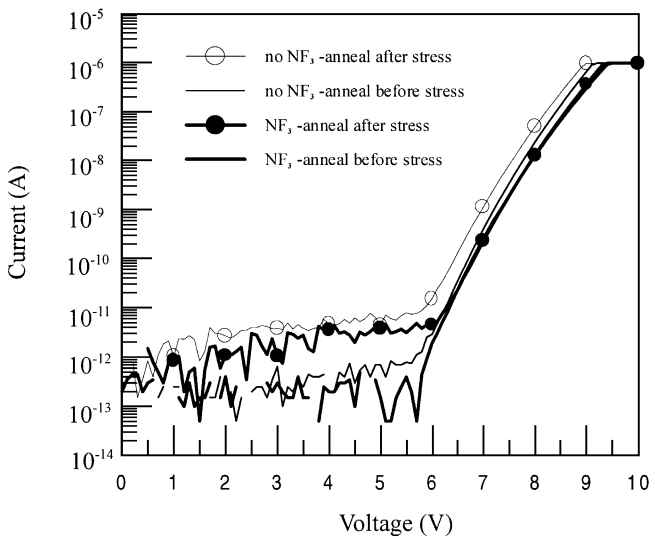

Fig. 4. The fresh and stressed I-V curves of the stress-induced-leakage-current (SILC) for samples without NF_3-annealing and the 20-min. NF_3-annealing. The injected charge density is 0.05 C/cm^2.

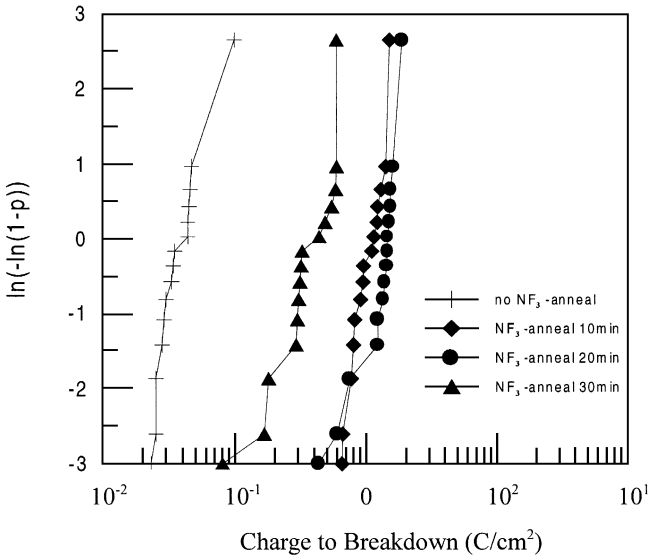

Fig. 3. The Weibull plots of the charge-to-breakdown for NF_3-annealing polyoxide in different time at room temperature of 25°C. The stress current density is 10 mA/cm^2.

due to surface roughness and non-uniform polyoxide thickness. Figure 3 shows the Q_{bd} for these four samples. With NF_3 treatments, Q_{bd} increases significantly. Besides the improvement on roughness as mentioned in Fig. 1, the improved integrity is also due to incorporation of nitrogen and fluorine atoms which relax the interface stress.[2,4] It is found that Q_{bd} greater than 1 C/cm^2 can be obtained as NF_3 annealing time is larger than 20-min. Finally the stress-induced-leakage-current (SILC) was investigated. Mechanism of SILC could be explained by the stress-induced weak sports with a lowing barrier height, the trap-assisted tunneling by the neutral electron trap filling and emptying, and the positive charge assisted tunneling.[6–8] The fresh and the after stressed I–V curves are shown in Fig. 4. It is seen that the SILC of the NF_3-annealing sample was smaller than that of the control sample. Once again, the stronger Si–F and Si–N bonds at the polysilicon/polyoxide interface resulting from the NF_3 annealing made polyoxides less vulnerable than the control sample under the electrical stressing. In this study, all samples were measured with the positive-gate bias and the results of the negative-gate bias were similar to those obtained from the positive-gate bias.

4. Conclusions

NF_3-annealing method had been demonstrated to improve the polyoxide integrity. The breakdown field up to 15 MV/cm and charge-to-breakdown more than 1 C/cm^2 can be obtained using NF_3-annealing. Incorporating with stronger Si–N and Si–F bonds at the polysilicon/polyoxide interface, significant improvements are found in terms of roughness, breakdown strength, charge-to-breakdown, and stress-induced-leakage-current.

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