Electrochemical and Solid-State Letters, **3** (5) 235-238 (2000) 235
S1099-0062(99)10-107-X CCC: $7.00 © The Electrochemical Society, Inc.

Improvements of Amorphous-Silicon Inverted-Staggered Thin-Film Transistors Using High-Temperature-Deposited Al Gate with Chemical Mechanical Polishing

Po-Sheng Shih,[a,*] Ting-Chang Chang,[b,c,,z] Chung-Yu Liang,[d] Tiao-Yuan Huang,[a,b] and Chun-Yen Chang[a]**

[a]*Institute of Electronics, National Chiao Tung University, Taiwan*
[b]*National Nano Device Laboratories, Hsin-Chu 300, Taiwan*
[c]*Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan*
[d]*Instiutte of Optical Science, National Central University, Taiwan*

Chemical mechanical polished Al (CMP-Al) films deposited at various temperatures were explored as the gate electrodes of amorphous-silicon (a-Si:H) inverted-staggered thin-film transistors (TFTs) for the first time. Although the surface roughness of the as-deposited Al films increased with increasing deposition temperature, Al films deposited at higher temperature were more robust to hillock formation during subsequent annealing. To take advantage of the better hillock suppression properties, CMP is employed to reduce the inherently large surface roughness of these high-temperature-deposited Al films. Our results show that the electrical characteristics of the TFTs are significantly improved. Specifically, the threshold voltage is reduced from 2.37 to 1.43 V, the mobility is improved from 0.32 to 1.36 cm^2/V s, and the subthreshold swing is improved from 0.72 to 0.58 V/decade as the Al deposition temperature is increased from 25 to 400°C.
© 2000 The Electrochemical Society. S1099-0062(99)10-107-X. All rights reserved.

Manuscript submitted October 28, 1999; revised manuscript received December 24, 1999. Available electronically March 9, 2000.

Amorphous silicon (a-Si:H) thin film transistors (TFTs) are widely used as the pixel switching elements in many state-of-the-art active-matrix liquid crystal displays (AMLCDs). For most AMLCD applications, the so-called invert-staggered device structure with a bottom gate is employed.[1] In the inverted-staggered structure, the morphology of gate insulator (*e.g.,* SiN_x) and thus the interface roughness between the gate insulator and the active amorphous silicon layer (*i.e.,* SiN_x/a-Si:H) is strongly influenced by the morphology of the bottom-gate metallurgy. Because the bottom-gate is deposited prior to the formation of gate insulator and the active amorphous silicon layer, it is susceptible to hillock formation during subsequent high-temperature fabrication processes, causing inevitable surface roughness. An excessive surface roughness of the bottom gate metallurgy might increase the interface trap density and worsen the roughness scattering at the SiN_x/a-Si:H interface, leading to mobility degradation and device instability.

To alleviate these problems, refractory metals such as Cr, Mo, and Ta, have been proposed as potential bottom-gate material. Because of their higher thermal stability and hence higher resistance to hillock formation, the resultant surface roughness can be lessened. However, this approach suffers from the relatively high resistivities (> 10 μΩ cm) inherent in refractory metals, resulting in intolerable RC gate delays that limit the feasible AMLCD size to no more than 15-20 in. [2] Among the conducting metals, Cu has the lowest resistivity (*i.e.,* 1.5-2 μΩ cm). However, it suffers from poor adhesion to glass substrate, easy surface oxidation,[3] and high reactivity during the plasma-enhanced chemical vapor deposition (PECVD) process, making it unsuitable as the bottom-gate material for TFTs. On the other hand, sputter-deposited Al alloy depicts high hillock suppression, and lower electrical resistivity than refractory metals, but it still falls short on meeting the requirement for advanced high-performance AMLCD applications because of their relatively high electrical resistivity of about 10 μΩ cm. Although adding group VIII transition elements[5] or rare-earth metal elements[6] can somewhat reduce its resistivity, the achievable resistivity is still too large for most high-performance AMLCD applications.

In contrast, pure Al depicts a desirable low electrical resistivity of 2.7 μΩ cm. However, it suffers instead from the inferior thermal and mechanical stabilities. Hillocks are known to form on Al surface during LCD fabrication.[7] The microstructure of Al is dependent on deposition temperature. Since the hillock formation is strongly related to the microstructure,[8] the deposition temperature of Al is expected to play a crucial role in hillock formation. Therefore, the electrical characteristics of a-Si:H TFTs should also be related to the Al gate deposition temperature. However, little work has been reported regarding the effects of Al deposition temperature on the electrical characteristics of a-Si:H inverted-staggered TFTs.

Concurrently, chemical mechanical polishing (CMP) has recently been employed for global planarization of the silicon wafer surface for very large scale integrated circuits.[9] More recently, CMP has also been applied for improving the surface morphology of polysilicon floating-gate for nonvolatile memory applications and also for improving the surface morphology of the active channel polysilicon channel layer in polysilicon TFTs.[10] In this paper, we report, for the first time, the combined effects of high deposition temperature and chemical mechanical polishing of aluminum bottom gate on the electrical characteristics of inverted-staggered TFTs.

Experimental

Inverted-staggered a-Si:H TFTs with CMP aluminum gate deposited at various temperatures were fabricated for the first time. Briefly, silicon wafers coated with a 500 nm thermal oxide were used as the starting substrates. Then, Al films with thickness of 500 nm were sputter-deposited with MRC primus 2500 sputter using Ar as the sputtering gas. The pressure and power during sputtering were 1 mTorr and 15 kW. Subsequently, CMP was carried out on a Westech 372M polisher to smooth the Al films to a final thickness of 400 nm. Polished pads evaluated in this work were Rodel Politex regular E. Rodel R200-T3 was chose as the carrier film. For a one-step polishing process, polishing parameters like pressure, platen and carrier rotary speeds, back pressure, and slurry flow rate were set to be 5 psi, 60 rpm, 65 rpm, 2 psi, and 150 mL/min, respectively. Slurries were formulated with 0.3 μm α-Al_2O_3 abrasive, 5% phosphoric acid, and 3% hydrogren peroxide in acidic aqueous solution. Slurry pH was set at 2 that was buffered with 0.1 M citric acid and adjusted with KOH. Afterward, the bottom-gate electrodes were

* Electrochemical Society Student Member.
** Electrochemical Society Active Member.
z E-mail: tcchang@ndl.gov.tw

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

S1099-0062(99)10-107-X CCC: $7.00 © The Electrochemical Society, Inc.

defined by a photolithography step and wet chemical etching. Since the sidewall of Al gates were sloped after wet chemical etching (which is isotropic), the sidewall coverage problems caused by the successive layers can be eliminated. Next, a 250 nm silicon nitride (SiN_x) layer was deposited at 300°C for 30 min by plasma enhanced chemical vapor deposition (PECVD) to serve as the gate insulating layer. Then, a 200 nm undoped a-Si:H film and a 50 nm n^+ a-Si:H film were deposited successively at 250°C without breaking vacuum for 24 and 6 min, respectively. The active device layer was then defined by photolithography and dry etching. Afterward, a 300 nm Al metal layer was deposited by thermal evaporation, and patterned by photolithography and subsequent wet etching to form the source and drain electrodes. Finally, the unwanted n^+ layer between the two source and drain electrodes was removed by dry etching. All devices were annealed at 200°C in N_2 ambient for 20 min to form good ohmic contacts.

Results and Discussion

In order to investigate the temperature dependence of hillock suppression, the as-deposited Al films without chemical mechanical polishing were annealed at 300°C for 30 min. Atomic force microscopy (AFM) was used to examine the surface roughness of as-deposited and 300°C annealed films. The results are shown in Fig. 1 for Al films as a function of deposition temperature. It can be seen that the surface roughness of the as-deposited Al films (solid line) increases significantly from 3.21 to 20.09 nm as the deposition temperature increases from room temperature to 400°C. This is consistent with the larger grain size and therefore rougher surface with increasing deposition temperature. In contrast, the dependence of surface roughness on the deposition temperature becomes irregular with deposition temperature for 300°C annealed films (dashed line), with the film deposited at 200°C showing the largest surface roughness.

Because hillock formation leads to Al surface roughness, the degree of surface roughness is a good indicator of hillock resistance. Figure 2 shows the increments in surface roughness of Al films caused by the 300°C thermal annealing. It can be seen that the roughness increment is reduced with increasing deposition temperature. This implies that the hillock resistance is enhanced with higher deposition temperature. Note that the increment in surface roughness is 11.57 nm for Al film deposited at room temperature and is only 0.28 nm for the film deposited at 400°C. The improvement of hillock resistance with temperature is quite significant. It is believed that the relaxation of compressive stress by lateral diffusion of Al atoms along the grain boundaries and its precipitation on the surface are responsible for the hillock formation.[7] With increasing deposition temperature, the grain size increases. Therefore the number of grain boundary and the lateral diffusion of Al atoms are reduced, resulting in more robust hillock resistance. In addition, increasing Al(111) peak density is also known to enhance hillock resistance.[8] This is consistent with our previous finding that a higher Al deposition temperature results in higher Al(111) peak density.[11]

Despite their better hillock resistance, the drawback of high-temperature-deposited Al films is their inherently larger as-deposited surface roughness, as shown in Fig. 1, which deteriorates the performance of inverted-staggered a-Si:H TFT. This drawback, however, can be cleverly overcome by employing chemical mechanical polishing technique to polish the high-temperature-deposited Al films. The scanning electron microscopy (SEM) images of Al films deposited at 400°C before and after chemical mechanical polishing are shown in Fig. 3a and b, respectively. It is clear that the Al film surface becomes much smoother after chemical mechanical polishing. This result is further confirmed with the three-dimensional AFM images, as shown in Fig. 4. There are inevitable scratches on CMP-Al films. The average surface roughness after chemical mechanical polishing is reduced to around 3 nm. We believe the scratches and surface roughness could be further reduced by further optimization of the polishing condition.

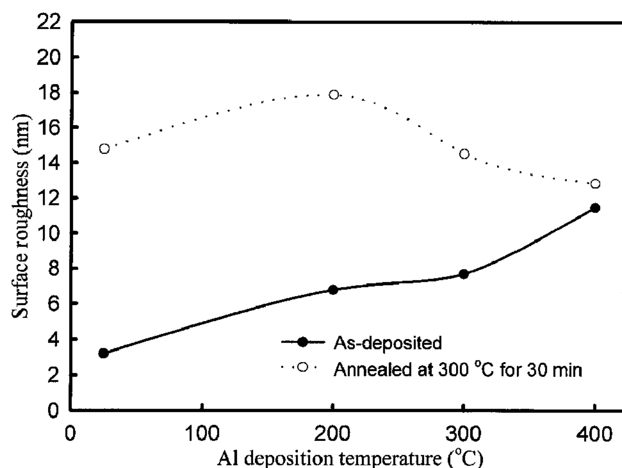

Figure 1. Root mean square (rms) surface roughness as a function of deposition temperature for as-deposited (solid line) and 300°C annealed (dashed line) Al films.

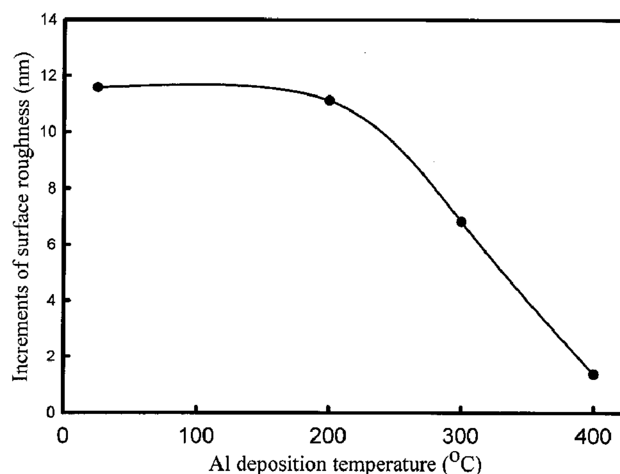

Figure 2. RMS surface roughness increment after 300°C annealing for Al films as a function of deposition temperature. The annealing time was 30 min.

Besides, our experimental results show that the roughness increment and thus the hillock resistance of CMP-Al is almost identical to that of as-deposited Al. Figure 5 shows the transfer characteristics of a-Si:H TFTs with CMP-Al gate (referred to as polished TFT hereafter) deposited at various temperatures. Note that the leakage current is below the detection limit of our measurement system (*i.e.,* 10^{-13} A). Specifically, for polished TFT with Al gate deposited at 400°C, ON current (I_{ON}) is around 10^{-5} A (measured at a gate voltage, $V_g = 20$ V), leakage current (I_{OFF}) is around 10^{-13} A, and I_{ON}/I_{OFF} ratio ~108. While for polished TFT with Al gate deposited at room temperature, I_{ON} depicts a relatively small value of 2.8 x 10^{-6} A and I_{ON}/I_{OFF} ratio ~2.8 x 10^7. Detailed device characteristics are summarized in Table I. Device characteristics of a-Si:H TFTs with unpolished Al gates (referred to as unpolished TFT hereafter) are also shown for comparison. The mobility and threshold voltage are determined from transistor characteristics in the saturation region by plotting $(I_{ds})^{1/2}$ *vs.* V_g. It is clear that the threshold voltage, mobility, and subthreshold swing all improve monotonically with increasing Al deposition temperature. However, the improvements in unpolished TFTs with increasing deposition temperature are less pronounced than those in polished TFTs, which is believed to be due to the inherently larger surface roughness for unpolished high-temperature-deposited Al films. Note

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

S1099-0062(99)10-107-X CCC: $7.00 © The Electrochemical Society, Inc.

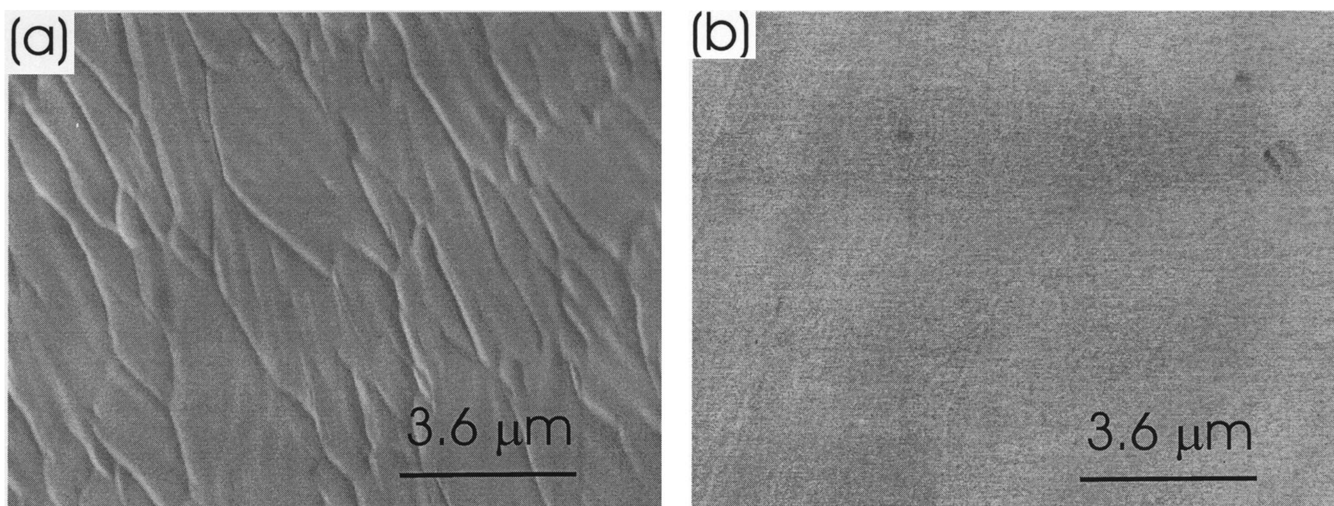

Figure 3. SEM images of Al films (a) before and (b) after CMP. The deposition temperature was 400°C.

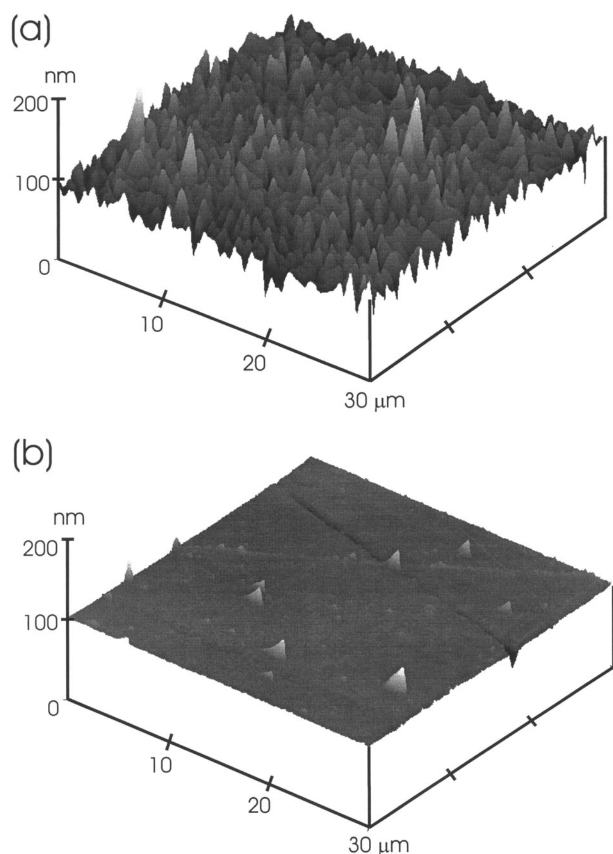

Figure 4. Three-dimensional AFM images of Al films (a) before and (b) after CMP. The deposition temperature was 400°C.

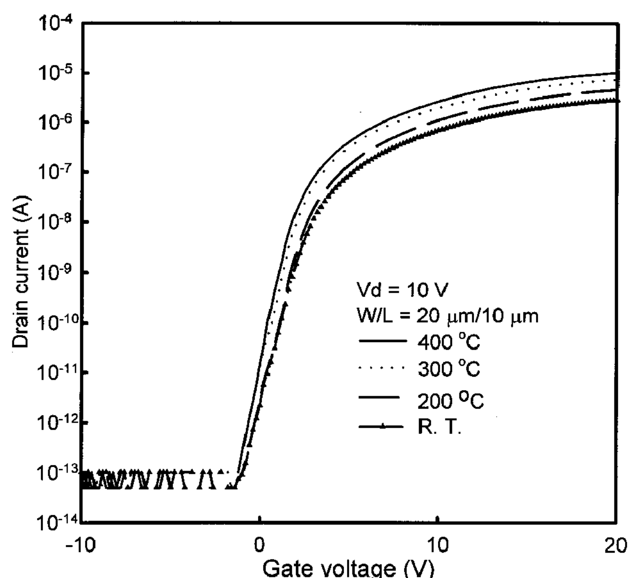

Figure 5. Transfer characteristics of inverted-staggered a-Si:H TFTs with CMP-Al gates deposited at various temperatures.

that for Al gate deposited at room temperature, the device performance in unpolished TFT is slightly better than that of polished TFT. This is because the surface roughness of Al film deposited at room temperature is reduced from 3.21 to 3 nm after chemical mechanical polishing. As a result, the device characteristic improvement due to planarization of Al gate surface after chemical mechanical polishing is overwhelmed by the scratches on Al gate surface caused by chemical mechanical polishing process, leading to poor device characteristics of polished TFT with room-temperature-deposited Al.

Two possible mechanisms can be used to explain the observed device characteristics improvements with increasing Al deposition temperature. The first is the reduced roughness scattering and interface trap density with increasing Al deposition temperature. The SiN_x surface roughness, which is directly influenced by the morphology of underlying Al gate, is reduced with increasing Al deposition temperature. The mobility reduction due to surface roughness scattering, as well as threshold voltage and subthreshold swing increments due to interface traps have been observed in the case of Si/SiO_2 interface. For the a-Si:H/SiN_x interface, it is reasonable to assume that similar effect exists. The other possible mechanism is a better a-Si:H film quality grown at a smoother a-Si:H/SiN_x interface with increasing Al deposition temperature. This is because on a rougher SiN_x surface, there exists many active sites, which prevent the surface diffusion of SiH_3 precursors during the depositon of a-Si:H. Thus, it is likely that the initial a-Si:H growth layer has a larger defect density on a rougher SiN_x film.[12]

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

S1099-0062(99)10-107-X CCC: $7.00 © The Electrochemical Society, Inc.

Table I. Summary of threshold voltage, mobility, subthreshold swing, and ON/OFF current ratio for devices with polished and unpolished Al gates.

Deposition temperature (°C)		V_{th} (V)	Mobility (cm^2/v s)	Subthreshold swing (V/decade)	ON/OFF current ratio
Room temperature	Polished	2.37	0.32	0.72	2.85×10^7
	Unpolished	2.2	0.38	0.7	3.29×10^7
200	Polished	2.03	0.59	0.68	4.59×10^7
	Unpolished	2.0	0.41	0.69	3.53×10^7
300	Polished	1.71	0.98	0.63	7.32×10^7
	Unpolished	1.9	0.56	0.67	4.82×10^7
400	Polished	1.43	1.36	0.58	1.02×10^8
	Unpolished	1.6	0.69	0.64	4.90×10^7

Conclusions

We have successfully applied, for the first time, CMP-Al bottom gate deposited at various temperatures to fabricate a-Si:H inverted-staggered TFTs. Our results clearly show that by employing a higher Al deposition temperature and CMP to the Al bottom gate, significant improvement in the a-Si:H TFT characteristics can be achieved. The use of a CMP-Al bottom gate deposited at high deposition temperature (*e.g.,* 400°C) thus appears to be quite promising for future large-area AMLCD applications.

Acknowledgments

The authors express their appreciation to the staff of Semiconductor Research Center, National Chiao Tung University, for their technical support. This work is supported in part by the National Science Council of the Republic of China (NSC89-2215-E-009-007 and NSC-89-2215-E-110-001).

National Chiao Tung University assisted in meeting the publication costs of this article.

References

1. M. J. Powell, *IEEE Trans. Electron. Devices,* **36**, 2753 (1989).
2. W. E. Howard, *J. Soc. Inform. Display,* **3**, 127 (1995).
3. P. M. Fryer, E. Colgan, E. Galligan, W. Graham, R. Horton, L. Jenkins, R. John, Y. Kuo, K. Latzko, F. Libsch, A. Lien, R. Nywening, R. Polastre, M. E. Rothwell, J. Wilson, R. Wisnieff, and S. Wright, in *Flat Panel Display Materials, Proceedings of the 1998 Symposium,* Materials Research Society, p. 37 (1998).
4. T. Onishi, E. Iwamura, and K. Takagi, *Thin Solid Films,* **340**, 306 (1999).
5. T. Onishi, E. Iwamura, K. Takagi, and K. Yoshikawa, *J. Vac. Sci. Technol., A,* **14**, 2728 (1996).
6. S. Takayama and N. Tsutsui, *J. Vac. Sci. Technol., B.,* **14**, 3257 (1996).
7. E. Jwamura, T. Ohnishi, and K. Yoshikawa, *Thin Solid Films,* **270**, 450 (1995).
8. B. C. Martin, C. J. Tracy, J. W. Mayer, and L. E. Hendrickson, *Thin Solid Films,* **271**, 64 (1995).
9. H. Park, Y. J. Cho, J. I. Song, Y. B. Koh, and M. Y. Lee, *Jpn. J. Appl. Phys.,* **37**, 3871 (1998).
10. C. Y. Chang, H. Y. Lin, T. F. Lei, J. Y. Cheng, L. P. Chen, and B. T. Dai, *IEEE Electron Device Lett.,* **17**, 100 (1996).
11. P. S. Shih, T. C. Chang, S. M. Chen, M. S. Feng, D. Z. Peng, and C. Y. Chang, *Surf. Coat. Technol.,* **108-109**, 588 (1998).
12. H. Uchida, K. Takechi, S. Nishida, and S. Kaneko, *Jpn. J. Appl. Phys.,* **30**, 3691 (1991).

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).