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High-Quality Thermal Oxide Grown on High-Temperature-Formed SiGe

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We have developed a high-quality gate oxide on $Si_{0.6}Ge_{0.4}$ with a 30 Å Si top layer. The good oxide integrity comparable to conventional thermal oxide is demonstrated by the low interface trap density of 6.2×10^{10} eV^{-1} cm^{-2}, low oxide charge of 5.8×10^{10} cm^{-2}, small leakage current at 3.3 V of 4.2×10^{-8} A/cm^2, high breakdown field of 13.8 MV/cm, good charge-to-breakdown of 5.2 C/cm^2, and small stress-induced leakage current. This good oxide integrity is directly related to our previously developed SiGe formed by solid phase epitaxy at high temperatures that is stable during thermal oxidation. This simple process is fully compatible with existing very large scale integration technology.
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Gate oxide integrity[1-4] is one of the most important factors for integrating SiGe p-metal oxide semiconductor field effect transistors (p-MOSFET) into current complementary metal oxide semiconductor (CMOS) technology, even though SiGe itself exhibits higher hole mobility, improved current drive capability, and increased packaging density of CMOS circuits. Unfortunately, in spite of the maturely developed SiGe material, the growth of high-quality oxide is still the major challenge for SiGe p-MOSFET. The main issue for achieving high-quality gate oxide is that direct thermal oxidation produces a mixed SiO_2 and GeO_x with degraded oxide quality.[5-7] Furthermore, Ge pileup in the oxide/Si interface is also believed to severely increase the interface trap density. To overcome these problems mentioned above, low-temperature radio-frequency (rf) plasma[8] and electron cyclotron resonance[9,10] techniques are proposed for SiGe oxidation. Although accompanying H_2O vapor anneal favors acceptable interface trap and fixed charge density, it is still difficult to achieve comparable oxide breakdown electric field as conventional thermal oxide and the gate oxide integrity is suspected to degrade by plasma damage. Another technique employs an Si cap layer on SiGe with subsequent plasma-enhanced chemical vapor deposited oxide or low-temperature oxidation (700-750°C).[11-14] Although good oxide charge and interface trap densities are reported, unfortunately, the low-temperature constraint may not only degrade the oxide reliability but also prohibits the source-drain implant activation that will increase both contact resistance and junction leakage.[15] In this work, we propose a simple and inexpensive approach to form high-quality gate oxide on high-temperature-formed $Si_{0.6}Ge_{0.4}$. Because our SiGe is formed by solid phase epitaxy at high temperatures, no low-temperature processing restriction would be imposed and conventional thermal oxidation can be directly applied. To further ensure good oxide integrity, a ~30 Å Si top layer is formed on $Si_{0.6}Ge_{0.4}$ for thermal oxidation. Good oxide quality of 50 Å is evidenced by the comparable properties to conventional Si dioxide (SiO_2) such as leakage current, breakdown electric field, charge-to-breakdown (Q_{BD}), interface trap density, and small stress-induced leakage current (SILC). The biggest advantage of the formed SiGe MOS structure is that its process is completely compatible to current very large scale integration (VLSI) technology.

Experimental

4 in. p-type Si(100) wafers were used in this work with a resistivity of 10 Ω cm. The wafer were cleaned in a 3:1 solution of H_2SO_4 and H_2O_2, a high-purity deionized (DI) water rinse, a 1% HF etch, a DI water rinse, and a final HF vapor passivation. MOS capacitors were fabricated to characterize the oxide quality. After device isolation with a 3000 Å field oxide, a 350 Å SiGe layer with good crystalline quality was first formed in the active region by solid phase epitaxy at 900°C using rapid thermal annealing (RTA). In fact, this process is very similar to form single crystalline $CoSi_2$ on Si.[16] More detailed material characterization can be found in our previous study.[17,18] An amorphous Si is then deposited on the SiGe layer and subsequent 900°C RTA is applied to form the 30 Å Si top layer by solid phase epitaxy. Before gate oxidation, wafers were cleaned again with standard RCA process to avoid any contamination that will strongly affect the oxide quality. Gate oxides of 50 Å were grown by dry O_2 at 900°C followed by a 3000 Å poly-Si deposition with the subsequent n-type doping by phosphorus. Standard contact is formed by aluminum sputtering and sintered at 400°C for 30 min in forming gas. In addition to thermal oxides grown on Si/SiGe, control thermal SiO_2 was also fabricated as references. We have used X-ray diffraction (XRD) to characterize the crystal structure and composition of SiGe. The surface roughness before and after oxidation was observed by atomic force microscopy (AFM). The gate oxide integrity was electrically examined by capacitance-voltage (C-V) measurements, current-voltage (I-V) characteristics, time-dependent dielectric breakdown (TDDB), Q_{BD}, and SILC.

Results and Discussion

We first characterized the composition and material quality of the 30 Å Si/350 Å SiGe by measuring XRD spectra shown in Fig. 1. The composition of this SiGe layer is obtained from its relative peak position to Si and a 40% Ge is calculated in the alloy. The strong and sharp diffracted peak comparable to Si indicates a single crystalline behavior with good SiGe material quality. The inset picture is the electron diffraction pattern of this structure. By examining the higher-order reflections, we found the diffraction spots resulting from SiGe and Si are well aligned, which proves the epitaxial nature of

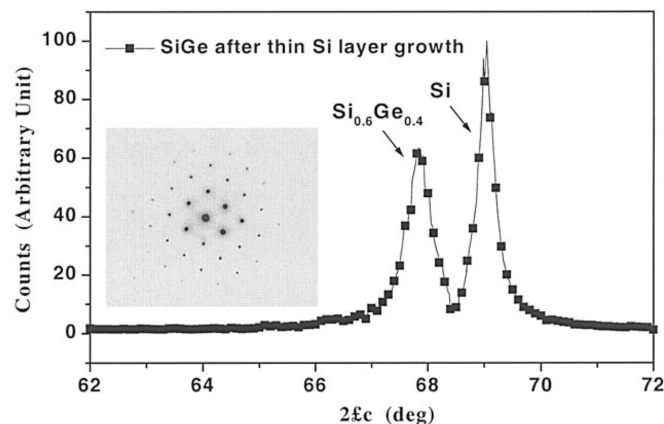

Figure 1. XRD of SiGe and Si substrate after a thin Si layer growth. The narrow linewidth of SiGe compatible to Si suggests good material quality. Inset: the related electron diffraction pattern.

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this heterostructure. The highly oriented diffraction pattern is also consistent with the sharp and strong XRD peak that indicates the formed SiGe has good crystalline quality. It is important to notice that the top Si should be single crystal although the oxidized SiO_2 is amorphous. This is because electron or hole wave function[19] may occupy both SiGe and unconsumed top Si that can degrade the device interface and transport property due to the poor quality of amorphous Si as the case of thin film transistor.

We used C-V measurements to investigate the oxide quality. Figure 2a shows the typical C-V curves of the $Si/Si_{0.6}Ge_{0.4}$ MOS capacitor with a 50 Å oxide. The curve clearly shows no anomalous phenomenon such as sequential population of $Si_{0.6}Ge_{0.4}$ channel and top Si layer.[11] This is because the thin top Si layer is almost fully consumed during thermal oxidation. The closely matched curves measured at high and low frequency under accumulation suggests good interface property with a very low trap density. We have further plotted the calculated interface-trap density in Fig. 2b obtained from the C-V curves. A low interface and oxide charge density of 6.2×10^{10} eV^{-1} cm^{-2} and of 5.8×10^{10} cm^{-2} are measured, respectively, which indicates the good oxide quality similar to thermal SiO_2 and are acceptable for practical VLSI technology.

We have also studied the oxide leakage current and breakdown behavior. Figure 3 shows the I-V characteristics of 50 Å thermal oxides grown on both $Si/Si_{0.6}Ge_{0.4}$ and Si. The small current peak at low voltage (<0.5 V) is due to the neutral trap conduction distributed in the oxide. It is important to note that the oxide grown on $Si/Si_{0.6}Ge_{0.4}$ has comparable electrical characteristics with Si control sample. This is because the thermal oxide is grown on top Si layer rather than directly on SiGe that circumambulates the problems of forming a mixed SiO_2 and GeO_x with Ge snow plowing and accumulated at oxide/SiGe interface.[9] Nevertheless, the slightly higher leakage current and lower breakdown voltage may be due to the inferior crystalline quality of the top Si layer to bulk Si. A respective breakdown electric field and leakage current at −3.3 V of 13.8 MV/cm and 4.2×10^{-8} A/cm^2 are measured for thermal oxide grown on $Si/Si_{0.6}Ge_{0.4}$, which is also capable for current VLSI application.

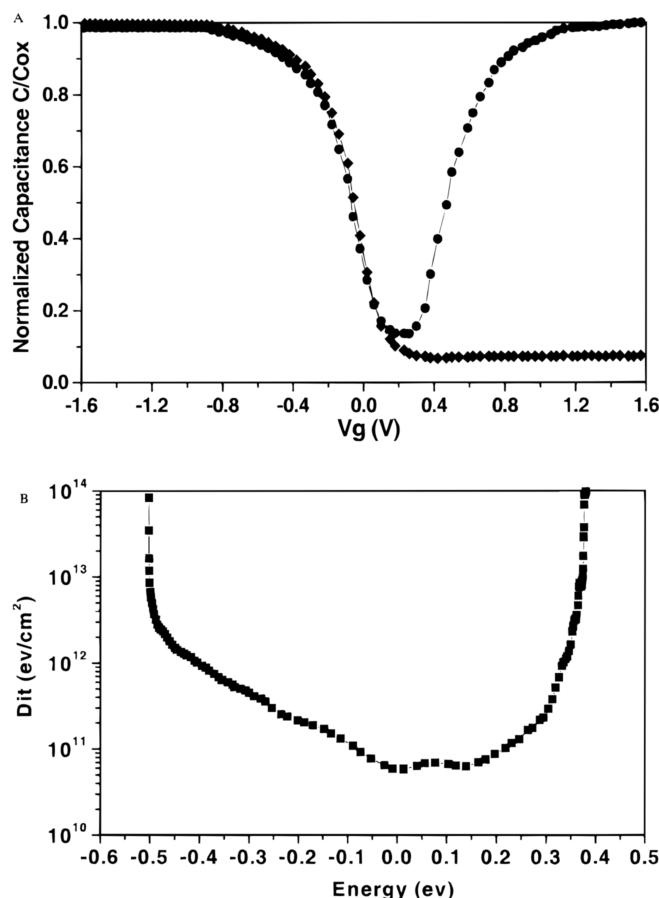

Figure 2. (a) Low- and high-frequency C-V curves and (b) interface-trap density of the 30 Å Si/350 Å $Si_{0.6}Ge_{0.4}$ MOS capacitor with a 50 Å oxide grown at 900°C.

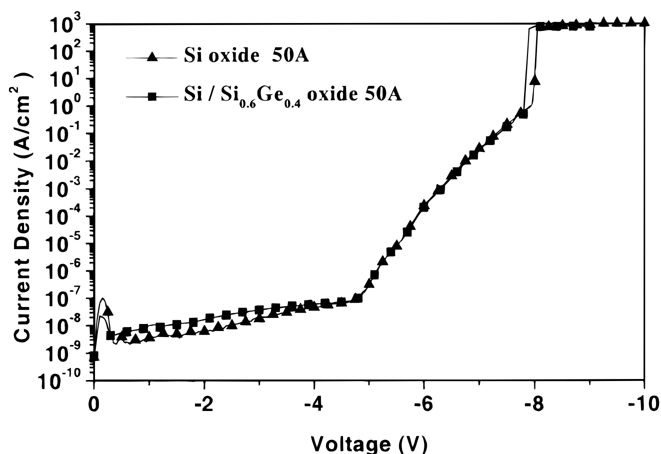

Figure 3. I-V characteristics of 50 Å thermal oxides formed on both 30 Å Si/350 Å $Si_{0.6}Ge_{0.4}$ and standard Si.

Gate oxide reliability is another important factor for practical applications. Figure 4 shows the cumulative failure plot on TDDB lifetime under a constant voltage stress at −6.5 V. A negative polarity was used in this measurement to avoid any voltage drop in the depletion region. The inset figure shows the time evolution of gate current under this stress voltage. It shows that there was a gradual decrease of oxide current with time until the oxide undergoes a dielectric breakdown and Q_{BD} can be calculated from this plot. The Q_{BD} obtained under this condition is in the range of 5.1 to 6.7 C/cm^2 for the control Si sample and 4.5 to 5.9 C/cm^2 for oxide grown on $Si/Si_{0.6}Ge_{0.4}$. The tight distribution and comparable TDDB and Q_{BD} values with control thermal SiO_2 suggest the excellent reliability of $Si/Si_{0.6}Ge_{0.4}$ oxide.

We also measured the SILC to further examine the oxide quality because it is important for gate oxide reliability and those devices with carrier transport through oxide such as flash memory. Figure 5 shows the SILC of oxide grown on $Si/Si_{0.6}Ge_{0.4}$ and the inset figure is the tunneling current under −5 V stress for 10000 s. The tiny increase of leakage current also proves good SILC resistance of thermal oxide grown on $Si/Si_{0.6}Ge_{0.4}$. This small SILC effect on oxide is also consistent with the high breakdown electric field, Q_{BD}, and TDDB mentioned previously.

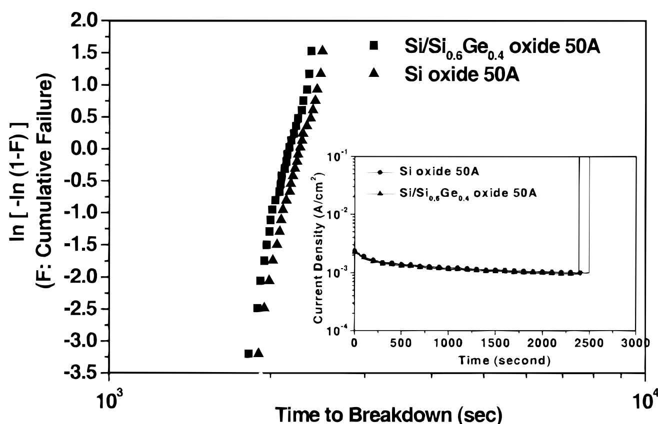

Figure 4. Cumulative failure plot on TDDB lifetime under a constant voltage stress of −6.5 V. Inset: the time evolution of gate current.

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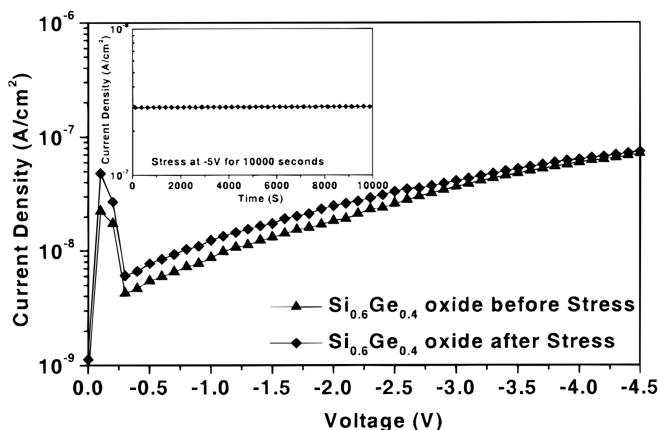

Figure 5. SILC effect of 50 Å thermal oxide grown on 30 Å Si/350 Å $Si_{0.6}Ge_{0.4}$ measured under −5 V for 10,000 s.

We further studied the oxidation effect on $Si/Si_{0.6}Ge_{0.4}$ by measuring the surface roughness change using AFM. Figure 6a and b illustrate the measured surface topography before and after oxidation, respectively. A measured root-mean-square (rms) roughness is 1.3 and 1.6 Å for $Si/Si_{0.6}Ge_{0.4}$ before and after oxidation, respectively. It is important to notice that these rms values are also comparable with thermal SiO_2 grown on Si substrate.[20] The very smooth oxide surface also suggests that the high temperature (900°C) formed $Si/Si_{0.6}Ge_{0.4}$ is stable during subsequent high-temperature (900°C) oxidation. This is due to the formed $Si_{0.6}Ge_{0.4}$ that is already strain-relaxed during the first high-temperature solid phase epitaxy. Furthermore, no strain relaxation related roughness reported previously[14] could be identified in AFM figures. Therefore, the reason for good oxide quality may be ascribed to both high oxidation temperature, smooth and pinhole free oxide surface. This result is in sharp contrast to traditional low-temperature chemical vapor deposition grown SiGe because strain relaxation and defect generation are observed during high-temperature oxidation.

Conclusions

We have developed a new method to grow high-quality thermal oxide on $Si_{0.6}Ge_{0.4}$ with a thin Si top layer. The good oxide integrity is due to the high-temperature thermal oxidation directly on Si top layer, with additional strain relaxed and thermally stable $Si_{0.6}Ge_{0.4}$ formed by solid phase epitaxy at high temperatures. The advantage of this process is that it provides a simple and inexpensive way to form SiGe with high-quality gate oxide and this process is fully compatible to the current CMOS technology.

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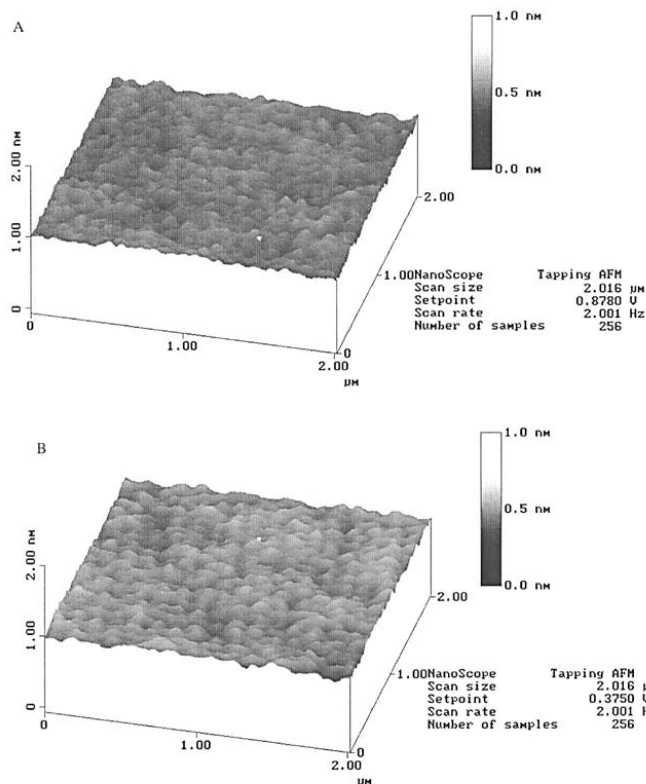

Figure 6. AFM surface morphology (a) before and (b) after 50 Å thermally oxide grown on 30 Å Si/350 Å $Si_{0.6}Ge_{0.4}$.

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