vided by the results of Fig. 3 is that, at sufficiently high energy density, a single pulse irradiation can produce the required activation of the thin film phosphor whilst maintaining the high field electron transport properties of the device determined by the interface state distribution. This is indicated by the maintenance of a sharp luminance against voltage characteristic with no drop in threshold voltage. Such an improvement in EL characteristics will have a very considerable impact in the field of both large and small area flat panel displays, where TFEL has already been demonstrated to be a reliable technology.

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Low contact resistance of poly-plug structure by *in-situ* HF-vapour cleaning

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A low contact-resistance poly-plug structure realised by *in-situ* HF-vapour cleaning in a clustered tool is described. The native oxide in the contact area can be efficiently removed by the combination of an HF-dipping and *in-situ* HF-vapour cleaning process, resulting in a low specific contact resistance.

Introduction: As device sizes are scaled down, the realisation of thinner dielectrics and use of smaller contact holes are desirable to increase the speed and density of the circuits. For thin dielectric films, the use of an *in-situ* HF-vapour cleaning process before oxidation (or deposition) has been found to improve the dielectric integrity compared to the conventional wet HF-dipping cleaning method [1, 2]. For a high-density memory (e.g. DRAMs), traditional metal contacts are not used in memory bit-cells owing to the high leakage current [3]. Instead, a polysilicon-plug (poly-plug) between the source/drain and the first level metal is used. However, the high aspect ratio and small dimensions of the contacts make the removal of native oxide difficult when using the conventional wet etching technique, i.e. it is not easy to wet the small hole with a high aspect ratio and there is a diffusion out of by-products. This will result in a huge contact resistance. Recently, it has been demonstrated that a clustered tool, including *in-situ* HF-vapour cleaning, can be used to obtain a native-oxide-free silicon surface without exposing the surface to air after etching. This technique is attractive for the poly-plug process for DRAMs because the high aspect ratio contact in DRAMs can be easily cleaned using vapour phase HF cleaning. In this Letter a comparison of four methods for contact hole cleaning is presented, including conventional wet HF-dipping and/or a new *in-situ* HF-vapour cleaning method.

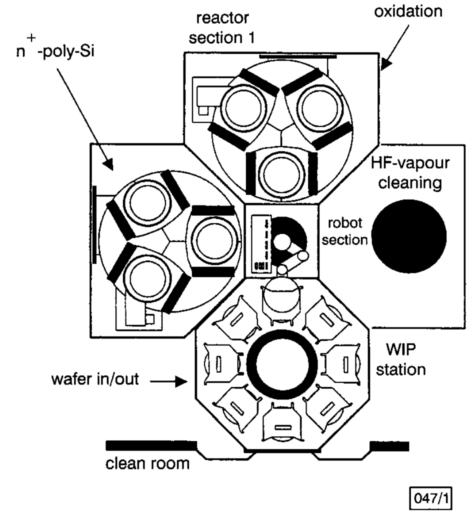

Fig. 1 *Schematic diagram of clustered system with three modules*

Experiments: Fig. 1 shows the top view of the clustered vertical system (ASM-A400/3) consisting of three modules, i.e. HF-vapour cleaning, oxidation, and *in-situ* n^+-doped poly-Si deposition. Wafers were processed using HF-vapour cleaning and *in-situ* n^+-doped poly-Si modules in sequence without exposure to the ambient, so as to obtain a native-oxide-free n^+-poly-Si/Si contact structure. To achieve this, the cabinet was filled with high purity nitrogen (with a residual oxygen content of <4ppm), to suppress any native oxide growth after the HF-vapour stripping of the original native oxide. In this experiment, a Kelvin contact structure was used to study the specific contact resistance of the poly-plug contact source/drain. After the channels and the contact holes were defined, the contact holes were cleaned by (i) a de-ionised (DI) water rinse, (ii) 50:1 HF-dipping, (iii) *in-situ* HF-vapour cleaning, (iv) 50:1 HF-dipping + *in-situ* HF-vapour cleaning. The *in-situ* n^+-poly-Si was then deposited in the clustered system and RTA 1050°C annealing was carried out to form the n^+ region. The metal pad was then deposited and defined. The contact resistance was measured using an HP4156 apparatus.

Results and discussion: Fig. 2 shows the specific contact resistance of the poly-plug contact source/drain after the use of four different contact-hole cleaning methods. It can be seen that the specific contact resistance is dramatically reduced after wet HF-dipping or *in-situ* HF-vapour cleaning. In addition, the vapour phase cleaning process (*in-situ* HF-vapour cleaning) is better than wet cleaning (HF-dipping). The best result is achieved by the combination of HF-dipping and *in-situ* HF-vapour cleaning, which exhibits a contact resistance that is one order of magnitude smaller than that obtained using DI water rinsing. To understand the interfacial oxygen profile, the depth profile of oxygen was measured using SIMS for these four samples. The results are shown in Fig. 3. The oxygen peak indicates the relative quantity of native oxide. In the DI-water-rinsed case, the oxygen peak is the highest of the four samples. This in turn leads to the highest specific contact resistance, as shown in Fig. 2. The oxygen peak and bandwidth for

HF-dipping or the *in-situ* HF-vapour cleaning method are lower and narrower than those for the DI-water-rinsed sample. This is consistent with the lower specific contact resistance as shown in Fig. 2. This implies that either wet HF-dipping or HF-vapour cleaning is essential to remove native oxide in the contact area. The lowest specific contact resistance is found by the combination of HF-dipping and HF-vapour cleaning, which also exhibits one order of magnitude smaller oxygen count than that obtained using wet HF-dipping or the HF-vapour method.

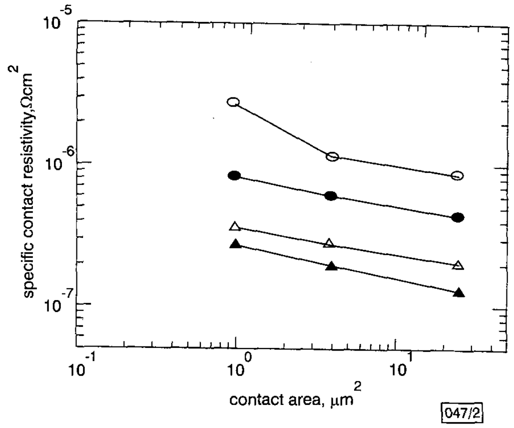

Fig. 2 *Specific contact resistance of poly-plug contact after different contact hole cleaning methods*

—○— DI rinsed
—●— HF dip
—△— HF vapour
—▲— HF dip + HF vapour

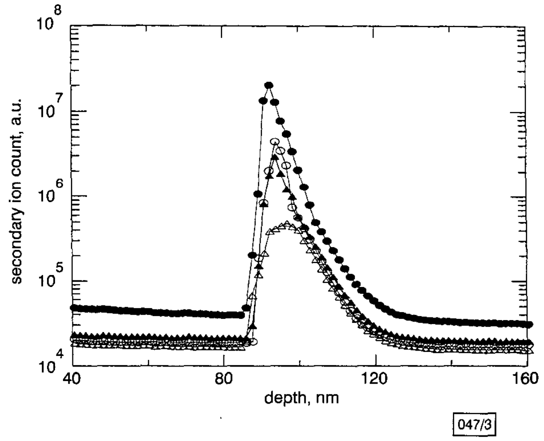

Fig. 3 *SIMS depth profile of oxygen for four samples*

—●— DI rinsed
—○— HF dip
—▲— HF vapour
—△— HF dip + HF vapour

Conclusions: We have described a low contact-resistance poly-plug structure obtained using *in-situ* HF-vapour cleaning in a clustered tool. The native oxide in the contact area can be efficiently removed by the combination of an HF-dipping and *in-situ* HF-vapour cleaning process, resulting in a small specific contact resistance.

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Transient processes in AlGaN/GaN heterostructure field effect transistors

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The authors report on the correlation between transient behaviour and 1/*f* noise in GaN/AlGaN heterostructure field effect transistors (HFETs) and novel GaN/AlGaN metal-oxide-semiconductor heterostructure field effect transistors (MOS-HFETs). When the HFETs were switched from the OFF to ON position, they exhibited non-exponential transient processes with characteristic times from 10^{-7} to 10^{-2}s. The transient behaviour correlated with the level of 1/*f* noise. MOS-HFETs fabricated on the same wafer as the HFETs did not exhibit such a transient (within the time resolution of the measurement setup, which was a few nanoseconds).

Recent measurements of pulse current voltage characteristics of GaN MESFETs [1] showed that due to the deep levels in GaN pulse current voltage characteristics differ essentially from that measured at DC current. However, transient processes responsible for this feature were not analysed. A very high relaxation time of several hundred seconds in AlGaN FETs was reported in [2]. Recently, Kohn [3] reported on the studies of trapping effects in AlGaN/GaN HEMTs, which highlighted the importance of these effects in these devices.

In this Letter, we report on the correlation between transient behaviour and 1/*f* noise in GaN/AlGaN heterostructure field effect transistors (HFETs) and novel GaN/AlGaN metal-oxide-semiconductor heterostructure field effect transistors (MOS-HFETs) [4].

The MOS-HFETs had a very high (10 orders of magnitude) on-to-off ratio. At the gate bias, $V_g = -1$V, the gate leakage current did not exceed 100pA for MOS-HFETs and was within the range from 1μA to 10μA for HFETs.

The pulse measurements were performed in a common source configuration. The transistors were biased in the linear regime, and negative or positive voltage pulses were applied to the gate. A low inductance resistor was connected in series with the drain. Both gate and drain current pulses were recorded using a digital oscilloscope. A probe station with tungsten probes was used to provide contacts to the transistor pads. The time resolution of the setup was better than 7ns for both rise and fall times.

The AlGaN/GaN HFETs and MOS-HFETs under investigation were normally-on transistors. To study the transient behaviour we applied a negative voltage pulse of amplitude V_g to the gate, which decreased the drain current or turned the transistors off. Fig. 1 shows the waveform of the drain voltage pulse for HFETs at different gate voltage pulse amplitude. DC gate bias was kept at zero. The transient process during the time of τ ~200ns can be seen only when the transistor is switched from the OFF to ON position. As can be seen from Fig. 1, we did not find any transients longer than 7ns during the turn-off transient, even when the gate voltage was switched from a relatively high positive value of 3–5V to well below the threshold voltage, V_t.