Design on the Low-Leakage Diode String for Using in the Power-Rail ESD Clamp Circuits in a 0.35-μm Silicide CMOS Process

Ming-Dou Ker, *Senior Member, IEEE,* and Wen-Yu Lo

***Abstract*—A new design on the diode string with very low leakage current is proposed for using in the ESD clamp circuits across the power rails. By adding an NMOS-controlled lateral SCR (NCLSCR) device into the stacked diode string, the leakage current of this new diode string with six stacked diodes at 5-V (3.3-V) forward bias can be reduced to only 2.1 (1.07) nA at a temperature of 125°C in a 0.35-μm silicide CMOS process, whereas the previous designs have a leakage current in the order of mA. The total blocking voltage of this new design with NCLSCR can be linearly adjusted by changing the number of the stacked diodes in the diode string without causing latch-up danger across the power rails. From the experimental results, the human-body-model ESD level of the ESD clamp circuit with the proposed low-leakage diode string is greater than 8 kV in a 0.35-μm silicide CMOS process by using neither the ESD-implantation nor the silicide-blocking process modifications.**

***Index Terms*—Electrostatic discharge (ESD), latch-up, ESD protection circuit, diode string, SCR, leakage current, ESD bus.**

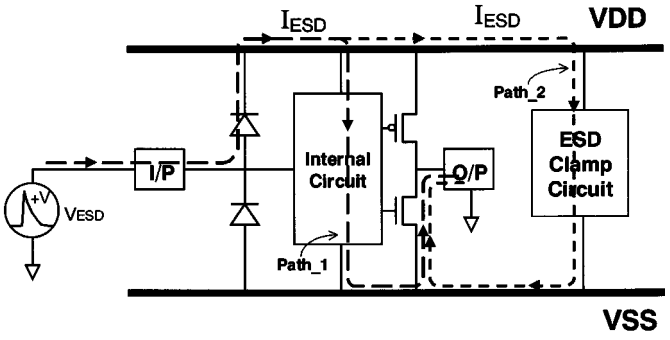

Fig. 1. The ESD current discharging paths in an IC during the pin-to-pin ESD stress condition. If the IC has no ESD clamp circuit between the VDD and VSS power rails, the ESD current is discharged through the Path_1, which often causes ESD damage located at the internal circuits. If the IC has an effective ESD clamp circuit between the VDD and VSS power rails, the ESD current is discharged through the Path_2.

I. Introduction

ELECTROSTATIC discharge (ESD) has been a serious reliability concern in deep-submicron CMOS IC's. In order to obtain high ESD robustness, a CMOS IC must be incorporated with on-chip ESD protection circuits at every input and output pin. However, some unexpected ESD damages had been still found in the internal circuits of CMOS IC's beyond the input or output ESD protection circuits [1]–[6]. Even the parasitic capacitance and resistance along the power lines of the IC could also cause a negative impact on ESD reliability of the CMOS IC [3]–[6].

Since the ESD stress may have positive or negative voltage on an input (or output) pin with respect to the grounded VDD or VSS pins, there are four different ESD-testing pin combinations at each input (output) pin [7]. For a comprehensive ESD verification, two additional ESD-testing pin combinations, the pin-to-pin ESD stress and the VDD-to-VSS ESD stress, had been also specified to verify the whole-chip ESD reliability [7]. These two additional ESD-testing pin combinations often lead to more complex ESD current paths from the input or output pins through the power lines into the internal circuits, which will cause some unexpected damages on the internal circuits even if there are input and output ESD protection circuits in the IC's [8]–[10]. The pin-to-pin ESD stress, as shown in Fig. 1, often causes the unexpected ESD damage located in the internal circuits, rather than the input or output ESD protection circuits. In Fig. 1, a positive ESD voltage is applied to some input pin with some output pin relatively grounded, while the VDD and VSS pins are floating. The ESD current will be diverted from the input pad to the floating VDD power line through the forward-biased diode in the input ESD protection circuit. The ESD current flowing in the VDD power line can be conducted into the internal circuits through the connection of VDD line. Then, the ESD current is discharged through the internal circuits and may cause random ESD damage in the internal circuits, as the **Path_1** current path shown in Fig. 1. If there is an effective ESD clamp circuit across the VDD and VSS power lines, the ESD current can be discharged through the **Path_2** current path in Fig. 1. Therefore, the internal circuits can be safely protected against the ESD damages. Thus, an effective ESD clamp circuit between the power rails is necessary for protecting the internal circuits against ESD damage [11]–[18].

In this paper, a new power-rail ESD clamp circuit with the SCR device and the diode string is proposed. This new design can apply the excellent ESD robustness of the SCR device and the diode string for power-rail ESD clamp, but without the disadvantages of both the leakage current in the previous diode string designs [12]–[17] and the latch-up problem in the SCR device from VDD to VSS.

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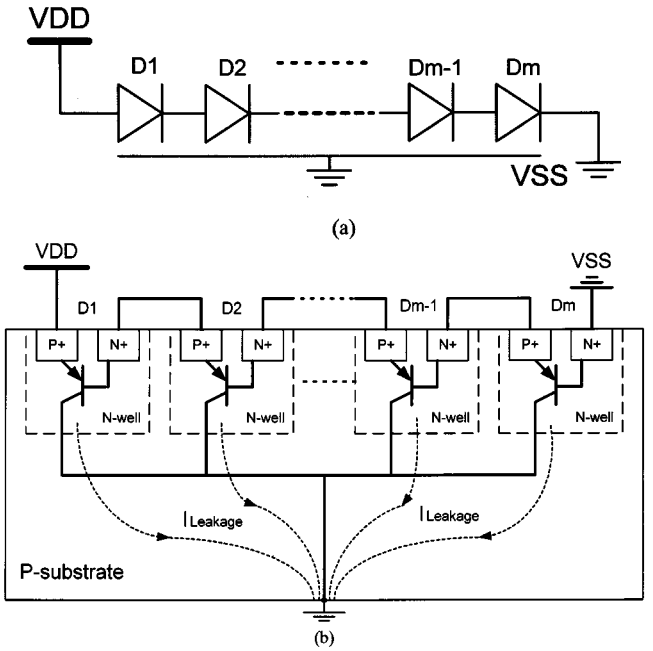


Fig. 2. (a) The schematic circuit diagram and (b) the cross-sectional view, of the pure diode string realized in a P-substrate N-well CMOS technology.

II. Review on the Diode String and the SCR for ESD Protection

A. The Diode String

Because the diode in the forward-biased condition can sustain a much higher ESD level than it in the reverse-biased condition, the diode string with multiple stacked diodes was therefore proposed to clamp the ESD overstress voltage on the 3.3–5-V-tolerant I/O pad [12] or between the mixed-voltage power lines [13]–[17].

The p-n-p-based diode string used as the ESD clamp from VDD to VSS power lines is illustrated in Fig. 2(a), whereas the device structure of such a diode string realized in a P-substrate n-well CMOS process is illustrated in Fig. 2(b). Each diode forms a parasitic vertical p-n-p transistor with the substrate in a common collector configuration. The blocking voltage ($V_{\rm String}$) across a diode string with m stacked diodes can be expressed as [15]:

$$V_{\rm String}(I) = mV_D(I) - nV_T \times \left[\frac{m(m-1)}{2}\right] \times \ln(\beta+1) \tag{1}$$

$$V_D(I) = nV_T \times \ln\left(\frac{I}{AI_S}\right) \tag{2}$$

$$V_D(T_1) = nE_{g0} + \left(\frac{T_1}{T_0}\right) \times \left(V_D(T_0) - \frac{nE_{g0}}{q}\right) \tag{3}$$

where

- I current flowing into the diode string;
- V_D forward turn-on voltage of one diode;
- V_T $= (KT/q)$ is the thermal voltage, where q is the electron charge, K is Boltzmann's constant, and T is the absolute temperature;
- n ideality factor;
- β beta gain of the parasitic vertical p-n-p transistor,
- I_S saturation current of the p-n junction diode,
- A area of the p-n junction diode,
- m number of stacked diodes in the diode string, and
- E_{g^0} $= 1.206$ eV is the extrapolated bandgap of Si at the temperature of 0 K.

From (1), if the β gain is close to zero, the blocking voltage of a diode string can be linearly increased when more diodes are stacked in the diode string. However, if the β gain is one or even larger, the addition of stacked diodes in the diode string doesn't linearly increase the blocking voltage across the diode string, but causes more leakage current flowing into the substrate. This means that more stacked diodes would be needed to support the same blocking voltage of a diode string at a specified current when the β gain of the parasitic vertical p-n-p increases. The main issue of the p-n-p-based diode string used as the VDD-to-VSS ESD clamp circuit is the leakage current, where the amplification effect of multistage *Darlington* beta gain often causes more leakage current from VDD to the grounded substrate. If the voltage difference between VDD and VSS becomes larger, the leakage current will increase exponentially.

Another issue on the diode string is the reduction on the blocking voltage of the diode string at a higher temperature. The temperature effect on a diode in the forward-biased condition is shown in (3), where the temperature coefficient of V_D is negative, because the nE_{g^0}/q (=1.206 V) is greater than V_D (around 0.55–0.65 V for forward current of 1–10 μA at the room temperature). This means that more stacked diodes are required in the diode string to control a reasonable leakage current at a higher temperature. This will occupy a larger silicon layout area in a chip.

B. Previous Design on the Diode String to Reduce Leakage Current

To reduce the leakage current of the p-n-p-based diode string, especially operating in the high-temperature environment, three previous designs had been reported by T. Maloney [15]–[17], which are re-drawn in Fig. 3(a)–(c) with the names of *Cladded diode string*, *Boosted diode string*, and *Cantilever diode string*, respectively. Such three previous designs are also fabricated with the proposed new design in the same wafer to verify their leakage current and ESD robustness.

1) The Cladded Diode String: The reason for the declining incremental voltage across the p-n-p-based diode string, while the number of stacked diodes increases, is the lower current level through the latter diode stages. An idea to solve this problem was provided by augmenting the diode string with a bias network to distribute small but significant forward current into the later diode stages. The cladded diode string shown in Fig. 3(a) is created by this concept, in which M1 and M2 are both long channel PMOS transistors as resistors to provide forward current from VDD to the later stacked diodes. M3 is an NMOS transistor used as a resistive connection to VSS (ground) on the gates of M1 and M2. The device dimensions (*W/L*) of M1, M2, and M3, are decided from the previous design [15] as 1.8/40, 1.8/40, and 1.8/5 (μm/μm), respectively, which are simulated by the *HSPICE* program with a 0.35-μm silicide CMOS device parameters.

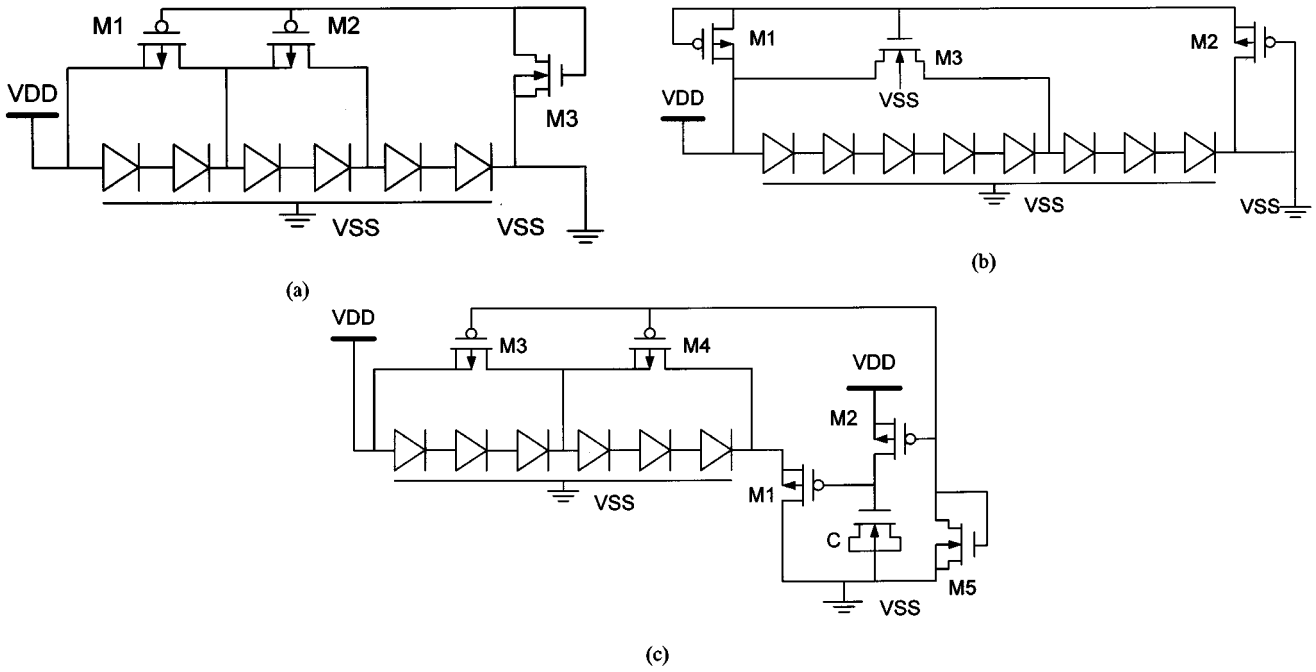


Fig. 3. The circuit diagrams of: (a) the *Cladded diode string*, (b) the *Boosted diode string*, and (c) the *Cantilever diode string*, in the previous diode string designs [15].

2) The Boosted Diode String: The boosted diode string was designed with the similar concept of the cladded diode string by distributing current to the later stacked diodes. In Fig. 3(b), the PMOS transistors M1 and M2 are always on, but such long channel devices do not draw significant leakage current. When the voltage at the source of M3 is lower than its gate voltage with a voltage difference greater than its threshold voltage, the source follower M3 (a stronger device) turns on until the later part of the diode string is replenished adequately. The device dimensions (W/L) of M1, M2, and M3, are decided as 1.8/40, 1.8/40, and 200/1 (μm/μm), respectively, in a 0.35-μm silicide CMOS process.

3) The Cantilever Diode String: The design concept of the cantilever diode string is to block the diode string from VSS when the IC is in the normal operating condition, which help to avoid the amplification effect of multistage *Darlington* beta gain among the vertical p-n-p transistors in the diode string, and therefore to reduce the leakage current into the P-substrate. In Fig. 3(c), the PMOS transistor M1 is used as the termination of the diode string from VSS in normal condition but sinks a substantial amount of current while an ESD pulse occurs. The PMOS transistor M2 and MOS-capacitor C are used as a *RC*-based ESD detection circuit to distinguish the ESD-stress or the normal operating conditions, and to turn on or off M1 correctly. The PMOS transistors M3 and M4 are long channel devices used as the bias network as that shown in the cladded diode string design. The small NMOS transistor M5 provides a ground connection without allowing a power supply voltage across a single thin gate oxide. The device dimensions (*W/L*) of M1, M2, M3, M4 and M5, are decided as 200/1, 1.8/40, 1.8/40, 1.8/40 and 1.8/5 (μm/μm), respectively, in a 0.35-μm silicide CMOS process.

C. The NMOS-Controlled Lateral SCR

Due to the inherent capability of high power delivery, the lateral SCR device has been used as an on-chip ESD protection element in CMOS IC's. Experimental results had shown that the lateral SCR device can sustain high ESD stress within a smallest layout area as compared to other traditional ESD protection elements [19]. An improved design on the lateral SCR is to use the low-voltage-trigger lateral SCR (LVTSCR) device to protect CMOS IC's [20]–[24]. The trigger voltage of an LVTSCR can be lowered to the drain snapback-breakdown voltage of a short-channel thin-oxide NMOS device, which is about $\sim$10 V in a 0.35-μm silicide CMOS process.

Due to the low trigger voltage ($\sim$10 V), the LVTSCR device can perform excellent on-chip ESD protection without the support of the secondary protection circuit. But, its low trigger current ($\sim$10 mA) may cause the LVTSCR to be accidentally triggered on by the external noise pulses while the CMOS IC is in the normal operating condition [25]–[27]. Moreover, due to the system-level reliability request of the so-called "CE" mark from the *European Community*, an ESD gun with ESD voltage of $\pm$8–15 kV is used to verify the electromagnetic compatibility (EMC) of the electronic products [28]–[30]. Such EMC/ESD test can cause a heavily overshooting or undershooting voltage transition on the VDD and VSS pins of IC's in the system board. Such a system-level EMC/ESD event easily causes the transient-induced latch-up failure in CMOS IC's [31]–[33], if a single lateral SCR or an LVTSCR device is used as the ESD clamp device between the VDD and VSS power lines.

The LVTSCR devices in the input or output ESD protection circuits are also susceptible to such system-level noise pulses. Because the holding voltage of the LVTSCR in bulk CMOS technologies is only $\sim$1 V, the voltage levels of the input or output signals can be destroyed if the LVTSCR in the ESD protection circuits is accidentally turned on when the IC is in the normal operating condition [27]. For example, in Fig. 4(a), the output buffer of Chip 1 is used to drive the input pad of Chip 2, where the input ESD protection circuit in Chip 2 is formed

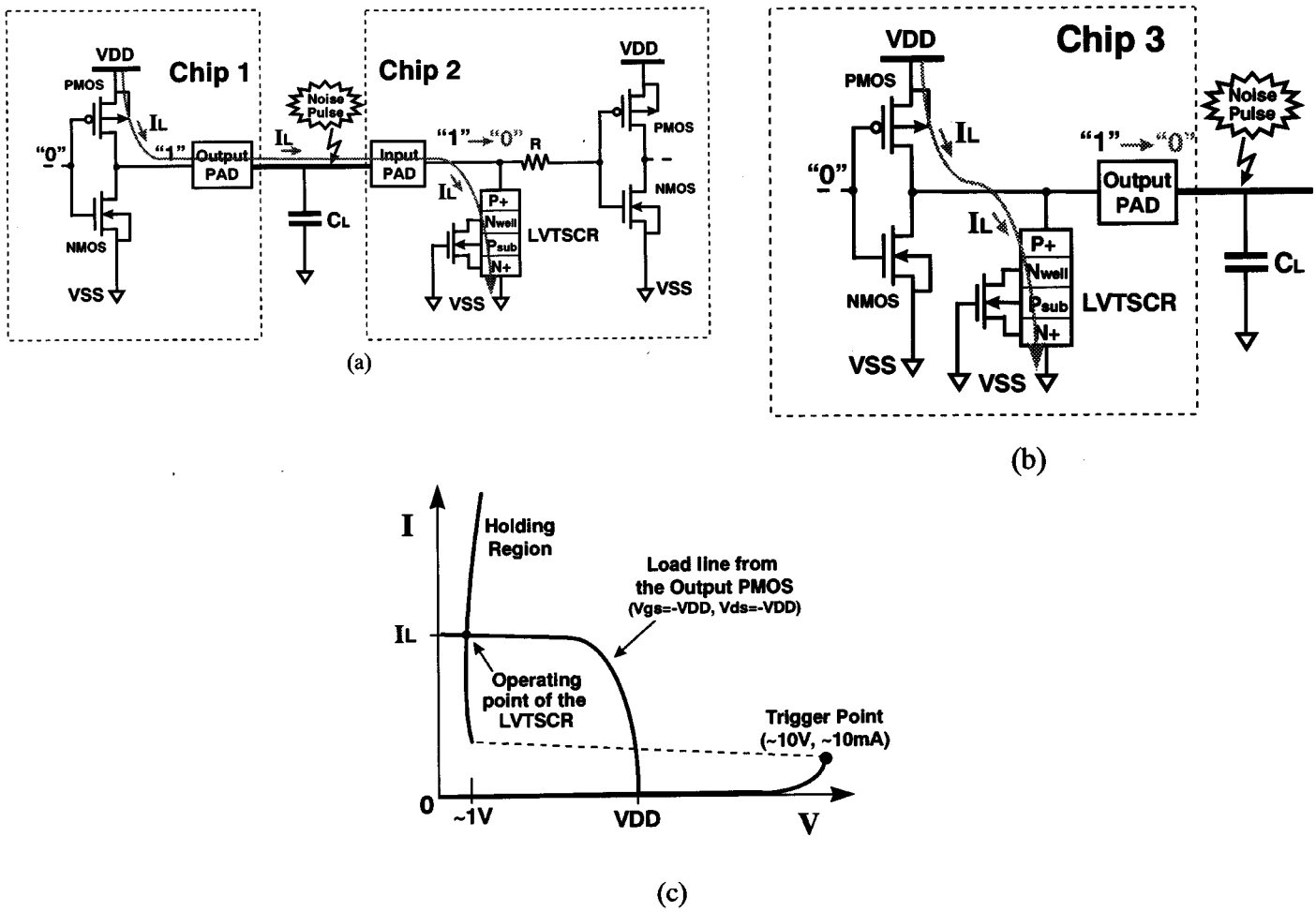


Fig. 4. The schematic diagram to show the LVTSCR in: (a) an input ESD protection circuit in Chip 2; (b) an output ESD protection circuit in Chip 3, being accidentally triggered on by the system-level overshooting noise pulses; and (c) intercept point between the *I–V* curves of the output PMOS and the LVTSCR decides the voltage level on the pad and the leakage current I_L from VDD to VSS.

by the LVTSCR. While the output buffer in Chip 1 sends an output signal of logic "1" to the input pad of Chip 2, the output PMOS in Chip 1 is turned on by the pre-buffer circuit. Therefore, the voltage level on the input pad of Chip 2 is charged up to VDD, and the LVTSCR is initially kept off. But, if there is a board-level noise pulse coupled to the interconnection line between the output pad of Chip 1 and the input pad of Chip 2, the LVTSCR in Chip 2 could be triggered on by the overshooting noise pulse and the voltage level on the input pad is clamped to only ~1 V by the turned-on LVTSCR. If the LVTSCR device is used in the output ESD protection circuit, as shown in Fig. 4(b), the LVTSCR could be also triggered on by the noise pulse coupled at the output pad.

Because the output PMOS often has a large device dimension to drive the external heavy load, the load line of the output PMOS has a stable intercept point on the *I–V* curve of the LVTSCR. The intercept point in Fig. 4(c) is the operating point of the LVTSCR, where there is a leakage current I_L flowing from the VDD through the output PMOS and LVTSCR to the VSS in the electronics systems. Due to the triggering of noise pulses, the turned-on LVTSCR clamps the voltage level on the input pad of Chip2 (the output pad of Chip 3) from VDD to ~1 V. This changes the logic state from "1" to "0" on the pad and causes an operation error in the application system. Therefore, the LVTSCR or SCR with a holding voltage lower than VDD should be suitably modified to overcome the latch-up issue before they are used in the on-chip ESD protection circuits.

III. Design of the Low-Leakage Diode String

In this section, a new diode string design with very low leakage current is proposed for using in the power-rail ESD clamp circuits. By adding an NMOS-controlled lateral SCR (NCLSCR) device into the stacked diode string, the excellent ESD protection performance of the diode string can be maintained with neither the leakage current in the previous diode string designs nor the VDD-to-VSS latch-up problem in the SCR device.

A. The New Proposed Low-Leakage Diode String

The new design to reduce the leakage current in the diode string is shown in Fig. 5(a), whereas the corresponding device structure is drawn in Fig. 5(b). An NCLSCR device is added on the top of the diode string to block the leakage current from VDD to VSS through the diode string. But, the NCLSCR is

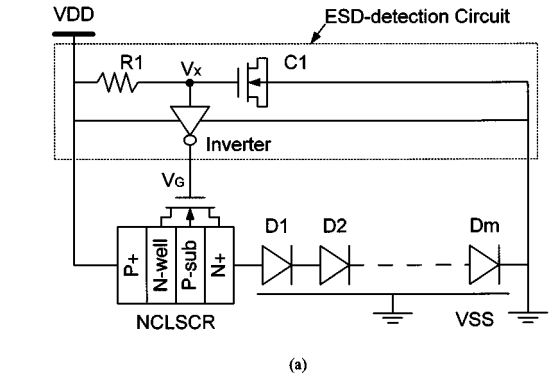


Fig. 5. (a) The schematic circuit diagram, and (b) the device structure, of the new proposed diode string realized in p-substrate CMOS technology.

designed to be quickly turned on to bypass the ESD current through the diode string, while the IC is in the ESD-stress condition. To achieve such desired turn-on and turn-off operations on the NCLSCR, the *RC*-based ESD-detection circuit [18] is applied to control the gate of the NCLSCR. The *RC* time constant in the *RC*-based ESD-detection circuit is designed about 0.1–1 μs to distinguish the ESD-stress transition or the normal VDD power-on transition.

The human-body-model ESD voltage has a rise time about $\sim$10 ns [7]. When an ESD voltage is across the VDD and VSS power lines, the voltage level at Vx shown in Fig. 5(a) is increased much slower than the voltage level on the VDD power line, because the *RC*-based ESD-detection circuit has a time constant of 0.1–1 μs. Due to the delay of the voltage increase on the node Vx, the inverter in Fig. 5(a) is self-biased by the ESD voltage across the VDD and VSS power lines and conducts a high voltage to the gate (V_G) to turn on the NCLSCR. Therefore, the ESD current can be discharged from VDD to VSS though the NCLSCR and the diode string (the Path_2 in Fig. 1) without causing the unexpected ESD damage located at the internal circuits.

Under the normal VDD power-on condition, the VDD power-on waveform has a rise time in the range of milliseconds (ms). With such a slow rise time of ms, the voltage level on the node Vx in the ESD-detection circuit can follow the VDD voltage in time to keep the V_G at 0 V. Because the gate of the NCLSCR is always biased at 0 V, the NCLSCR is kept off to block the leakage current from VDD to VSS through the diode string. The leakage current of the NCLSCR device is mainly composed by the off-state leakage current of the NMOS

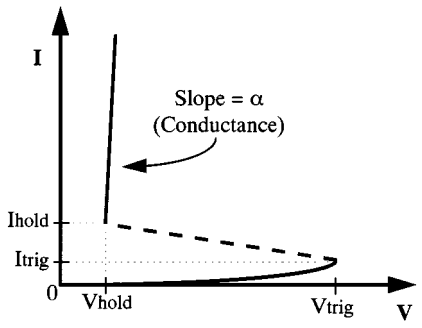


Fig. 6. The typical *I–V* curve of an NCLSCR device.

transistor and the junction leakage current across the n-well and the p-substrate in the NCLSCR device, which does not obviously increase when the environment temperature becomes higher. Therefore, the leakage current of this new design can be significantly reduced to a very low current level ($\sim$nA) even at a higher temperature.

To overcome the latch-up danger, the holding voltage of this new diode string should be designed greater than the voltage difference across the power rails by adding the more stacked diodes in the diode string. With a sufficient large holding voltage, latch-up cannot be held even if the NCLSCR has been accidentally triggered on by an overshooting noise pulse. In fact, when the overshooting noise pulse occurs across the power rails, the NCLSCR can be turned on to clamp it to a voltage level around the holding voltage of this new design. When the overshooting noise pulse disappears, the NCLSCR device turns off automatically and blocks the leakage current from VDD to VSS. Thus, the new proposed low-leakage diode string is also advantageous to clamp the overshooting noise on the power lines, when the IC is in the normal operation conditions.

B. Blocking Voltage of The Low-Leakage Diode String

Because the NCLSCR device in the diode string is used to block the leakage current, the NCLSCR may be immune to latch-up when it is used in the power-rail ESD clamp circuit. Therefore, a simple design equation used to describe the *I–V* relationship of the proposed low-leakage diode string are calculated in the following.

The typical *I–V* curve of an NCLSCR device is shown in Fig. 6 with the parameters of the trigger voltage (current) and the holding voltage (current). If the total blocking (holding) voltage of the proposed low-leakage diode string in the turn-on condition can be greater than VDD of the IC in the normal operating condition, the proposed low-leakage diode string is free to the latch-up issue in the CMOS IC. The voltage across an NCLSCR device in the holding region can be simply modeled as

$$V_{\rm SCR}(I) = V_{\rm hold} + \left(\frac{I - I_{\rm hold}}{\alpha}\right) \quad \text{when } I \geq I_{\rm hold}, \qquad (4)$$

where I is the current through the NCLSCR device, α is the conductance of the NCLSCR device in the holding region, $I_{\rm hold}$ is the holding current of the NCLSCR device, and $V_{\rm hold}$ is the holding voltage of the NCLSCR device.

By applying the superposition principle on the proposed low-leakage diode string, the total blocking voltage ($V_{\rm Total}$) of this new design in the turn-on condition can be derived as

$$V_{\rm Total}(I) = V_{\rm SCR}(I) + V_{\rm String}(I) \quad \text{when } I \geq I_{\rm hold}. \quad (5)$$

By substituting (1) and (4) into (5), the total blocking voltage ($V_{\rm Total}$) of the proposed low-leakage diode string with an NCLSCR and m stacked diodes in the turn-on condition can be presented as

$$V_{\rm Total}(I) = V_{\rm hold} + \left(\frac{I - I_{\rm hold}}{\alpha}\right) + m\left[nV_T \times \ln\left(\frac{I}{AI_S}\right)\right] - nV_T \times \left[\frac{m(m-1)}{2}\right] \times \ln(\beta+1), \quad \text{when } I \geq I_{\rm hold}. \quad (6)$$

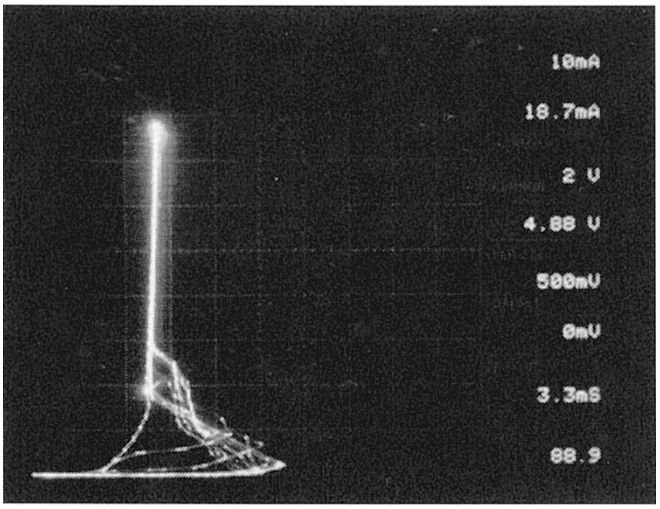
From (6), a suitable number of the stacked diodes in the proposed design can be calculated to make its total blocking voltage greater than the voltage difference across the VDD and VSS power lines. With the total blocking voltage greater than the voltage difference across VDD and VSS power lines, the proposed low-leakage diode string can be guaranteed free to latch-up issue for using in the on-chip ESD protection circuits.

IV. Experimental Results

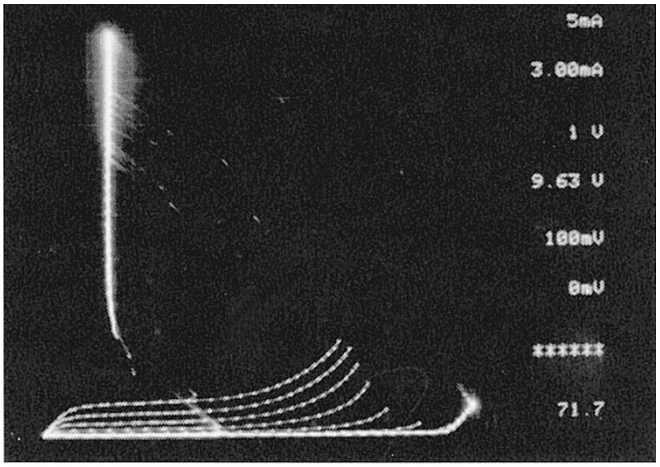
The proposed low-leakage diode string with different number of stacked diodes and the previous diode strings in Fig. 3(a)–(c) had been practically fabricated in a same test chip in a 0.35-μm silicide CMOS process without using the ESD-implantation and the silicide-blocking process modifications. Each diode in the diode strings of this new design and the previous designs has the same device dimension and layout style in the fabricated test chip. The NCLSCR is drawn with a width of 80 μm, a control gate length of 0.35 μm, and a device silicon area of 80 $\times$ 17.5 μm^2. Each p-n-p-based diode in the diode strings is drawn with an emitter area of 80 $\times$ 4.9 μm^2 and a base area of 80 $\times$ 3.3 μm^2. Such a diode occupies a total silicon area of 80 $\times$ 13.2 μm^2. The NMOS-capacitor C1 of the *RC*-based ESD-detection circuit with a device dimension (W/L) of 25/25 (μm/μm) has a capacitance about 2.76 pF, and the resistor R1 in the ESD-detection circuit is drawn by an N-well resistance of 100 kΩ. The time constant of this *RC*-based ESD detection circuit is about 0.276 μs. Experimental tests are therefore measured to compare the ESD robustness and the leakage current among this new proposed diode string and the previous designs for using in the power-rail ESD clamp circuits.

A. The Leakage Current

The measured *I–V* curves of an NCLSCR with four stacked diodes under different gate biases at a temperature of 25 °C are shown in Fig. 7(a), whereas the *I–V* curves of a single NCLSCR are shown in Fig. 7(b). The trigger voltage of the NCLSCR with different number of stacked diodes can be reduced when the gate bias (V_G) on the NCLSCR device is increased. The relation between the total blocking voltage (the holding voltage) of this new design and the number of stacked diodes at the temperatures of 25 °C and 125 °C is measured and summarized in Fig. 8.



(a)



(b)

Fig. 7. The *I–V* curves of (a) an NCLSCR with four stacked diodes, and (b) only a single NCLSCR, under different gate biases in 0.35-μm silicide CMOS process at a temperature of 25 °C.

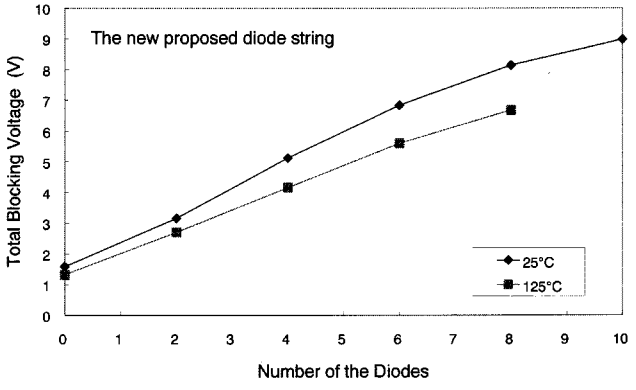


Fig. 8. The relation between the total blocking voltage of this new low-leakage diode string and the number of stacked diodes at the temperatures of 25 °C and 125 °C.

The NCLSCR also contributes about 1-V voltage block to the new proposed diode string, therefore the total blocking voltage is around 1 V in Fig. 8 while the number of diode is equal to zero.

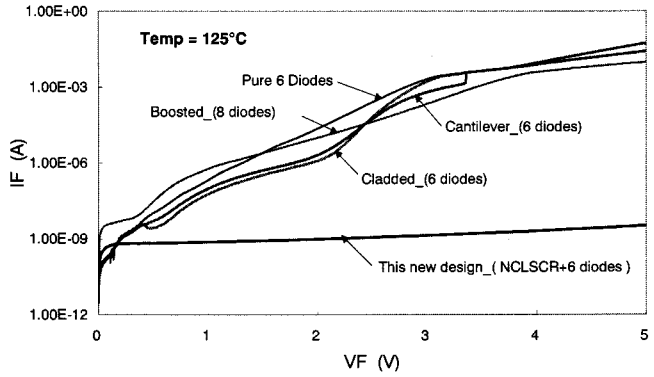


Fig. 9. The measured *I–V* curves of the diode strings among the different designs at the temperature of 125 °C (Y axis is drawn in the log scale).

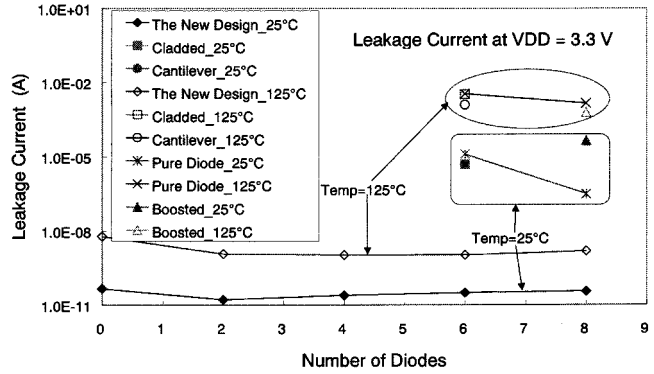


Fig. 10. The leakage currents among the different diode string designs at the temperatures of 25 °C and 125 °C under 3.3-V voltage bias (Y axis is drawn in the log scale).

The measured *I–V* curves of the diode strings among the different designs with six or eight stacked diodes are measured and compared in Fig. 9, under the temperature of 125°C. As seen in Fig. 9, the proposed new design (NCLSCR + 6 diodes) only has a slight increase on its leakage current (∼nA) when the bias voltage is increased to 5 V at the temperature of 125°C. On the contrary, the previous designs [15] have a very obvious increase on their leakage current of up to several mA when the bias voltage is increased to 3 V. This verifies the excellent performance of this new design to reduce the leakage current on the diode string.

The comparison on the leakage current of different diode string designs at the temperatures of 25 °C and 125 °C under a fixed 3.3-V voltage bias is shown in Fig. 10. The leakage current of the pure diode string with six stacked diodes under the VDD bias of 3.3 V at the temperature of 25 °C (125 °C) is 12.45 μA (3.46 mA). The *Cladded diode string* with six diodes under the VDD bias of 3.3 V at the temperature of 25 °C (125°C) is 3.5 μA (3.33 mA). The *Boosted diode string* with eight diodes under the VDD bias of 3.3 V at the temperature of 25 °C (125 °C) is 44.03 μA (0.61 mA). The *Cantilever diode string* with six diodes under the VDD bias of 3.3 V at the temperature of 25 °C (125 °C) is 4.96 μA (1.25 mA). But, the new proposed low-leakage diode string with an NCLSCR and six stacked diodes under the VDD bias of 3.3 V at the temperature of 25 °C (125 °C) is only 31 pA (1.07 nA). The leakage current of the new proposed diode string is not increased in Fig. 10 when the number of the stacked diodes is increased, because the leakage current in the diode string has been blocked by the NCLSCR in its off state.

TABLE I
THE HBM AND MM ESD LEVEL OF THE VDD-TO-VSS ESD CLAMP CIRCUIT WITH THE PROPOSED LOW-LEAKAGE DIODE STRING WITH DIFFERENT NUMBER OF STACKED DIODES.

Designs / ESD Level	A single NCLSCR	NCLSCR + 2 diodes	NCLSCR + 4 diodes	NCLSCR + 6 diodes	NCLSCR + 8 diodes	NCLSCR + 10 diodes
HBM ESD Level	> 8KV	> 8KV	> 8KV	> 8KV	> 8KV	> 8KV
MM ESD Level	1600V	1350V	1100V	850V	650V	500V
Failure criterion : $I_{leakage} > 1\mu A$ @ Vbias = 6V						

B. ESD Robustness

The fabricated diode strings among different designs had been verified by the *Zapmaster* ESD tester in both the human-body-model (HBM) and the machine-model (MM) ESD stresses. The HBM and MM ESD robustness of the VDD-to-VSS ESD clamp circuit, as shown in Fig. 5 with different number of stacked diodes, is listed in Table I. The failure criterion to identify the ESD level is defined as the leakage current of the low-leakage diode string after ESD stress greater than 1 μA under 6-V voltage bias. As seen in Table I, the VDD-to-VSS ESD clamp circuits with different number of the stacked diodes can all sustain the ESD stress of greater than 8 kV in the HBM ESD test. But, the MM ESD level of this design decreases when the number of the stacked diodes increases. The diode string in the forward-biased condition can sustain a high ESD level, due to its low operating voltage level in the forward-biased condition. For the typical application in the 3-V CMOS IC, the new proposed low-leakage diode string with an NCLSCR and 4 diodes (which has a total blocking voltage of 4.16 V at the temperature of 125°C) can sustain an HBM (MM) ESD level of >8 kV (1100 V), which is much higher than the HBM (MM) ESD specification of 2 kV (200 V) in the general consumer IC products.

The ESD levels of the previous designs, including the *Cladded diode string* with six diodes, the *Boosted diode string* with eight diodes, and the *Cantilever diode string* with six diodes are also investigated by the ESD tester as a reference. The HBM and MM ESD levels of those designs are listen in Table II. Because those previous designs initially have larger leakage currents, the failure criterion is therefore defined as the relative 10% shift on the voltage at $I = 1$ μA of their original *I–V* curves. The original voltage levels at $I = 1$ μA in the *Cladded diode string* with six diodes, the *Boosted diode string* with eight diodes, and the *Cantilever diode string* with six diodes are 2.4, 1.6, and 2.2, respectively, before any ESD stress on the fabricated test chip. Each diode used in those previous designs has the same device dimension and layout style as that used in the proposed low-leakage diode string. As

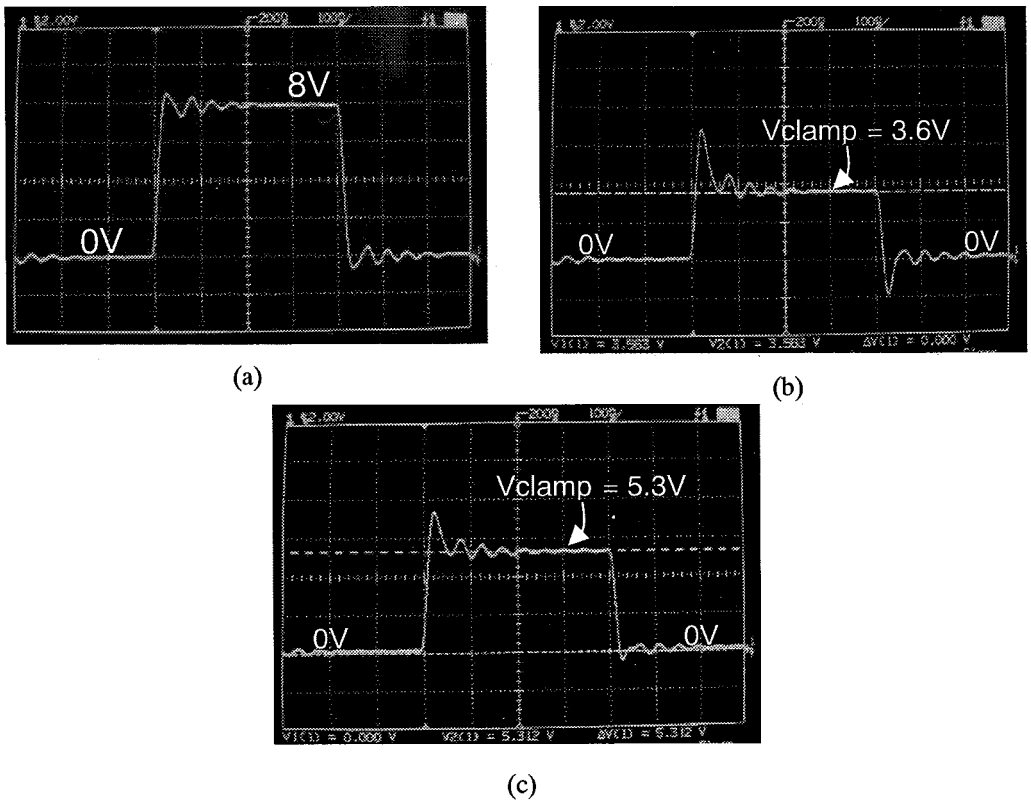


Fig. 11. The voltage waveforms of: (a) the original 0–8-V voltage pulse, (b) the degraded voltage pulse clamped by the VDD-to-VSS ESD clamp circuit with an NCLSCR and twostacked diodes, and (c) the degraded voltage pulse clamped by the VDD-to-VSS ESD clamp circuit with an NCLSCR and sixstacked diodes. (Y axis $=$ 2 V/div., X axis $=$ 100 ns/div.).

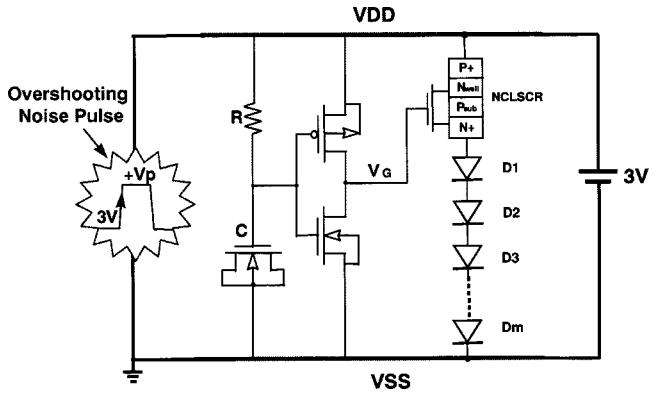


Fig. 12. The experimental setup to verify the latch-up issue of the VDD-to-VSS ESD clamp circuit with the new low-leakage diode string under 3-V VDD bias and a coupled overshooting noise pulse on the VDD power line.

TABLE II
THE HBM AND MM ESD LEVEL OF THE VDD-TO-VSS ESD CLAMP CIRCUIT WITH THE PREVIOUS DESIGNS IN FIG. 3

Designs / ESD Level	Cladded Diode String (6 diodes)	Boosted Diode String (8 diodes)	Cantilever Diode String (6 diodes)
HBM ESD Level	> 8KV	4.5KV	> 8KV
MM ESD Level	1200V	450V	500V

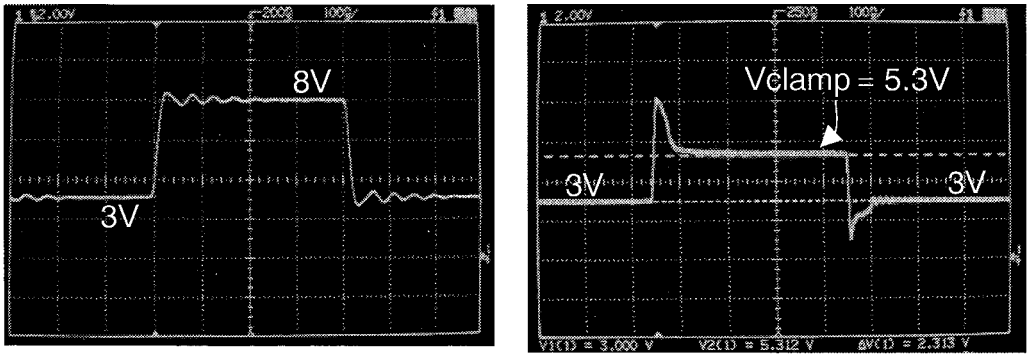
Failure criterion : V (@ 1μA) shift > 10%

seen in Table II, the *Boosted diode string* with eight diodes has an HBM (MM) ESD level of only 4.5 kV (450 V).

From comparing the ESD results between Tables I and II, the new proposed diode string can still maintain the excellent ESD robustness of the diode string but with a very low leakage current from VDD to VSS. For applications in the 3.3-V CMOS IC's, the leakage current, the HBM and MM ESD robustness, and the occupied silicon area between the proposed low-leakage diode string (an NCLSCR+4 stacked diodes) and the *Cantilever diode string* with six stacked diodes are compared in Table III. The proposed low-leakage diode string (an NCLSCR + 4 stacked diodes) under 3.3-V bias at the temperature of 125 °C has a leakage current of only 1.08 nA, whereas the *Cantilever diode string* with six stacked diodes has a leakage current of up to 1.25 mA. Therefore, this new proposed low-leakage diode string has a much smaller leakage current, smaller silicon area, but higher ESD robustness, as comparing to those previous designs.

C. Turn-On Verification

A voltage pulse generated from a pulse generator (*HP*8118A) with a pulse height of 8 V and a rise time of ∼10 ns is used to simulate the rising edge of an ESD pulse. Such a voltage pulse is



(a) (b)

Fig. 13. (a) The voltage waveform the original 3–8-V voltage pulse, and (b) the degraded voltage waveform clamped by the VDD-to-VSS ESD clamp circuit with an NCLSCR and four stacked diodes. (Y axis $=$ 2 V/Div., X axis $=$ 100 ns/Div.).

TABLE III
PERFORMANCE COMPARISON BETWEEN THE *CANTILEVER DIODE STRING* AND THE PROPOSED LOW-LEAKAGE DIODE STRING FOR APPLICATION IN 3.3-V CMOS IC's IN A 0.35-μm SILICIDE CMOS PROCESS

Performance / Designs	Leakage Current at 3.3V and 25°C	Leakage Current at 3.3V and 125°C	HBM ESD Level	MM ESD Level	ESD Active Area (μm²)
Low-Leakage Diode String (NCLSCR + 4 diodes)	24.15 pA	1.08 nA	> 8KV	1100V	80 ×70.3
Cantilever Diode String (6 diodes)	4.96 μA	1.25 mA	> 8KV	500V	80×79.2

applied to the floating VDD power line to verify the turn-on behavior of the VDD-to-VSS ESD clamp circuit with the proposed low-leakage diode string. The measured voltage waveforms are shown in Fig. 11. The voltage waveform of the original 0-8-V voltage pulse is shown in Fig. 11(a), which is generated from the pulse generator. When this voltage pulse is applied to the VDD-to-VSS ESD clamp circuit with the proposed low-leakage diode string, the rising edge of the voltage pulse is detected by the RC-based ESD detection circuit which triggers on the diode string to clamp the overstress voltage. The voltage waveform clamped by the low-leakage diode string with an NCLSCR and 2 stacked diodes is shown in Fig. 11(b), where the voltage level on the VDD power line is clamped to 3.6 V with a turn-on time about ~20 ns to fully turn on the low-leakage diode string. The voltage waveform clamped by the low-leakage diode string with an NCLSCR and four stacked diodes is shown in Fig. 11(c), where the voltage level on the VDD power line is clamped to 5.3 V.

When the IC is under the normal operating condition, the VDD is biased at 3 V and the VSS is biased at 0 V in the 3-V applications. But, the system-level noise pulses may couple to the VDD of the IC to cause an overshooting voltage pulse on the VDD power line. The ESD clamp circuit for placing between the VDD and VSS power lines should be verified in such a condition to make sure that the ESD clamp circuit does not cause latch-up danger between the power lines. The experimental setup to verify this issue is shown in Fig. 12, where a 3–8 V voltage pulse with a rise time of ~10 ns is used to simulate the overshooting noise coupled to the power line. Such an overshooting voltage pulse is applied to the 3-V biased VDD power line to verify the turn-on behavior of the ESD clamp circuit with the low-leakage diode string. The voltage waveform of the original 3–8-V voltage pulse with a pulse width of 400 ns to simulate the overshooting noise pulse is shown in Fig. 13(a). When this voltage pulse is applied to the ESD clamp circuit with the 3-V VDD bias, the low-leakage diode string in the ESD clamp circuit can be turned on to clamp the overshooting voltage pulse on the VDD power line. The voltage waveform clamped by the VDD-to-VSS ESD clamp circuit with an NCLSCR and four stacked diodes is shown in Fig. 13(b), where the voltage level on the VDD power line is clamped to 5.3 V which is corresponding to its total blocking voltage of the low-leakage diode string. After the triggering of the overshooting voltage pulse, the diode string with a total blocking voltage greater than VDD can automatically turn itself off. In Fig. 13(b), the VDD power line is automatically restored to the 3-V voltage level after the triggering of the overshooting voltage pulse. This verifies that the low-leakage diode string with an NCLSCR device in the VDD-to-VSS ESD clamp circuit can clamp the overshooting noise pulse but without causing latch-up problem to the IC, when the IC is operating in the normal condition.

D. Applications

Such a new diode string can be widely applied for whole-chip ESD protection in the CMOS IC's with separated power lines or mixed-voltage power supplies. When a CMOS IC has multiple VDD power supplies, such as 3.3 and 5 V, the whole-chip ESD protection scheme with the new low-leakage diode string is illustrated in Fig. 14. Three low-leakage diode string and their corresponding control circuits are placed among the VDD1, VDD2, and VSS to achieve the whole-chip ESD protection.

Another whole-chip ESD protection scheme, by using the concept of multiple ESD buses [34], can be also realized with the proposed low-leakage diode string, as shown in Fig. 15. The additional ESD buses are provided to quickly discharge the ESD current away from the internal circuits, especially in the pin-to-pin ESD zapping. Between the VDD (VSS) ESD bus and the separated VDD (VSS) power lines, there are ESD conduction circuits connecting to each other to discharge the ESD stress across different circuit blocks. The ESD conduction circuit was often realized by the bi-directional back-to-back diodes [35]. But, when the separated power lines have different voltage levels, such as 3.3 and 5 V, the bi-directional back-to-back diodes are not suitable. The low-leakage diode

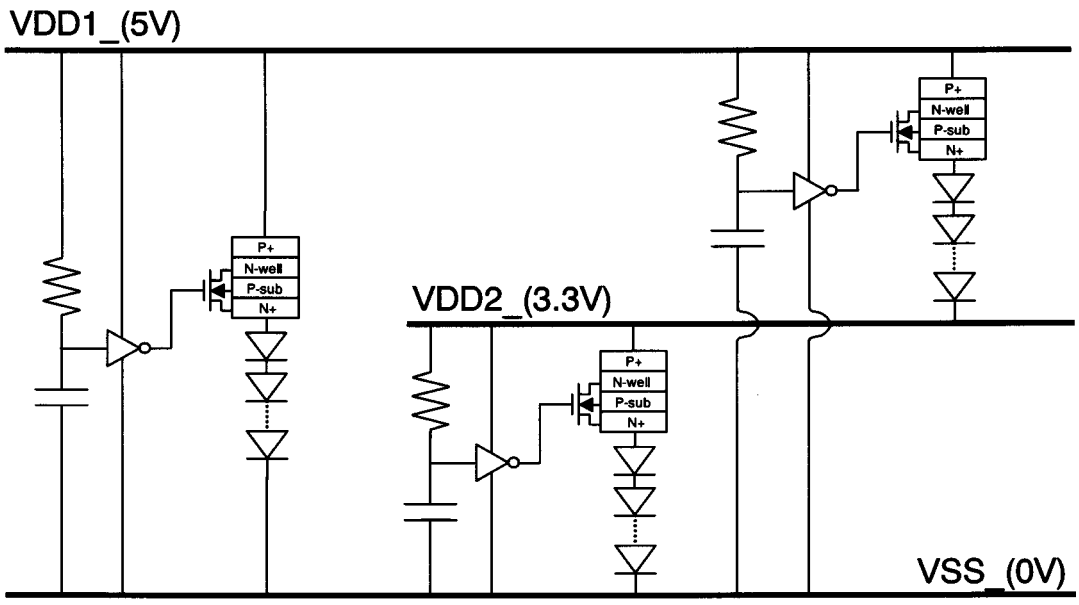


Fig. 14. The application of the new low-leakage diode string for using in the ESD clamp circuits between different power rails, which have different VDD voltage levels in a CMOS IC.

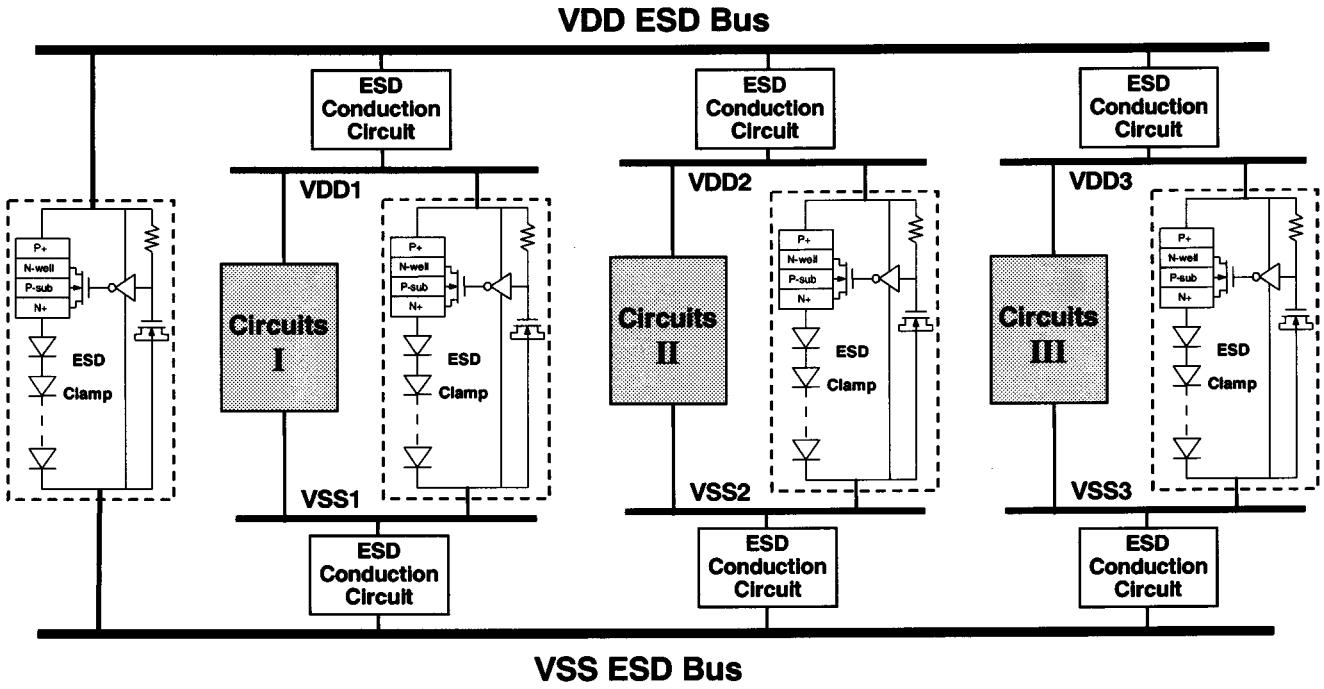


Fig. 15. Another application example of the new low-leakage diode string in a CMOS IC to achieve the whole-chip ESD protection scheme with the VDD and VSS ESD buses.

string can be therefore used in such ESD conduction circuits to bypass ESD current through the ESD buses to avoid ESD damage located on the internal circuits of the IC. But, such diode strings are kept off with a very low leakage current ($\sim$nA) between the separated power lines, when the IC with mixed-voltage power supplies is under the normal operating condition.

V. Conclusion

A new design on the low-leakage diode string, by using an NCLSCR to block the leakage current, has been successfully verified in a 0.35-μm silicide CMOS process and compared to the previous designs. The proposed low-leakage diode string with an NCLSCR and four stacked diodes can provide a total blocking voltage of 4.16 V and a leakage current of only 1.08 nA at the temperature of 125 °C for safe application in the 3.3-V CMOS IC's without causing latch-up danger. The low-leakage diode string with an NCLSCR and four stacked diodes can sustain the HBM (MM) ESD stress of >8 kV (1100 V) in a silicon area of 80×70.3 μm^2 in a 0.35-μm silicide CMOS process without using the ESD-implantation and silicide-blocking process modifications. This low-leakage

diode string for using in the power-rail ESD clamp circuit has the advantages of very low leakage current, smaller silicon area, higher ESD robustness, and no latch-up danger. Thus, this new low-leakage diode string is very suitable for using in the on-chip ESD protection circuits of CMOS IC's for low-power or portable applications.

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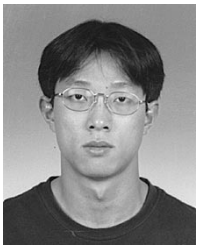

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