Numerical Simulation of Sidegating Effect in GaAs MESFET's

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***Abstract*—Two-dimensional simulation of the sidegating effect in GaAs MESFET's has been performed. The result confirms that Schottky contacts on a semi-insulating substrate cause serious high substrate leakage current and drain current reduction in GaAs MESFET's. The threshold behavior in sidegating effect is found to correlate with the conduction behavior of the Schottky-i-n(sidegate) structure when the sidegate is negatively biased. Shielding and enhancement of the sidegating effect by the Schottky contacts have also been studied and the results agree with the experimental findings. Besides, the presence of hole traps in the semi-insulating substrate is found to be essential to the sidegating effect.**

I. Introduction

In GaAs integrated circuits, the drain current of a FET can drop significantly when a negative voltage is applied to an adjacent device or an electrode. The reduction of the drain current is usually accompanied by an increase of the leakage current between the FET and the adjacent electrode (called the sidegate). [1] This so-called sidegating effect usually has a threshold, i.e., the FET current is reduced only when the negative-sidegate voltage exceeds certain threshold V_{sgt}. The sidegating effect, which can cause coupling or crosstalk between adjacent MESFET's, is a key problem that impedes the advance in integration level and extensive application of complex GaAs IC's made on semi-insulating substrates. This effect depends on material, processing, and circuit layout. It is temperature-dependent [2] and light-sensitive [3]. It has a strong impact on device performance and circuit yield.

Based on experimental results, several models for the sidegating effect have been proposed, including the trap-fill-limited carrier injection model [1] and the surface avalanche breakdown model [4]. Impact ionization of traps in the substrate [5] has also been included in sidegating to explain the hysteresis and the S-type negative differential conductivity (S-NDC) associated with the threshold behavior of sidegating when measurements are made in the voltage-controlled condition and the current-controlled condition, respectively. However, a model which can consistently account for all the observed features of sidegating effect remains to be established.

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Recently, it has been recognized by both experiments [6] and numerical simulations [7] that Schottky contacts on semi-insulating (SI) substrates play a very important role in the sidegating effect. This contact could be just a portion of the Schottky gate of a MESFET, or the Schottky shielding bar inserted on purpose to suppress the sidegating effect [8]. Previous reported simulation results by Goto *et al.* [7], [9], [10] have suggested the existence of the hole traps in an SI substrate, or an injection of holes into an SI substrate could be the origin of the sidegating effect. However, in the simulation they used a backgate configuration, where the sidegate terminal is placed at the back surface of the substrate. This configuration, which differs from the real situation where all the devices are on the front surface, makes the comparison between simulations and experiments difficult and might lose some insight of what really happens.

In this work, a true sidegate configuration is adopted, where the sidegate is placed at the top surface of the substrate along with all other contact terminals. The sidegating is then analyzed by a two-dimensional numerical simulation. The effects of the deep levels and the influence of the Schottky contacts on the sidegating effect in GaAs MESFET's are studied in detail. The role that hole traps play in the sidegating effect is also investigated.

II. Models for Simulation

For the numerical simulation, a two-dimensional, two-carrier device simulation program based on the drift-diffusion formulation was developed. In this program, transport of free carriers is calculated by solving current continuity equations and the Poisson's equation. The emission and capture of free carriers through deep traps in the substrate follow the Shockley–Read–Hall model.

Parameters used for the simulation are given in Table I. Constant electron mobility at low fields and velocity saturation beyond a critical field was used for the velocity–field relationship in simulation to avoid the complication due to negative resistance. The semi-insulating substrate was assumed to contain deep donors which compensate for shallow acceptors. The shallow acceptor concentration was taken to be 10^{15} cm^{-3}, which is about the concentration level of residual carbons in undoped LEC GaAs substrates. Two types of midgap donors were in-

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TABLE I
PARAMETERS USED

Temperature	300 K
Energy gap	1.424 eV
Relative dielectric constant	13.1
Electron mobility $\mu_{on}/(1 + (\mu_{on} * E/V_{sn}))$ cm^2/V · s	
Hole mobility $\mu_{op}/(1 + (\mu_{op} * E/V_{sp}))$ cm^2/V · s	
$\mu_{on} = 5000$ cm^2/V · s $\mu_{op} = 300$ cm^2/V · s	
$V_{sn} = 1.5 \times 10^7$ cm/s $V_{sp} = 10^7$ cm/s	
E = electric field in V/cm	
Schottky-barrier height	0.80 eV

TABLE II
CONDITIONS RELATED TO TRAPS

Cases of Substrates		Electron trap $C_n = 1 \times 10^{-13}$ cm^2 $C_p = 3 \times 10^{-16}$ cm^2		Hole trap $C_n = 3 \times 10^{-16}$ cm^2 $C_p = 1 \times 10^{-13}$ cm^2
	$E_c - E_t$(eV)	N_t(cm^{-3})	$E_c - E_t$(eV)	N_t(cm^{-3})
HTR	0.715	1×10^{15}	0.745	1×10^{16}
ETR	0.715	1×10^{16}	0.745	1×10^{15}
ET	0.715	1.1×10^{16}	—	0
HT	—	0	0.745	1×10^{16}

*C_n: capture cross-section of electrons.
*C_p: capture cross-section of holes.

cluded: one is an electron trap and the other is a hole trap. According to the relative concentrations of electron traps and hole traps listed in Table II, four different substrate conditions; namely, electron-trap rich (ETR), hole-trap rich (HTR), electron trap only (ET), and hole trap only (HT) cases were simulated. HT and HTR substrates might not seem to be realistic, but the results can provide comparison and help clarify the real situation.

Two device structures, shown as structures A and B in Fig. 1 were investigated in our simulation. The FET's had a 1-μm gate with a 3-μm source-to-drain spacing. The FET's channel was 0.12 μm thick and was uniformly doped to 10^{17} cm^{-3}. The sidegate and the FET terminals were all placed on the top surface of the substrate in both structures. In structure A, the sidegate was placed at 7 μm away from the FET. In structure B, the sidegate was 7 μm away but a 1 μm-wide Schottky bar contacting the semi-insulating substrate was added in-between the FET and the sidegate, simulating either a portion of the gate or a shielding bar. The drain voltage and the gate voltage were set at 1 and 0 V, respectively.

III. CALCULATIONS WITHOUT A SCHOTTKY BAR

First, in order to see the relationship between the sidegating effect and the substrate conditions, structure A shown in Fig. 1 was simulated with four different substrate conditions: HT, HTR, ETR, and ET.

The obtained drain current I_{dss} at a drain voltage of 1 V, and sidegate leakage current I_{bg} as functions of the negative sidegate voltage are plotted in Fig. 2(a) and (b), respectively. In the case of HT, where the substrate contains only hole traps, I_{dss} decreases rapidly starting from zero sidegate voltage. In the case of HTR, where the substrate is hole-trap-rich but with the addition of some electron traps, I_{dss} still decreases without threshold, but with a smaller reduction rate. On the other hand, in the case of

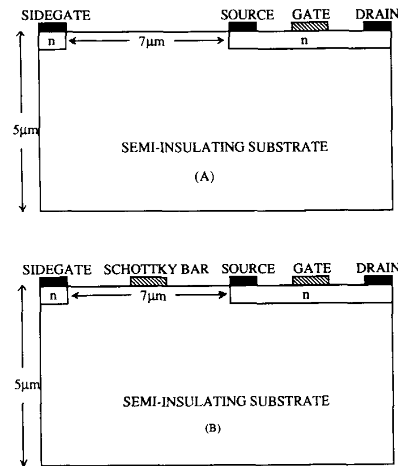


Fig. 1. Device structures used for numerical simulations. The drain (D), gate (G), source (S) contacts of the MESFET, the Schottky bar (SB), and the sidegate terminal (SG) are all placed on the top surface of semi-insulating substrate.

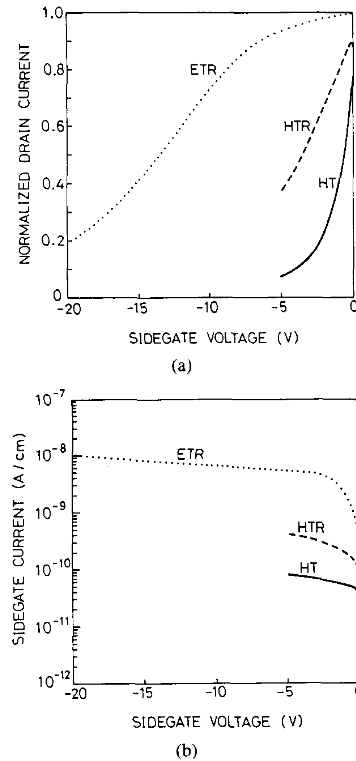
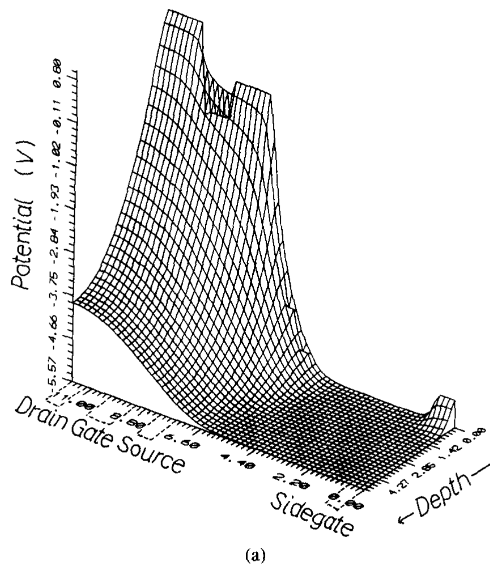
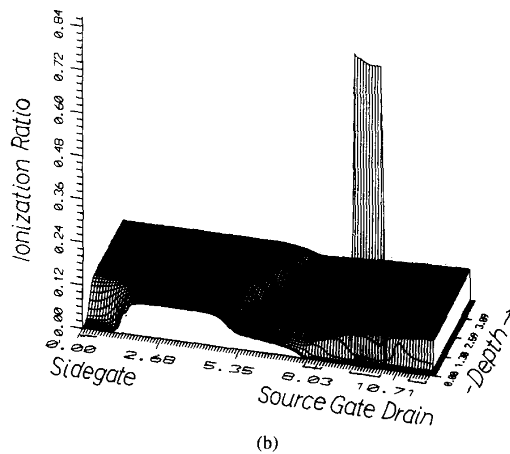


Fig. 2. Calculated (a) FET drain current and (b) sidegate leakage current in structure A (without Schottky bars) for the cases of HT (solid line), HTR (dashed line), and ETR (dotted line) substrates. The drain currents are normalized by the drain current of the ETR case at zero sidegate voltage.

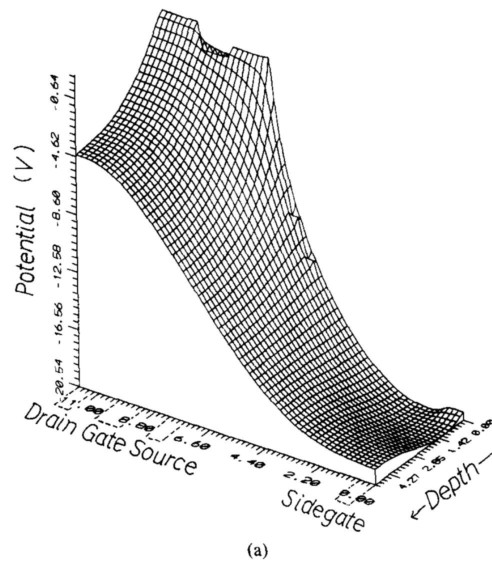


(a)

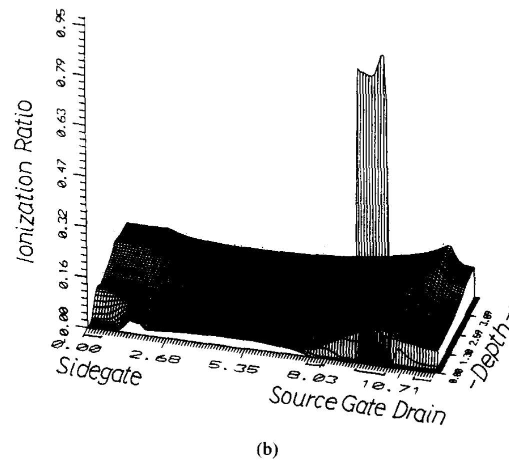


(b)

Fig. 3. (a) The potential profile and (b) the distribution of the ionization ratio of deep donors in the HTR substrate. The sidegate is biased at −5 V.



(a)



(b)

Fig. 4. (a) The potential profile and (b) the distribution of the ionization ratio of deep donors in the ETR substrate. The sidegate is biased at −20 V.

ETR, where the substrate is electron-trap-rich, the sidegating effect is much reduced and the reduction of the drain current increases with the negative sidegate voltage. The leakage current between the sidegate and the FET is higher for the substrate which is electron-trap-rich. However, steep rise in the sidegate current is not observed. The results of the ET case, where the substrate contains only electron traps, are very close to those of the ETR case and thus not shown in the figure.

In order to see the effects of electron and hole traps on the potential distribution in the substrate, profiles of the potential and the ionization ratio of deep donors (including both electron and hole traps) inside the substrate after the drain current is seriously reduced are shown in Figs. 3, and 4 for the HTR and ETR cases, respectively. In these substrates, the ionization ratio of $N_{dd}^{+}/N_{dd} = 10^{15}/1.1 \times 10^{16}$ (about 0.1) corresponds to the electrical neutrality of the substrate, and $N_{dd}^{+}/N_{dd} = 0$ corresponds to the fully negatively charged state of the substrate, caused by the electron occupation at the deep levels together with the ionization of shallow acceptors. In the case of the HTR substrate, there is an almost flat potential region in the sidegate side of the semi-insulating substrate (see Fig. 3(a)). The potential of this flat region follows the negative sidegate voltage and, therefore, a large voltage drop occurs near the FET. From the distribution of ionized deep levels shown in Fig. 3(b), we can see that, because of the negative voltage applied to the sidegate, holes are emitted from the hole traps near the channel/substrate interface leaving behind a negative charged and hole-depleted region close to the FET channel. This negative space-charge region is partially balanced by a positive space-charge region in the channel of the FET and therefore causes the reduction of its drain current.

In the case of ETR substrate, the potential profile is almost linearly graded throughout the substrate (see Fig. 4(a)). Because of this linearly graded potential distribution, it takes a higher (more negative) voltage to create the same amount of voltage drop near the FET channel as in the HT and HTR cases. So the sidegating effect is much smaller in this type of substrate. Owing to the difference in trap types, the potential distribution observed here is similar to that of a n-n$^-$-n structure while those of the HT and the HTR substrates are similar to that of an n-p$^-$-n structure. This explains why the leakage current in the ETR case is higher than those in the HT and the HTR cases (see Fig. 2(b)). From the profiles of ionized deep donors, shown in Fig. 4(b), we can see that in the ETR case, because of the electrons which are injected from the sidegate and trapped in the electron traps, the ionization ratio of deep donors is close to zero near the surface of the whole substrate and a negatively charged region is formed there due to the electron occupation of deep donors and the ionization of shallow acceptors. This is quite different from the HTR case, where the substrate is negatively charged only in the regions right beneath the FET and the sidegate.

IV. Calculations With Schottky Bars

The influence of Schottky bars contacting the SI substrate on sidegating effect was studied by performing 2D simulations on structure *B* (see Fig. 1). The sidegating characteristics were analyzed with different voltages applied to the Schottky bar inserted between the FET and the sidegate. This Schottky bar can be regarded as a part of the Schottky gate which extrudes out of the active region and contacts the SI substrate or any interconnection metal which contacts the substrate. The Schottky bar can also be a shield for the sidegating effect as reported in [8]. Since conventional LEC semi-insulating GaAs substrates are electron-trap-rich, the simulations were performed on ETR substrates.

The obtained drain currents I_{dss}, as a function of the negative sidegate voltage for the cases without and with a biased Schottky bar, are plotted in Fig. 5. It can be seen from these curves that, with the presence of the biased Schottky bar, the sidegating effect is greatly enhanced and there is a distinct threshold (V_{sgt}) for the effect. The drain current of the FET drops drastically when the sidegate voltage exceeds the threshold. This result confirms the recent finding by Liu *et al.* [6] and Goto *et al.* [7]. The increase in I_{bg} and the decrease in I_{dss} are much more abrupt for the structure with a Schottky bar.

The effect of different biases on the Schottky bar on the sidegating effect has also been simulated. Fig. 6(a) shows the calculated sidegating characteristics with the Schottky bar biased at +1, 0, −1, −2, and −3 V. Sidegating effect is greatly enhanced by the positive voltage applied to the Schottky bar and is reduced by the negative voltages applied to the bar. The value of the sidegating threshold voltage V_{sgt} increases with the negative bias of the Schottky bar. This result agrees qualitatively with the experimental observation reported by Lee and Chang, who have suggested to use negatively biased Schottky bars as shields for the sidegating effect [8]. The corresponding sidegate leakage currents I_{bg} are shown in Fig. 6(b). Unlike in cases without Schottky bars, the leakage current increases abruptly at the threshold or the onset of sidegating. This abrupt change in leakage current and the accompanied sidegating threshold agree with the experimental findings on the threshold behavior of the sidegating effect [1]–[3], [6], [8], [12].

To inquire further into the threshold behavior of the

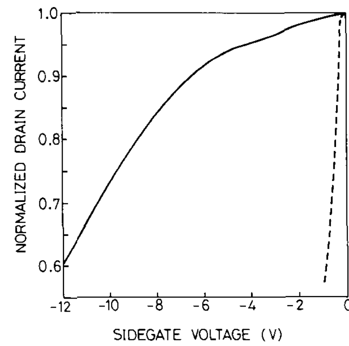


Fig. 5. Calculated FET drain current as a function of the negative sidegate voltage for the cases without (solid line) and with (dashed line) a Schottky bar biased at 0 V.

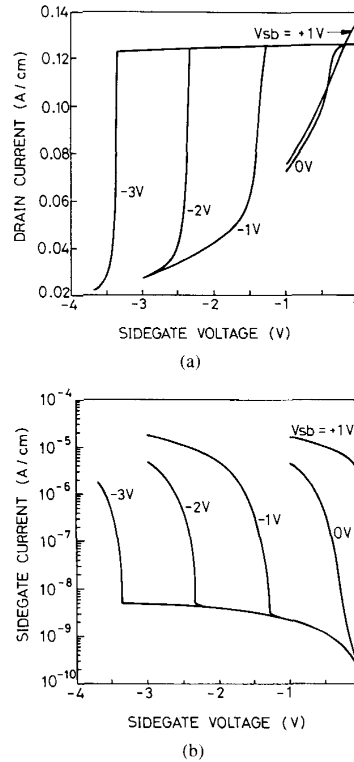


Fig. 6. Calculated (a) drain currents and (b) sidegate currents in structure *B* with the Schottky bar biased at +1, 0, −1, −2, and −3 V.

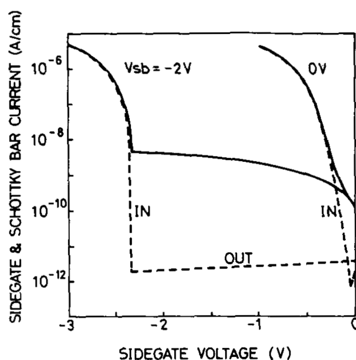


Fig. 7. The sidegate current (solid line) and the value of the Schottky bar current (dashed line) in structure B with the Schottky bar biased at 0 and −2 V. Direction of the current flow through the Schottky bar is explicitly marked as IN or OUT.

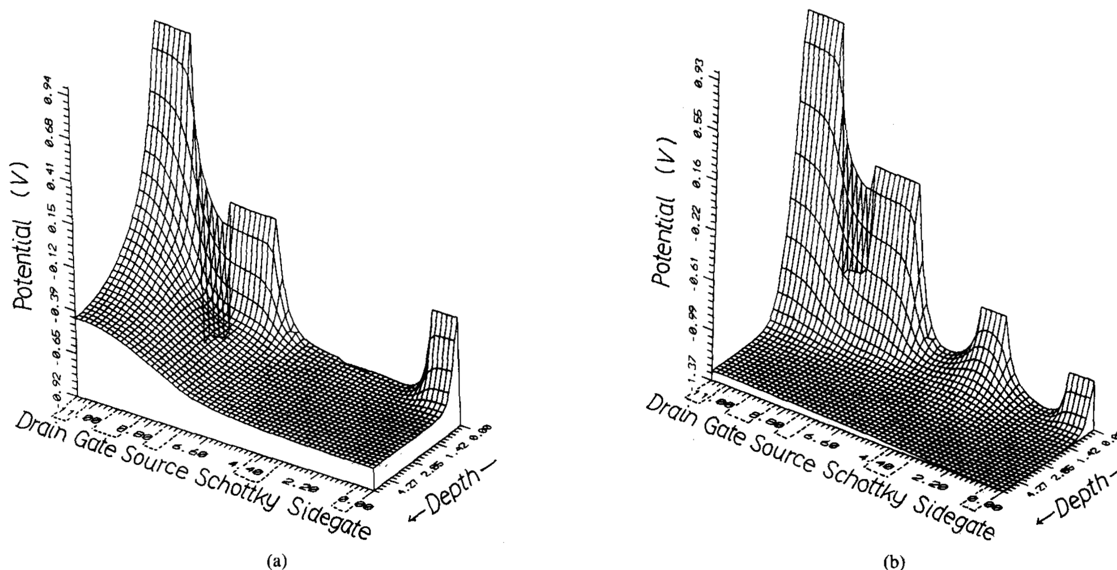


Fig. 8. The potential profiles before (a) and after (b) the onset of sidegating in structure B with the Schottky bar biased at 0 V and the sidegate biased at −0.25 V (a) and −1 V (b), respectively.

sidegating effect, we have extracted the relevant leakage currents between the electrodes as functions of the sidegate voltage with the Schottky bar biased at 0 and −2 V. As shown in Fig. 7, we can see that before the onset of sidegating the current flow through the Schottky bar (I_{sb}) is much smaller than the total sidegate leakage current I_{bg}. However, at the sidegating threshold the Schottky current changes sign and goes up rapidly as the negative sidegate voltage increases. The sidegate leakage current now becomes dominated by the current going through the Schottky bar. Direction change of the Schottky current obviously occurs when the Schottky bar changes from a reverse-bias condition to a forward-bias condition. Before the sidegating threshold, the Schottky bar is reverse-biased and the current flows out of the contact. After the threshold, the Schottky bar becomes forward-biased and the current flows into the contact (from outside).

The potential profiles and the distributions of hole concentration before and after the onset of sidegating are shown in Figs. 8 and 9, respectively. Before the sidegating threshold, there is a nearly flat potential region and a hole accumulation region (the thermal equilibrium value of hole concentration is about 10^6 cm^{-3}) in the sidegate side of the SI substrate. After the sidegate voltage exceeds the sidegating threshold, the hole accumulation region extends and the potential becomes essentially flat in the whole i-substrate region. The negative sidegate voltage, which propagates to the vicinity of FET, causes the depletion of holes and thus a negatively charged region in the substrate side of the channel/substrate interface. Therefore, the channel electrons of the FET are depleted and the sidegating effect results.

In order to see the importance of hole traps in the sidegating effect, an ET substrate, which contains only

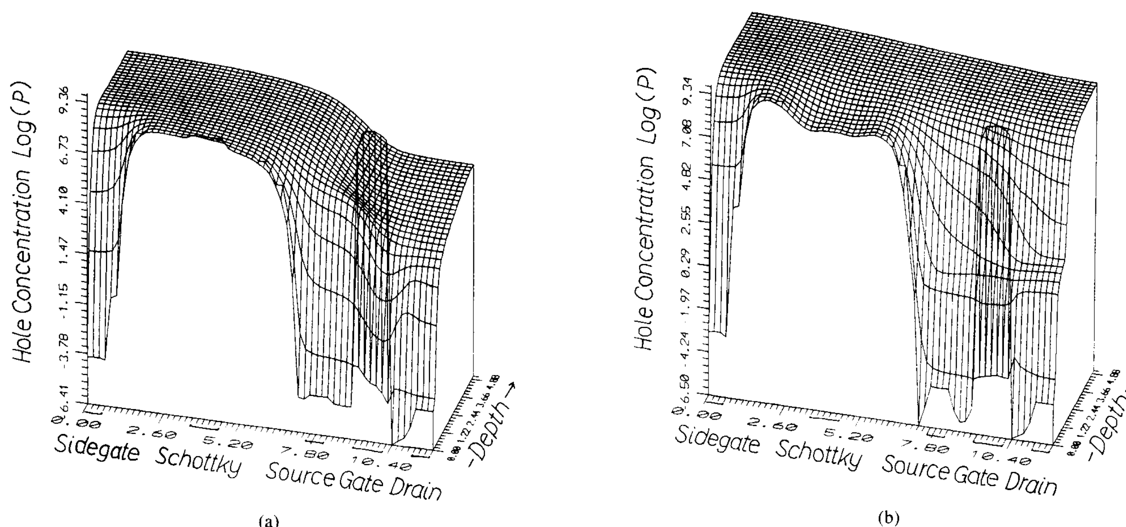


Fig. 9. The distributions of the hole concentration before (a) and after (b) the onset of sidegating in structure B with the Schottky bar biased at 0 V and the sidegate biased at -0.25 V (a) and -1 V (b), respectively.

electron traps, was simulated for comparison. In this case, the calculated sidegate current and the Schottky bar current vary with the sidegate voltage in a similar way as those in ETR substrates; however, the current level of these two currents is smaller than that of the ETR case by about two orders of magnitude and an apparent reduction in the drain current is not observed even after the Schottky current dominates the sidegate current. The hole accumulation region and nearly flat potential region are found to be confined to the substrate region between and under the Schottky bar and the sidegate.

V. Discussion

By comparing the reported experimental sidegating results [8], [12] with the curves simulated with and without Schottky bars, it can be confirmed that the Schottky contact on the SI substrate is responsible for the significant drain-current reduction and the high substrate leakage current observed in sidegating effects.

From results of the simulations which include the effect of Schottky contacts, a clear picture of the competition between the contact currents or biases can be drawn. The potential of the SI substrate around the Schottky bar is affected by the positive bias applied to the drain of the FET, the negative voltage applied to the sidegate, and the bias applied to the bar itself. Before the application of negative sidegate voltages, the Schottky current comes from the FET side and flows out of the Schottky contact as the reverse saturation current of the n(FET)-i-Schottky structure. When the applied sidegate voltage is low (relative to the bias of the Schottky bar), the current through the Schottky contact I_{sb} remains very small and the substrate leakage current is dominated by that between the FET and the sidegate. Only when the negative biases applied to the sidegate are large enough to overcome the effect of the drain bias of the FET, does the current between the Schottky contact and the sidegate begin to flow as it should in a forward-biased Schottky-i-n (sidegate) structure. After the onset of forward Schottky-i-n current, the Schottky bar current reverses sign and increases very rapidly, the sidegate current then becomes dominated by the current between the Schottky contact and the sidegate. It has been observed experimentally [13] that the direction of the gate current of a FET changes from flowing out to flowing in after the sidegating occurs. Since the Schottky gate contains a small portion that contacts the i-substrate directly, this result agrees with our simulation results.

As for the role that hole traps play in the sidegating effect, a qualitative description could be given as follows. After the onset of the forward Schottky-i-n (sidegate) current, some holes are injected into the SI substrate from the Schottky bar. In the presence of hole traps, holes accumulated in the substrate could spread to the FET side of the structure with the aid of the hole traps. As the Schottky-i-n current increases, the flat potential region extends from the sidegate to the FET, carrying the negative sidegate voltage to the vicinity of the FET, and resulting in a negatively charged region there by the emission of holes from hole traps in response to the hole depletion. On the contrary, when the SI substrate contains only electron traps, injected and accumulated holes are confined to the region between two conducting contacts (Schottky and sidegate), whereas injected electrons are transported to the FET side and fill the electron traps in the SI substrate around the FET.

VI. Conclusion

We have performed two-dimensional simulations on the sidegating effect in GaAs MESFET's with a realistic configuration, where both the FET and the sidegate are placed

on the surface of the substrate. Substrates which are electron-trap-rich are found to have very small sidegating effect compared with the substrates which are hole-trap-rich. Hole traps are found to be crucial in spreading out the negative voltages from the sidegate. However, in electron-trap-rich substrates, such as the normally used LEC undoped substrates, Schottky contacts on the semi-insulating substrate can induce sidegating effect and are found to be the major cause for the sidegating effect. The simulated results are qualitatively in good agreement with the observed sidegating features, including the enhancement and shielding of the sidegating effect and the abrupt changes in drain and sidegate leakage currents. The threshold behavior of the sidegating effect is found to be related to the leakage current of the Schottky-i-n(sidegate) structure under the influence from the biases of the FET. Both the injection of holes and the presence of hole traps are essential to the sidegating effect.

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