Fault coverage and defect level estimation models for partially testable MCMs

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Abstract: The authors propose a simple and efficient mathematical model for designers to estimate fault coverage for partially testable multichip modules (MCMs). This model shows a relation between fault coverage, test methodology, and the fraction and distribution of design for testability (DFT) dies in MCMs. Experimental results show that the proposed model can efficiently predict the fault coverage of a partially testable MCM with less than 5% deviation. An automatic DFT dies deployment algorithm, based on the genetic algorithm and the model is proposed to help designers to obtain a fault coverage as close to the upper bound of fault coverage as possible. Two defect level estimation models, which relate fault coverage and manufacturing yield for measuring the test quality of MCMs under equiprobable and non-equiprobable faults, respectively, are also formulated and analysed to support the effectiveness of the model.

1 Introduction

The increasing demand in circuit speed has motivated high-performance system development. A multichip module (MCM) which interconnects multiple bare dies onto a substrate provides potential advantages of high chip densities, small interconnection delays and high system performance. The merits of MCMs are gained from the elimination of a level of package (IC package). However, it is the same reason that dense packaging complicates the manufacturing and testing processes. General MCM testing strategies involve testing dies individually before they are assembled and testing the assembled module to avoid faults introduced during packaging [1]. However, it is difficult to test the bare die completely due not only to the increasing growth of pin count but also to the shrinking size of I/O pads. Traditional IC test equipment that is used to test the cased IC is not feasible for bare die testing, because there are no commercially available sockets that can hold a single die [2]. This gives rise to a need to add a design for testability (DFT) feature to each die, if possible, to provide necessary MCM testing capability.

Although design for testability techniques can enhance controllability and observability to solve many chip level testing problems in MCMs, the obvious penalty is the overhead. They not only increase design cost and chip area but also degrade circuit performance. As a result, not all chips in an MCM have design for testability features [3]. For instance, memory chips such as Cache-SRAMs and TAG-SRAMs, which have been used in Pentium MCM systems, are typical examples of not supporting design for testability for the reasons mentioned [4]. In addition, the very hybrid nature of MCMs allows different sources of dies to be incorporated into a single module. This implies that, except for vertically integrated companies, the quality of dies within the module cannot be assured and so the authors cannot be sure that each die is designed to have DFT features with it [5]. This means that, although the quality of bare dies is critical to the economy of high-yield assembly of MCMs [6], the MCM market cannot afford 100% product testability [5] and partially testable MCMs (PT-MCMs) still exist currently. This results in fault detection and diagnosis of MCMs being intractable.

Fault coverage (FC), defined as the fraction of defective dies detected in an MCM, is an important parameter in measuring test quality. However, in PT-MCMs, the fault coverage not only depends on the ingenuity of test methodologies but also depends on the fraction and the distribution of DFT dies. This is because the controllability and observability of NDFT dies (dies with no design for testability feature) can be enhanced by the DFT dies (dies with design for testability feature) around them. Until now, MCM designers rarely considered fault coverage issues when they are given a fixed fraction of DFT dies for PT-MCMs. This paper develops a fault coverage estimation model for facilitating designers to deploy the DFT dies in PT-MCMs in an efficient way, in order to increase the fault coverage of PT-MCMs. In addition, two defect level estimation models for MCMs under equiprobable and non-equiprobable faults, respectively, are also proposed. The defect level, defined as the fraction of MCMs that are defective and are shipped for use after testing is completed, is a function of fault coverage and manufacturing yield for measuring the test quality of MCMs.

2 Preliminaries

2.1 Background

Based on the testability feature, the dies used in a PT-MCM can be divided into two categories: dies with DFT feature and dies without any testability feature. Owing to the nature of high circuit density and small pad size of MCMs, the DFT techniques, such as boundary scan (BS) and built-in self test (BIST), are increasingly more accepta-

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ble [1, 5, 7]. In this paper, the authors follow the assumptions in [1, 5] where MCMs are populated by dies belonging to two categories: (i) dies designed with chip level BS where some of them possibly including BIST feature (DFT dies) and (ii) dies with no DFT feature (NDFT dies) [5].

DFT dies can test themselves and can also increase the controllability and observability of NDFT dies around them. Therefore, if the the fraction of DFT dies is increased, the controllability and observability of NDFT dies are increased. As a result, the testability and fault coverage for PT-MCMs are enhanced. In addition, the controllability and observability of NDFT dies can be increased by distributing the DFT dies more uniformly, due to the fact that the scattering of DFT dies will increase the contact pads between DFT dies and NDFT dies. Fig. 1 illustrates two PT-MCM designs with the same number of DFT dies. Interconnections are assumed to exist between neighbouring dies. The functions of these two designs are the same except for the testability feature in each die. The shaded squares represent NDFT dies and the others are DFT dies. It is clear that the testability of the design in Fig. 1*b* is higher than that in Fig. 1*a*. This is because the distribution of DFT dies in Fig. 1*b* is more uniform than that in Fig. 1*a*.

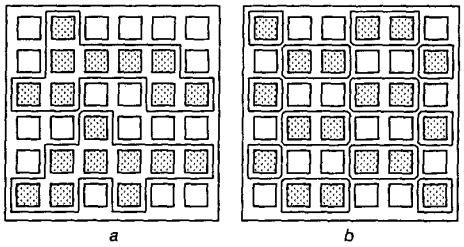

Fig. 1 *Two PT-MCM designs with different testability features*

2.2 Basic definitions and assumptions

The fault model for PT-MCMs is assumed at die level. The interconnection faults between dies are ignored and the dies in PT-MCMs are assumed to have equal probability of faults. Consider a sample MCM with n dies, among which n_1 is the number of DFT dies and n_2 is the number of NDFT dies. *DFT%* is defined as the fraction of DFT dies in an MCM and *NDFT%* as the fraction of NDFT dies in an MCM. A logic cluster is a cluster of NDFT dies which are enclosed by DFT dies and/or I/O pins only. For example, Figs. 1*a* and *b* show two PT-MCM designs with two and twelve logic clusters, respectively, as indicated by enclosed regions. The number and size of logic clusters are very important to represent the fraction and distribution of DFT dies in a PT-MCM. This is enlightened by the observation that the size of a logic cluster will shrink by scattering the DFT dies uniformly. In addition, the size as well as the number of logic clusters will both decrease by increasing the fraction of DFT dies. Owing to low controllability and observability of the logic clusters' internal logic, existing test methodologies [5, 8] for PT-MCMs can only identify faulty logic clusters. Faulty dies in a logic cluster cannot be identified, and this means that, if a logic cluster is identified as faulty, it is only certain that there is at least one faulty die in the logic cluster.

The undetectable degree (*u-degree*) of the ith logic cluster C_i is defined as the number of NDFT dies ($|C_i|$) in the logic cluster minus one, which can be expressed as *u-degree* (C_i) = $|C_i| - 1$ for $i = 1, 2, ..., t$, where t is the total number of logic clusters. The reason to minus one from the size of a logic cluster for *u-degree* is to reflect the fact that the faulty die of a logic cluster with size of 1 can be identified, and a faulty logic cluster with size greater than 1 can be identified if there is at least one faulty die in the logic cluster. *u-degree* is a very important parameter for indicating the distribution of DFT dies. Now, the distribution of the two PT-MCM designs in Fig. 1 will be quantitatively evaluated. The summation of *u-degree*s for all logic clusters in these two designs are $\Sigma_{i=1}^{2}(|C_i| - 1) = 16$ (Fig. 1*a*) and $\Sigma_{i=1}^{12}(|C_i| - 1) = 6$ (Fig. 1*b*), respectively.

3 Fault coverage estimation model

3.1 Fault coverage derivation

Let δ be a real number ranging from 0 to 1, which represents how smart a test methodology is. And N_f represents the number of defective dies in a PT-MCM. The mathematical expression to estimate the fault coverage (*FC*) for a PT-MCM is derived as follows:

$$
\begin{aligned}
FC &\equiv \frac{\text{number of defective dies detected}}{\text{number of defective dies in an MCM}} \\
&= \frac{\delta \times \left(\begin{array}{c}\text{number of defective dies} \\ \text{which are detectable}\end{array}\right)}{N_f} \\
&= \frac{\delta \times N_f \times \left(\begin{array}{c}\text{the fraction of detectable dies} \\ \text{in an MCM}\end{array}\right)}{N_f} \\
&= \delta \times (1 - (\text{the fraction of undetectable dies} \\
&\qquad\qquad \text{in an MCM})) \\
&= \delta \times \left(1 - \frac{\text{undetectable dies in an MCM}}{n}\right)
\end{aligned}
$$

Note that due to less controllability and observability of NDFT dies, the faulty dies in a logic cluster cannot be identified; which means that if a logic cluster is identified to be faulty, this only ensures that there is at least one faulty die in the logic cluster. Therefore, the number of undetectable dies in a logic cluster is $|C_i| - 1$. Thus, the total number of undetectable dies in an MCM is $\Sigma_{i=1}^{t}(|C_i| - 1)$ (i.e. summation of *u-degree*). The above expression can then be approximated as

$$
\begin{aligned}
FC &\approx \delta \times \left(1 - \frac{\left(\begin{array}{c}\text{summation of } u\text{-}degree \\ \text{in an MCM}\end{array}\right)}{n}\right) \\
&= \delta \times \left(1 - \frac{\sum_{i=1}^{t}(|C_i| - 1)}{n}\right) \\
&= \delta \times \left(1 - NDFT\% + \frac{t}{n}\right) \\
&= \delta \times \left(DFT\% + \frac{t}{n}\right)
\end{aligned}
\tag{1}
$$

This model shows that the fault coverage is in proportion to the fraction of DFT dies and is also in proportion to the number of logic clusters in a PT-MCM.

3.2 Upper bound of fault coverage

A given fixed fraction of DFT dies to estimate the upper bound of fault coverage is very important for designers to know when to stop the effort in deploying the DFT dies. It is trivial that the worst case of fault coverage for a PT-MCM is when all the DFT (NDFT) dies are clustered

together. This means that the number of logic clusters is exactly one ($t = 1$) and the worst case of fault coverage under a fixed $DFT\%$ for a PT-MCM can then be written as $FC_w = \delta \times (DFT\% + 1/n)$. When $n >> 1$, the equation can be simplified as $FC_w = \delta \times DFT\%$. Note that $FC_w = 0$ if there is no DFT die in an MCM, which is an extreme case with $DFT\% = 0$ and $t = 0$. On the other hand, if the size of each logic cluster is one (i.e. there are n_2 logic clusters with size of 1), then the best case of fault coverage under a fixed $DFT\%$ can be expressed as $FC_b = \delta \times (DFT\% + n_2/n) = \delta$. This equation shows the best case of fault coverage when each NDFT die is enclosed by DFT dies and/or I/O pins. Note that $FC_b = \delta$ is also applicable for the other extreme case with $DFT\% = 1$ and $n_2 = 0$.

In the following, two parameters are introduced to help the derivation of the upper bound of fault coverage. Suppose that k is the average number of DFT dies that encloses a logic cluster, and s is the maximum number of logic clusters that share a DFT die. Then we have $t \times k \leq n_1 \times s$. This inequality means that the total number of DFT dies that enclose all logic clusters is less than or equal to the total number of DFT dies multiplied by s. The upper bound of fault coverage (FC_u) can be derived as follows:

$$\begin{aligned} t \times k &\leq n_1 \times s \\ t &\leq n_1 \times \frac{s}{k} \\ \frac{t}{n} &\leq \frac{DFT\% \times s}{k} \\ DFT\% + \frac{t}{n} &\leq DFT\% \times \left(1 + \frac{s}{k}\right) \\ \delta \times \left(DFT\% + \frac{t}{n}\right) &\leq \delta \times DFT\% \times \left(1 + \frac{s}{k}\right) \\ FC &\leq \delta \times DFT\% \times \left(1 + \frac{s}{k}\right) \end{aligned} \tag{2}$$

Note that the value of $FC_u = \delta \times DFT\% \times (1 + s/k)$ should not be greater than 1, i.e. the quotient of s/k should be limited to satisfy the following inequalities:

$$\begin{aligned} \delta \times DFT\% \times \left(1 + \frac{s}{k}\right) &\leq 1 \\ \left(1 + \frac{s}{k}\right) &\leq \frac{1}{\delta \times DFT\%} \\ \frac{s}{k} &\leq \frac{1}{\delta \times DFT\%} - 1 \end{aligned}$$

Therefore,

$$\frac{s}{k} \leq \frac{1 - \delta \times DFT\%}{\delta \times DFT\%} \tag{3}$$

If δ is set to 1, the right-hand side of this inequality can be simplified to n_2/n_1.

4 Genetic algorithm-based DFT dies deployment automation

In this Section, an automation algorithm is presented, which is based on the genetic approach and the proposed models, to help designers to deploy the DFT dies in MCMs and to obtain a near optimal fault coverage. The application of the genetic algorithm (GA) to the DFT dies deployment problem requires an encoding scheme, an evaluation function and a set of genetic operators, namely selection, crossover and mutation [9]. Fig. 2 shows a GA-based automatic DFT dies deployment algorithm. Key operations in the algorithm are explained in the following.

Automatic-DFT-dies-deployment algorithm();
Begin
initialise parameters;
initialise population;
evaluate population based on FC;
while ($\frac{|FC_u - FC|}{FC_u} > \varepsilon$ and generation $< N$)
begin
select solutions for next population;
perform crossover and mutation;
evaluate population;
end(while);
end(algorithm).

Fig.2 *An automatic DFT dies deployment algorithm for MCMs*

Encoding scheme: In order to proceed encoding in each deployment generation, position matrix (***PM***) is defined to represent the original position of each die in an MCM. Each element (m_{ij}) of the ***PM*** is defined as: (i) $m_{ij} = 0$, if the die corresponding to m_{ij} is a DFT die, and (ii) $m_{ij} = 1$, if the die corresponding to m_{ij} is an NDFT die. Taking Fig. 1*a* as an example, the corresponding PM can be obtained by listing each die according to its position as follows:

$$\boldsymbol{PM} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 \\ 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 & 0 & 0 \end{bmatrix}$$

The chromosome can be constructed by listing the elements of the PM according to its horizontal ordering.

Evaluation function: The evaluation function (f_e) is used to evaluate the fitness value (fault coverage) of a deployment generation in the GA, which is from eqn. 1, and is rewritten as follows:

$$f_e = \delta \times \left(DFT\% + \frac{t}{n}\right)$$

Selection: The selection operator selects the fittest chromosomes for survival into the next generation. Chromosomes with higher fitness values ($|f_e|$) are chosen for the next generation.

Crossover: Order crossover (OX) [9] is used to build offspring by choosing a subsequence from one parent and preserving the relative sequence from the other parent.

Mutation: The mutation is done by randomly altering one symbol from 1 to 0 and another symbol from 0 to 1 in the chromosomes.

Table 1 shows a DFT dies deployment example based on the GA, which has a population of four chromosomes with 36 genes each, i.e. there are 36 dies in an MCM. The $DFT\%$ is 0.5 and s/k is assumed not greater than 0.75. This algorithm will terminate when the fault coverage deviation $(|FC_u - FC|)/FC_u$ is within ε (= 10%) or the generation is greater than N (= 200). In this example, $FC_u = 0.875$ for $\delta = 1$. Population 1 represents the initial population with four chromosomes which are generated randomly. Note that the first chromosome of population 1 represents the PT-MCM design shown in Fig. 1*a*. The algorithm terminates when the fault coverage derivation (= 5.1%), which is based on the first chromosome of the final population, is

within ε (= 10%). Note that the first chromosome of the final population represents the PT-MCM design shown in Fig. 1*b*.

Table 1: DFT dies deployment example based on the GA

	Fitness value
Population 1: (initial population)	
Chromosome	
0100000111101100110010000011111110100	0.56
0100000110101101110010000011101110101	0.61
0100010110101101110000000110101110101	0.67
0010111011001011100010001101101100 10	0.64
Population 2: (after crossover and selection)	
Chromosome	
1011101011100 | 10011001000011 | 001101010	0.69
1101100100010 | 10011001000011 | 110101101	0.67
0100010110101 | 10111000000110 | 101110101	0.67
0010111011001 | 01110001000110 | 110110010	0.64
Population 3: (after mutation and selection)	
Chromosome	
1011101011100100110001000110011010 10	0.75
1101100100010100110010000111101011 01	0.67
0100010110101101111000000101011101 01	0.69
0010111011001011100010001101101100 10	0.64
Final population: (within ε)	
Chromosome	
1001100110011001100110011001100110011001	0.83
1010011010100101000100111011001100 11	0.78
1011010101010010101100100011011100 10	0.81
0101011010101010100101010101011010 10	0.83

5 Defect level estimation models

The testing of complex VLSI circuits to ensure acceptable defect levels in products shipped to customers has become very challenging [12]. One way of minimising the number of faulty chips that escape the test procedures is to extensively test those circuits that have a high probability of being faulty [12]. This requires a model for predicting the defect level of chips. This Section presents two defect level estimation models for MCMs under equiprobable and non-equiprobable faults, respectively.

Williams and Brown [13] have derived a well known formula for computing the defect level of an integrated circuit as a function of yield and fault coverage. The following shows the Williams formula:

$$DL = 1 - Y^{(1-FC)} \tag{4}$$

where Y and FC represent the yield and fault coverage of an integrated circuit, respectively. In this model, fault coverage is evaluated by a fault model for which equiprobable faults are assumed. The Williams formula can be extended to MCMs if it is assumed that the dies in an MCM are equally likely to have a fault and are independent with no manufacturing defects induced. Hence, the defect level of an MCM can be expressed by the following formula [6]:

$$DL_{MCM} = 1 - Y_{MCM}^{(1-FC)} \tag{5}$$

Note that eqn. 5 is applicable for general MCMs. This result is also applicable to PT-MCMs with the same fault assumptions of eqn. 5. Substituting eqn. 1 into eqn. 5, the defect level for PT-MCMs is as follows:

$$DL_{PT-MCM} = 1 - Y_{PT-MCM}^{(1-\delta(DFT\%+t/n))} \tag{6}$$

Both eqns. 5 and 6 are based on the equiprobable fault assumption of MCMs. However, much work has been dedicated to the defect level analysis for non-equiprobable faults in digital ICs [11, 14, 15]. In the following, this concept is extended to MCMs by considering non-equiprobable faults.

First assume that the conditions for dies in an MCM to have a fault depends on their respective area and defect density and are independent with no manufacturing defects induced. Without loss of generality, then assume that there are n dies in an MCM and each die i with area A_i, defect density D_i, and yield Y_i, and there are m faulty dies in the MCM. Based on these assumptions, the results in [11] can directly be applied to the MCM defect level estimation. The result can be written as follows:

$$DL = 1 - Y^{(1-\Omega)} \tag{7}$$

where Ω is a generalised weighted fault coverage figured for non-equiprobable faults. The weighted fault coverage is given as

$$\Omega = \frac{\ln \prod_{j=1}^{m} Y_j}{\ln \prod_{i=1}^{n} Y_i} \tag{8}$$

For equiprobable faults, Ω reduces to FC and eqn. 7 is the same as the Williams formula in eqn. 4. To apply this result to MCMs, Y_i is interpreted as the yield of die i. For a definition of the original meaning of Y_i refer to [11]. Two different yield models to predict die yields are considered. The first model used to predict die yields is the Poisson yield model [16]. In this model, the die yield is modelled as

$$Y = e^{-AD} \tag{9}$$

where A and D represent the die area and defect density, respectively. The Poisson model assumes that defects are uniformly and randomly distributed, a model which tends to predict low yields for large die sizes [16]. The second yield model which is usually employed to account for clustered defects is termed as the negative binomial model [16]

$$Y = \left(1 + \frac{AD}{\alpha}\right)^{-\alpha} \tag{10}$$

where α is the clustering parameter. The elegance of the negative binomial model is that, through a statistical analysis of defect distribution data, a more accurate yield can be obtained. By applying these two yield models, two defect levels for MCMs under non-equiprobable faults are derived. Eqn. 11 shows the defect level for MCMs with random defects assumption of dies:

$$DL_{RMCM} = 1 - Y_{RMCM}^{(1-\Omega)} \tag{11}$$

where

$$\Omega = \frac{\ln \prod_{j=1}^{m} Y_j}{\ln \prod_{i=1}^{n} Y_i} = \frac{\ln \prod_{j=1}^{m} e^{-A_j D_j}}{\ln \prod_{i=1}^{n} e^{-A_i D_i}} = \frac{\sum_{j=1}^{m} A_j D_j}{\sum_{i=1}^{n} A_i D_i} \tag{12}$$

and Y_{RMCM} represents the yield of an MCM with random defects. The defect level for MCMs with clustered defects

of dies is expressed as:

$$DL_{CMCM} = 1 - Y_{CMCM}^{\left(1 - \frac{\ln \prod_{j=1}^{n} (1 + A_j D_j / \alpha_j)^{-\alpha_j}}{\ln \prod_{i=1}^{n} (1 + A_i D_i / \alpha_i)^{-\alpha_i}}\right)} \quad (13)$$

where Y_{CMCM} represents the yield of an MCM with clustered defects and α_i is the clustering parameter of the ith die in an MCM. Since the yield of an MCM with clustered defects can be expressed by the product of each die yield, which is based on the negative binomial model in an MCM, as shown in eqn. 14,

$$Y_{CMCM} = \prod_{i=1}^{n} Y_i = \prod_{i=1}^{n} \left(1 + \frac{A_i D_i}{\alpha_i}\right)^{-\alpha_i} \quad (14)$$

eqn. 13 can be reduced as follows:

$$DL_{CMCM} = 1 - \prod_{i=m+1}^{n} \left(1 + \frac{A_i D_i}{\alpha_i}\right)^{-\alpha_i} \quad (15)$$

Although the authors only consider two typical yield models, Poisson and negative binomial, the defect level models used by the authors under non-equiprobable faults are equally applicable to general MCMs and PT-MCMs by using other yield models.

6 Experiments

In order to validate their fault coverage estimation model, the authors have compared their approach with a pragmatic approach. Experimental results for the fault coverage, upper bound of fault coverage and defect level of PT-MCMs based on the proposed approach are also illustrated in this Section.

6.1 Comparison with other approach

A pragmatic test and diagnosis methodology for derivation of fault coverage for PT-MCMs, which was proposed by Lubaszewski *et al.* [5], is used to evaluate the fault coverage estimation model used in this paper. A sample MCM which contains 50 dies is the circuit to be tested. The ACM/SIGDA combinational benchmarks [10] are used as the construction dies for the sample MCM. Part of the benchmark circuits are duplicated several times to match the number of dies in the MCM. The parameter δ and *DFT*% are set to 1 and 0.6, respectively. The size and the number of logic clusters are varied to represent different distributions of DFT dies. Random faults are generated and the number of faulty dies is 10. For each distribution of DFT dies, random fault patterns are generated 100 times. The average value is taken as the final fault coverage of Lubaszewski's method for each distribution. Table 2 shows that the fault coverage estimation results are very close (5% deviation) to the actual fault coverages based on Lubaszewski's method.

6.2 Analysis

Fig. 3 shows the fault coverage of MCMs as a function of *DFT*% and the number of logic clusters (LCs). It is assumed that there are 60 dies in an MCM and the parameter δ is set to 1. First consider the relationship between the distribution of DFT dies and the fault coverage. When the fraction of DFT dies is fixed, an increase in the number of logic clusters results in an increase in the fault coverage. For example, if *DFT*% is 0.7 and the number of LCs is 6, 12 and 18, the fault coverage will be 0.8, 0.9 and 1.0, respectively. This is because an increase in the number of logic clusters will shrink the average size of logic clusters and reduce the number of undetectable dies. Fig. 3 also shows that *DFT*% is in proportion to fault coverage. This is because the size and number of logic clusters will both decrease by increasing the fraction of DFT dies. Fig. 4 shows the upper bound of fault coverage as a function of *DFT*% and the quotient of *s*/*k*. This Figure shows that the upper bound of fault coverage increases as the quotient of *s*/*k* increases. This is because a small value of *k* implies a small size of logic clusters, and a large value of *s* implies a small number of logic clusters. Obviously, the upper bound of fault coverage is in proportion to the *DFT*%, and an increase in the *DFT*% will result in an increase in the upper bound of fault coverage.

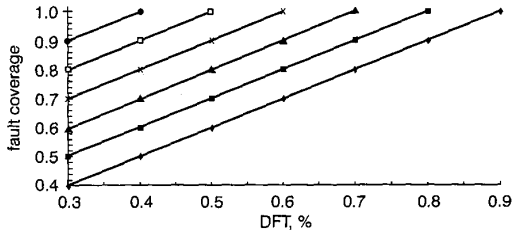

Fig. 3 *Fault coverage as a function of the fraction and distribution of DFT dies*
number of LCs = 6
number of LCs = 12
number of LCs = 18
number of LCs = 24
number of LCs = 30
number of LCs = 36
number of LCs = 42

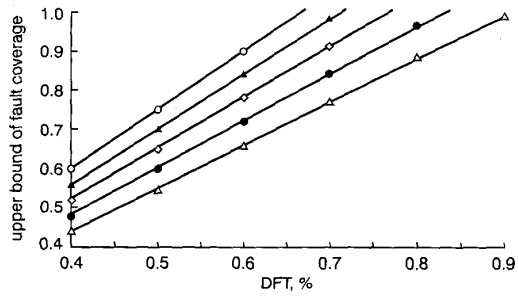

Fig. 4 *The upper bound of fault coverage as a function of DFT% and s/k*
s/*k* = 0.10
s/*k* = 0.20
s/*k* = 0.30
s/*k* = 0.40
s/*k* = 0.50

Table 2: Fault coverage based on our estimation model and Lubaszewski's method

	Number of logic clusters	Size of each cluster	*FC* of proposed model, %	*FC* of Lubaszewski's method, %
Distribution 1	1	20	62	59.13
Distribution 2	2	10, 10	64	61.80
Distribution 3	4	1, 3, 6, 10	68	64.92
Distribution 4	8	1, 1, 1, 2, 2, 3, 4, 6	76	74.62
Distribution 5	20	$\|C_i\| = 1$, $i = 1, 2, ..., 20$	100	98.81

The same data from Table 2 is used to illustrate the defect levels of PT-MCMs based on eqn. 6. Fig. 5 shows the defect levels of PT-MCMs, which is a function of fault coverage and number of LCs for $\delta = 1$, $DFT\% = 0.6$ and $n = 50$. It is evident that the defect level decreases as the manufacturing yield or the number of LCs increases for a fixed $DFT\%$. For example, if the manufacturing yield of the MCM is fixed at 0.6 and the number of LCs increases from 1 to 20, the defect level will decrease from 0.18 to 0. Therefore, given fixed values of MCM manufacturing yield and $DFT\%$, the MCM test quality (defect level) is highiy dependent upon the fault coverage (number of LCs).

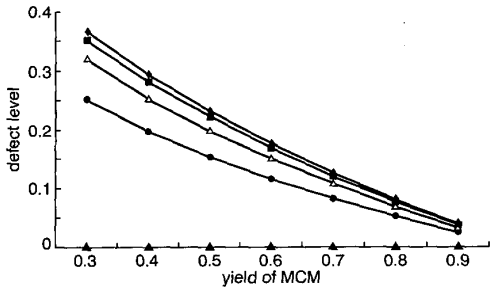

Fig. 5 *Defect level as a function of manufacturing yield and number of LCs for $\delta = 1$, $DFT\% = 0.6$ and $n = 50$*
—◆— number of LCs = 1
—■— number of LCs = 2
—△— number of LCs = 4
—●— number of LCs = 8
—▲— number of LCs = 20

7 Conclusions

The authors have presented efficient mathematical models to predict fault coverage and defect level of PT-MCMs, respectively. The fault coverage model can facilitate designers to deploy the DFT dies in MCMs in an easy and efficient way. By comparing the authors' model with the Lubaszewski's pragmatic test and diagnosis methodology, it has shown that this model can efficiently predict the fault coverage of a PT-MCM with less than 5% deviation. An automatic DFT dies deployment algorithm based on the GA and the authors' models is also developed to automate the deployment process. Two defect level estimation models, which are based on equiprobable and non-equiprobable fault distributions of MCMs, respectively, have also been presented. Both fault coverage and defect level at MCM level are two very important parameters in determining test quality of MCMs, and they are rarely discussed in the literature. The estimation models developed by the authors for these two parameters in MCMs can help to make up for such shortcomings.

8 References

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