which is based on the Karhunen-Loeve orthogonal expansion theorem [6]. Assuming that all paths are Rayleigh faded, we can write $\mathbf{C}_l$ as

$$\mathbf{C}_l = \sum_{k=0}^{N-1} G_{lk}\mathbf{B}_{lk} \quad (4)$$

where $\{\mathbf{B}_{lk}\}_{k=0}^{N-1}$ are the normalised eigenvectors of the covariance matrix $\mathbf{F}_l = E[\mathbf{C}_l\mathbf{C}_l^{*T}]$, and the vectors $\{\mathbf{G}_l\}_{l=0}^{L-1}$ where $\mathbf{G}_l = (G_{l0}, G_{l1}, ..., G_{l,N-1})^T$ are composed of independent complex zero-mean Gaussian coefficients with variances equal to the eigenvalues $\{\Gamma_{lk}\}_{k=0}^{N-1}$ of $\mathbf{F}_l$. When the RAKE receiver has an exact knowledge of the channel, the (m, n)th entry of $\mathbf{F}_l$ is given by

$$F_{lmn} = \phi_l(p_m - p_n)\sqrt{E_m E_n} \quad (5)$$

where $\phi_l(\cdot)$ is the autocorrelation function of the lth path, and p_k and E_k denote the time position and transmitted energy associated with the kth symbol, respectively. As can be observed from eqn. 5, the RAKE receiver must have knowledge of the channel (such as DPS, B_D and MIP) together with that of E_k so that it can construct $\mathbf{F}_l$ to obtain the vectors $\{\mathbf{B}_{lk}\}_{l=0,k=0}^{L-1,N-1}$. Since none of these parameters are known precisely by the receiver, we adopt an approximation of $\mathbf{F}_l$ in the form given by eqn. 5 and therefore an approximation of the vectors $\{\mathbf{B}_{lk}\}_{l=0,k=0}^{L-1,N-1}$.

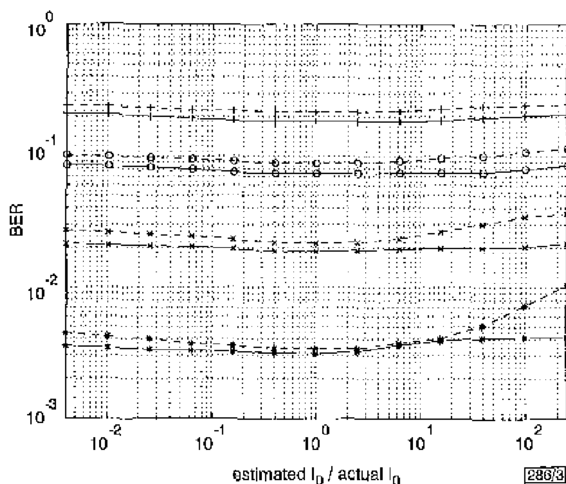

Fig. 3 *Raw BER against estimated I_0/actual I_0*

- - 120km/h
· ····· – 150km/h
+ –4dB
○ 0dB
× 4dB
✳ 8dB

To estimate the MAP channel, we use the MAP criterion to obtain an estimate of $\{\mathbf{G}_l\}_{l=0}^{L-1}$ by maximising the *a posteriori* conditional PDF $p(\{\mathbf{G}_l\}_{l=0}^{L-1}|\{\mathbf{R}_l\}_{l=0}^{L-1})$ with respect to $\{\mathbf{G}_l\}_{l=0}^{L-1}$. Directly solving this optimisation problem is intractable. However, a solution can be obtained easily using the iterative EM algorithm [3]. Following the proof outlined in [1], we can write the mth component of the re-estimate $\mathbf{G}_l^{(d+1)}$ at the dth iteration as

$$G_{lm}^{(d+1)} = \frac{1}{1 + I_0/\Gamma_{lm}} \sum_{k=0}^{N-1} R_{lk} \times \left(\sum_{A \in S_k} AP\left(A_k = A|\{\mathbf{R}_l\}_{l=0}^{L-1}, \{\mathbf{G}_l^{(d)}\}_{l=0}^{L-1}\right)\right)^* B_{lmk}^* \quad (6)$$

where B_{lmk} is the kth component of the vector $\mathbf{B}_{lm}$ and S_k is the alphabet set taken by A_k. As can be seen in eqn. 6, we also need to know I_0 to compute $\mathbf{G}_l^{(d+1)}$.

The iterative semi-blind MAP CEA is carried out a fixed number of times D. The channel estimate obtained at the last iteration is used for maximal ratio combining that provides the soft outputs $\Lambda_k^{(D)}$ [1, 2]. Assuming uncoded binary phase shift keying (BPSK), symbol decoding is performed by hard decision on the real part of $\Lambda_k^{(D)}$.

To properly execute the EM algorithm steps, the RAKE receiver should possess available estimates of the Doppler spread B_D, the noise variance I_0, the average powers $\phi_l(0)$ of all considered paths and the transmitted symbol energies E_k.

Simulation results and conclusions: We restrict our treatment to a UMTS/FDD uplink low-rate data service in the vehicular environment [4] where the pilot symbols are spread, and all the symbols are transmitted with equal energy $E_k = E, \forall k$. The channel model is ITU vehicular A [5] and the number of RAKE fingers is chosen as three. For our evaluation, we considered two vehicular speed values v = 120km/h, 500km/h, four E/I_0 values –4, 0, 4 and 8dB, and a carrier frequency f_0 = 192GHz. The simulations were carried out with D = 5 iterations. We assumed that the shape of the DPS was known by the receiver but that the average powers of the paths were unknown. The receiver therefore adopted a uniform MIP where all path powers were taken to be equal, i.e. $\phi_l(0) = 1/L, \forall l$.

Figs. 1–3 display the sensitivity of the CEA with respect to an estimated energy in B_D, E and I_0, respectively. For v = 120km/h, the curves are almost flat, indicating that for low to moderate Doppler spreading, the MAP CEA is robust to parameter estimation errors. For v = 500km/h, the effects of erroneous parameters are visible in the high E/I_0 region, whereas the low E/I_0 region exhibits greater robustness. Of the three parameters concerned, the MAP CEA is most sensitive to B_D. Nevertheless, the sensitivity with respect to this parameter is visible only in the high Doppler case, being more pronounced in the high E/I_0 region.

In conclusion, the results show that the semi-blind MAP CEA is relatively robust to errors in estimating B_D, E, I_0, and can be used even in channels with severe Doppler spreading.

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Power PHEMT with compact device layout for low voltage CDMA application

E.Y. Chang, Di-Houng Lee, S.H. Chen and H.C. Chang

A high efficiency low voltage operation dual delta-doped AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistor (PHEMT) for low voltage code division multiple access (CDMA) application has been developed. When tested at 2.4V and 1.9GHz under IS-95 CDMA modulation, the 20.16mm PHEMT device was found to have a linear output power of 28dBm with a power added efficiency of 30.2%. The device also has a saturation power of 30.0dBm with a power added efficiency of 61.5%. The high efficiency and linearity of the PHEMT at low bias voltage is attributed to the use of the dual delta-doped PHEMT structure and to the reduction of the size of the device layout. The device is suitable for low voltage CDMA applications.

Introduction: Advanced high performance wireless communication systems such as digital cellular phone and satellite communication systems require high efficiency power transistors operating at a low supply voltage to increase the talk time of the handsets. Devices for low voltage applications have been developed in recent years [1 – 5]. In this Letter, a dual delta-doped AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistor (PHEMT) is presented which can be used in low voltage code division multiple access (CDMA) applications. The developed PHEMT also has a very compact device layout. The reduction in the device layout results in a low knee voltage and low source resistance for the device which makes it suitable for low voltage applications. The developed device has been evaluated for IS-95 CDMA applications at 3.0 and 2.4V. This Letter represents the first report of a power PHEMT for 2.4V CDMA applications.

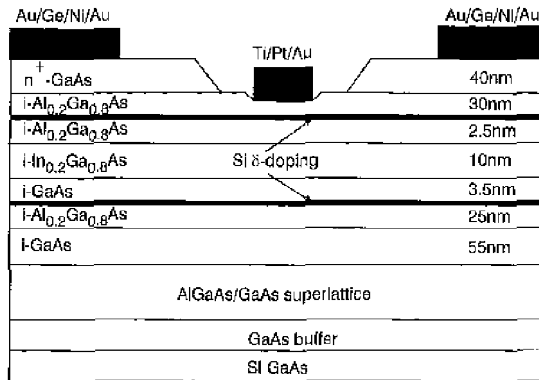

Fig. 1 *Structure of δ-doped AlGaAs/InGaAs/GaAs power PHEMT*

Device structure and layout: The device used in this Letter is an AlGaAs/InGaAs/GaAs based PHEMT. The epitaxial layer was grown by a molecular beam epitaxy (MBE) technique on a 3in (100) oriented semi-insulating GaAs wafer. The structure of the dual delta-doped AlGaAs/InGaAs/GaAs PHEMT is shown in Fig. 1. The capping layer was doped to $5 \times 10^{17}/cm^3$ to form good ohmic contacts. The two dimensional electron gas (2-DEG) was formed in the pseudomorphic InGaAs channel (100Å) by electron transfer from silicon delta doping above and below the InGaAs layer. The GaAs spacer was grown between AlGaAs and InGaAs to improve the interface quality. The fabricated device had a total gate width of 20.16mm with each finger 120μm in length. The drain to source spacing was 4μm and the gate length 0.5μm. The device had an area $1640 \times 300 \mu m^2$, which is quite compact compared with regular power device layouts.

Device fabrication: The device was processed using a standard power PHEMT process. Device isolation was accomplished by wet etching using an HF-based solution. The ohmic metal, Au/Ge/Ni, was deposited by electron-beam evaporation followed by rapid thermal annealing at 300°C for 10s. The double gate recess was performed to increase the device breakdown and reduce the device source resistance using a dilute citric acid based solution. The gate length of the device was 0.5μm, defined by deep UV lithography. The gate metal was formed by the electron-beam evaporation of Ti/Pt/Au metal. Plasma enhanced chemical vapour deposition (PECVD) silicon nitride was used for the device passivation. Gold plated airbridges were used for interconnections. The plated gold thickness was ~2.5μm. After the frontside was completed, the device was thinned to 5mil and metallised with plated gold on the backside to improve the thermal dissipation of the device.

Device performance: The developed device has a saturation current of 6A. The pinch-off voltage of the device is around –1.1V. The contact resistance R_c of the device with 120μm gate width is 106mΩ. The maximum transconductance of this device is 340 mS/mm. The gate-to-drain breakdown voltage defined at a gate-to-drain current density of 1mA/mm is 12V. The high current density and transconductance of this device are due to the dual delta-doped PHEMT structure.

The power performance of this 0.5 μm × 20.16mm device was measured at 1.9GHz with drain biases of 3.0 and 2.4V. Fig. 2 shows the output power and power added efficiency against input power for the 20.16mm wide device at 3.0V drain bias. The testing conditions were as follows: V_{gs} = –0.91V, V_{ds} = 3.0V, idle current = 300mA. At 32.77dBm output power, the device has an efficiency of 63.04%, and the gain at this point is 7.12dB. Fig. 3 shows the power performance of the 20.16mm device when tested at 2.4V. The device was operated under class AB conditions with a bias drain current of 400mA. For the 20.16mm device, under 2.4V bias conditions, the maximum output power is 30dBm and the power added efficiency of this device at the maximum output power is 61.5%. The gain of this device at the maximum output power is 8.47dB. The linear gain was 11.56dB and the output power at 1dB compression was 28.12dBm with a power added efficiency of 47.5%.

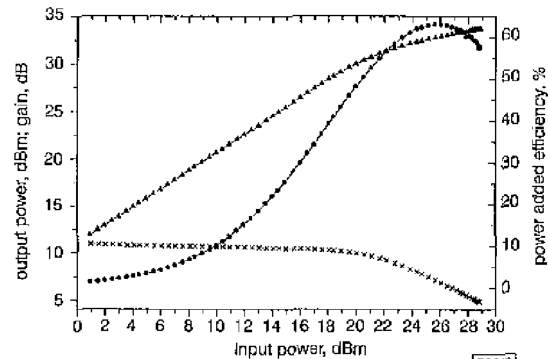

Fig. 2 *Power performance of 20.16mm device at 1.9GHz frequency under 3.0V drain-source bias voltage and 300mA idle drain current*

—▲– output power
—●— power added efficiency
· × · gain
Gate voltage = –0.91V

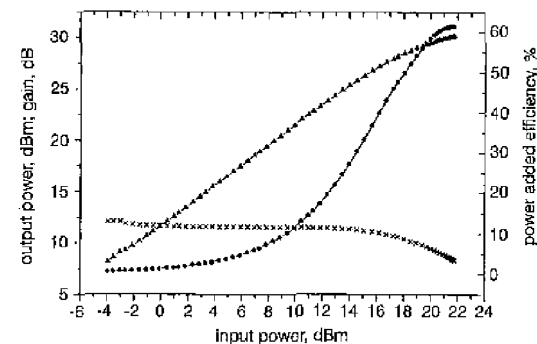

Fig. 3 *Power performance of 20.16mm device at 1.9GHz frequency under 2.4V drain-source bias voltage and 400mA idle drain current*

—▲– output power
—●— power added efficiency
×— gain
Gate voltage = –0.86V

The device was also tested at 1.9GHz under IS-95 CDMA modulation. At 3.0V bias, the testing condition for the CDMA modulation was as follows: V_{gs} = –0.91V, V_{ds} = 3.0V, idle current = 300mA. At 28.02dBm output power, the device gain is 9.81dB, the power added efficiency is 37.8%, and the device has an adjacent channel power rejection (ACPR) of –30.70dBc at 1.25MHz offset and –48.67dBc at 2.25MHz offset, as shown in Fig. 4. The device was also tested at 2.4V under IS-95 CDMA modulation. The test parameters were as follows: V_{gs} = –0.74V, V_{ds} = 2.4V, idle current = 800mA. At 28dBm output power, the device gain is 11.05dB, and the device has a power added efficiency of 30.2%. Fig. 5 shows the ACPR spectrum for the device under 2.4 V drain bias testing conditions. At 28dBm linear output power, the device has an ACPR of –31.46dBc at 1.25MHz offset and –48.83dBc at

2.25MHz offset. The developed device meets the IS-95 CDMA device specifications under both 3.0V and 2.4V bias conditions.

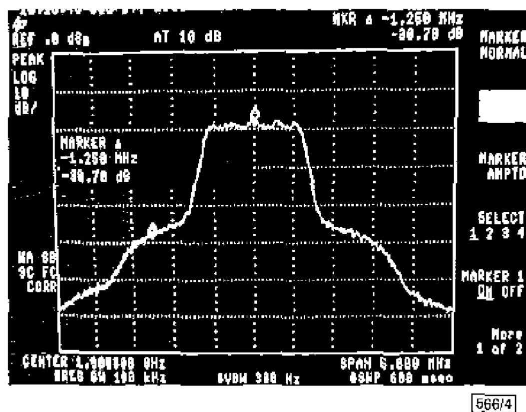

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Fig. 4 *CDMA spectrum of 20.16mm device at 3.0V drain bias voltage*

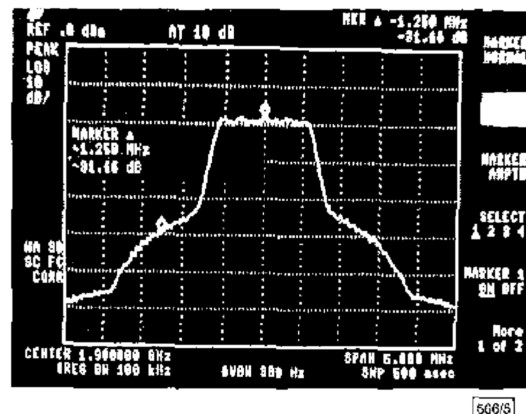

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Fig. 5 *CDMA spectrum of 20.16mm device at 2.4V drain bias voltage*

Conclusions: A low voltage power PHEMT for CDMA applications has been developed. The device has a double delta-doped AlGaAs/InGaAs/GaAs structure to provide high drain current density and transconductance. The size of the layout of the device was reduced to improve the low the voltage performance. At 2.4V bias, the developed device shows an output power of 30dBm with a power added efficiency of 61.5% and the gain of the device at maximum output power is 8.47dB. When tested under IS-95 CDMA modulation conditions, the device meets the CDMA specifications at both 3.0V and 2.4V drain bias. At 28dBm linear output power for CDMA application, the device has a power added efficiency of 37.8% at 3.0V bias and 30.2% at 2.4V bias. This Letter represents the first report on power PHEMTs for 2.4V CDMA applications. The device should be applicable to the next generation of digital wireless communication systems.

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Reduction of epitaxial alignment in n^+-p poly-Si emitter diode due to gettering of P and As by Ar implantation

Lurng Shehng Lee and Chung Len Lee

It is demonstrated that Ar implantation can retard the epitaxial realignment of poly-Si/Si in an As- or P-doped n^+-p poly-emitter diode during BF_2 implantation. This is believed to be due to the gettering of As, P, and F by bubble-like defects created by the Ar implantation used to reduce the pile-up of these dopants at the poly-Si/Si interface. Consequently, there is less break-up of the interface oxide, resulting in a reduction in epitaxial realignment.

Introduction: The use of a highly-doped poly-Si film as the diffusion source to form a shallow emitter has been widely adopted for fabricating high performance bipolar transistors [1, 2]. However, the high emitter drive-in thermal budget induces epitaxial realignment of the polysilicon [3]. In particular, the incorporated-F in the polysilicon, which is present due to the BF_2 ion implantation, enhances oxide break-up, causing more epitaxial realignment of the polysilicon [4, 5]. This epitaxial realignment results in an extended single crystal emitter, degrading the current gain of the transistor [6].

It was proposed and demonstrated that Ar implantation could be used to suppress the boron penetration in p^+ PMOSFETs [7]. It is expected that this technique can be applied to the double-diffused n^+/p poly-Si emitter diode to suppress the epitaxial realignment. In this Letter, it is demonstrated that this technique enables the achievement of this goal.

Experiment: In this experiment, the n^+-p poly-Si diodes were fabricated on p-type 15 25Ωcm (100) Si wafers. First, all wafers were dipped in an $HF:H_2O$ (1:10) solution to remove the native surface oxide. A poly-Si film of 3000Å was then deposited at 620°C, followed by an Ar implantation dose of $10^{16}cm^{-2}$ at 80keV. The projected range of the Ar was ~900Å. An As or P dose of $2 \times 10^{16}cm^{-2}$ was then implanted in the wafers at 80keV. BF_2 implantation with a dose of $4 \times 10^{15}cm^{-2}$ at 60keV was then carried out to simulate an emitter transistor structure with an extrinsic base. After all implantations, a 90Å oxide layer was grown on the wafers to prevent impurity out-diffusion, and then the wafers were annealed in a furnace in N_2 ambient at 900°C for 60min. All the wafers then received an additional rapid thermal annealing (RTA) at 1100°C for 20s in N_2 ambient. For comparison, similar devices without Ar implantation were also fabricated.

Results and discussion: Fig. 1*a* and *b* show the TEM cross-sectional micrographs of the junction region of the poly-Si emitter