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Cascoded LVTSCR with tunable holding voltage for ESD protection in bulk CMOS technology without latchup danger ☆

Ming-Dou Ker [a,*], Hun-Hsien Chang [b]

[a] *Integrated Circuits and Systems Laboratory, Institute of Electronics, National Chiao-Tung University, 1001 Ta-Hsueh Road, Hsinchu, Taiwan 300*

[b] *Design Service Division, Taiwan Semiconductor Manufacturing Company (TSMC), Science-Based Industrial Park, Hsinchu, Taiwan*

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Abstract

The lateral SCR devices used in CMOS on-chip ESD protection circuits are reviewed. Such SCR devices had been found to be accidentally triggered by noise pulses when the ICs are operated in the application systems. A cascoded design is therefore proposed to safely apply the LVTSCR devices for whole-chip ESD protection in CMOS ICs without causing unexpected operation errors or latchup danger. The temperature dependence on the holding voltage of the cascoded LVTSCRs has been investigated in detail. From the experimental verification, the cascoded LVTSCRs can be fully turned on within a time below 20 ns. The ESD robustness per layout area of the three-cascoded LVTSCRs can be 0.83 V/μm^2 in a 0.35-μm silicide CMOS process without using the extra silicide-blocking and ESD-implant masks, whereas the ESD robustness of the gate-grounded NMOS is only 0.25 V/μm^2. Such cascoded LVTSCRs with a tunable holding voltage greater than VDD can provide CMOS ICs with effective component-level ESD protection but without causing catchup danger if it is accidentally triggered by the system-level overshooting or undershooting noise pulses.

1. Introduction

Due to the low holding voltage (~1 V) of the lateral SCR device, the power dissipation (Power $\cong I_{ESD} \times V$hold) of the SCR device during the electrostatic discharge (ESD) stress is less than that of other ESD protection devices (such as the field-oxide device, thin-oxide NMOS, or diode in the breakdown condition) in deep-submicron CMOS technologies. Thus, the lateral SCR device can sustain very high ESD stress as compared to other ESD protection devices. For example, the holding voltage of an SCR device in a 0.35-μm bulk CMOS process is about 1 V, but the snapback holding voltage of an NMOS device in the same process is about 6 V. The SCR device can sustain about 6-times larger ESD current per unit layout area than the NMOS does. Because the SCR device can sustain much higher ESD stress within a smaller layout area, the lateral SCR devices had been used as the main discharging devices in the on-chip ESD protection circuits to protect CMOS ICs against ESD damage [1–20].

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* Corresponding author: Integrated Circuits and Systems Laboratory, Institute of Electronics, National Chiao-Tung University, 1001 Ta-Hsueh Road, Hsinchu, Taiwan 300. Tel.: +886-3-571-2121; fax: +886-3-571-5412.

E-mail address: mdker@ieee.org (M.-D. Ker).

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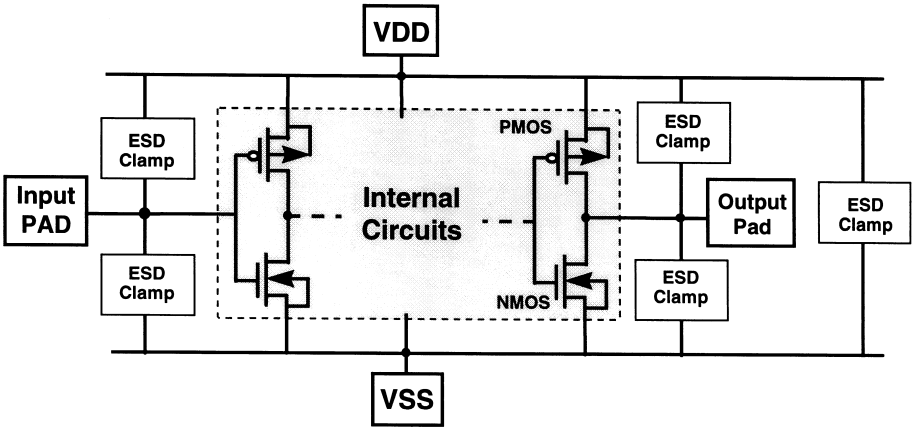


Fig. 1. The schematic circuit diagram to show the location of ESD clamp circuits in a CMOS IC to achieve whole-chip ESD protection.

To provide effective ESD protection for a whole CMOS IC, the on-chip ESD protection circuits are added around the input, output, and power pads of a CMOS IC. Because some ESD damage had been found on the internal circuits beyond the input or output ESD protection circuits [21–24], the ESD clamp circuit has to be also placed between the VDD and VSS power lines to provide the real whole-chip ESD protection [25–29]. The location of ESD clamp circuits in a CMOS IC to achieve whole-chip ESD protection is illustrated in Fig. 1. Therefore, the lateral SCR devices had been used in input/output ESD protection circuits [1–16], [18–20] and even in the VDD-to-VSS ESD clamp circuits [17,29] to protect CMOS ICs against ESD damage.

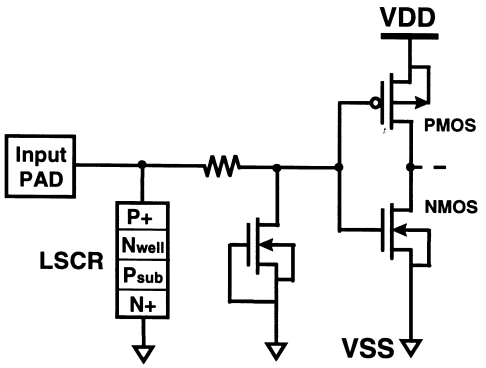
In this paper, the lateral SCR devices used in CMOS on-chip ESD protection circuits are reviewed. The latchup danger of using SCR devices in CMOS on-chip ESD protection circuits is first discussed. Such SCR devices had been found to be accidentally triggered by the noise pulses when the ICs are in the normal operating conditions. To overcome this problem, a cascode configuration with tunable holding voltage has been proposed to safely apply the SCR devices for effective ESD protection in bulk CMOS ICs. The device characteristics including the temperature effect of the cascoded LVTSCRs in a 0.35-μm silicide bulk CMOS process has been experimentally investigated in details with turn-on verification.

2. Brief overview on SCR devices used in CMOS on-chip ESD protection circuits

2.1. The lateral SCR (LSCR)

The lateral SCR (LSCR) device had been used as an effective ESD protection element for input pins in submicron CMOS ICs [1–3]. The typical application example of the LSCR device in an input ESD protection circuit is shown in Fig. 2(a). The device structure of the LSCR is illustrated in Fig. 2(b) and the I–V characteristics of the LSCR is illustrated in Fig. 2(c). The LSCR has a high trigger voltage (30–50 V), which is determined by the breakdown voltage of the N-well. The trigger voltage of the LSCR is generally much higher than the gate-oxide breakdown voltage of the input stages in submicron CMOS ICs. Therefore, the LSCR has to be used in conjunction with the secondary protection circuit (the series resistor and the gate-grounded NMOS in Fig. 2(a)) to perform the overall ESD protection function to protect the input stages.

The secondary protection circuit has to sustain the ESD stress before the LSCR is triggered to bypass ESD current on the input pad. Because of the slow turn-on speed to trigger LSCR, the secondary protection circuit was found to be damaged by the ESD energy [3]. So, the secondary protection circuit was designed with a considerably larger device dimension and a large series resistor to protect themselves. This secondary protection circuit with large device dimensions often occupies more layout area. If the secondary protection circuit was not properly designed, it caused a failure window in the ESD test scanning from the low voltage to the high voltage. Such an input ESD protection circuit was found to pass the ESD stress with a low voltage level or a high voltage level, but it failed when the ESD stress was with a middle voltage level [3]. So, the design and layout of the secondary protection circuit with the LSCR for the overall input ESD protection circuit is somewhat critical in CMOS ICs.



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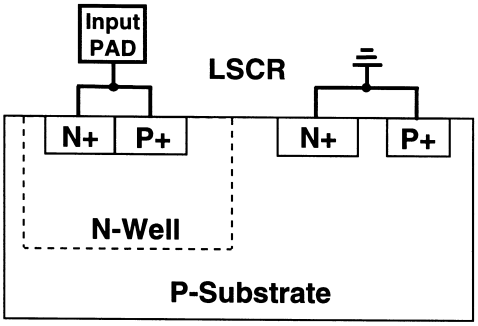

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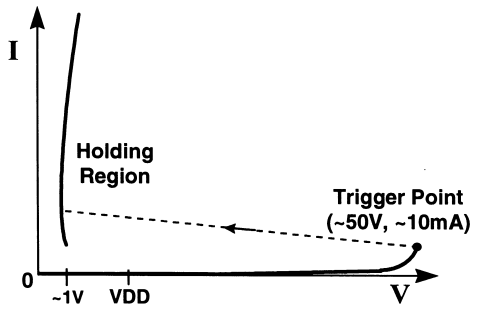
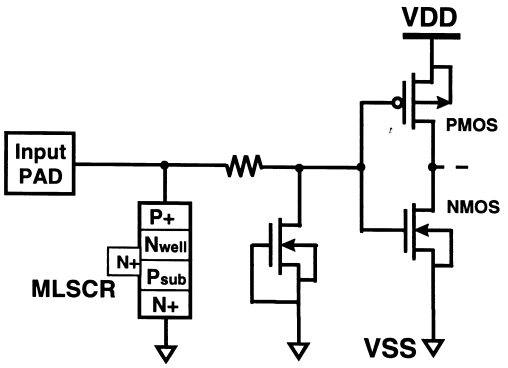


(c)

Fig. 2. (a) The input ESD protection circuit with the LSCR device. (b) The device structure of the LSCR in CMOS process. (c) The *I–V* characteristics of the LSCR in a 1.2-μm CMOS process [2].



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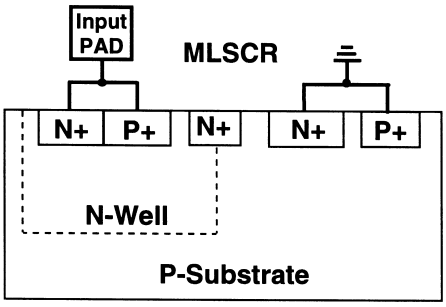

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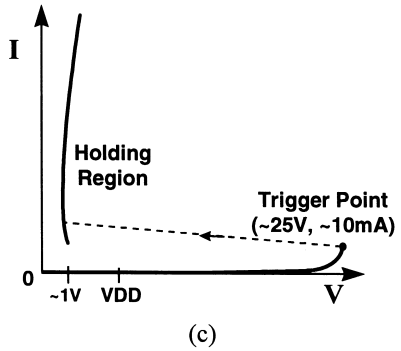


(c)

Fig. 3. (a) The input ESD protection circuit with the MLSCR device. (b) The device structure of the MLSCR in CMOS process. (c) The *I–V* characteristics of the MLSCR in a 1.2-μm CMOS process [4].

2.2. The modified lateral SCR (MLSCR)

To provide more effective ESD protection for the input stages, the modified lateral SCR (MLSCR) was invented to reduce the trigger voltage of the lateral SCR [4]. With a lower trigger voltage in the MLSCR, the secondary protection circuit could have smaller device dimensions to save total layout area. The example of using the MLSCR device in the input ESD protection circuit is shown in Fig. 3(a). The device structure of the MLSCR is illustrated in Fig. 3(b) and the *I–V* characteristics of the MLSCR is illustrated in Fig. 3(c). The MLSCR is made by adding an N+ diffusion across the well-substrate junction to lower the trigger voltage of the SCR device. Because the N+ dif-

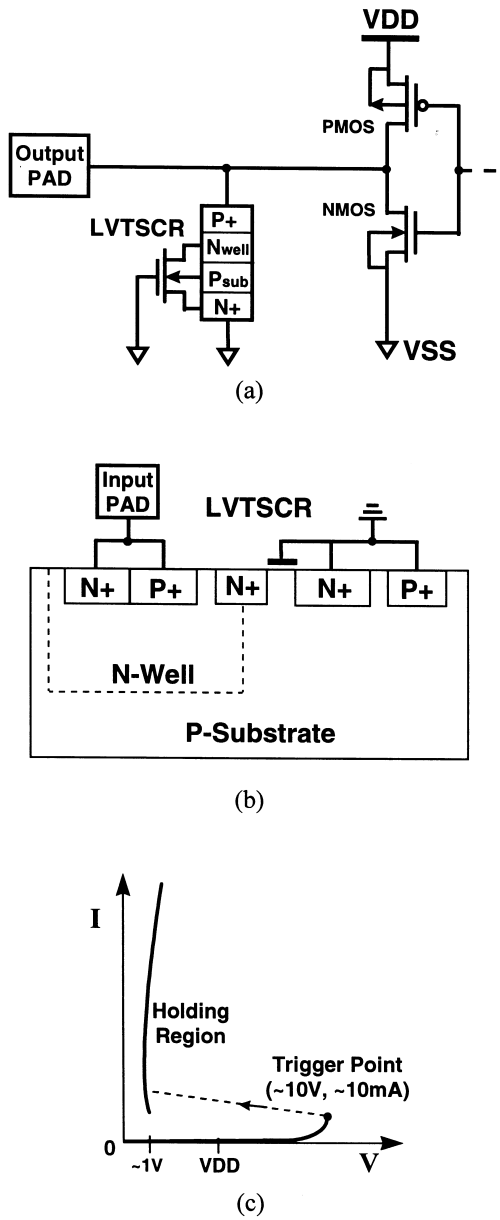


Fig. 4. (a) The input ESD protection circuit with the LVTSCR device. (b) The device structure of the LVTSCR in CMOS process. (c) The *I–V* characteristics of the LVTSCR in a 0.6-μm CMOS process [16].

fusion has a much higher doping concentration than the N-well, the trigger voltage of the MLSCR can be significantly lower than that of the LSCR in the same CMOS process. The trigger voltage of the MLSCR is determined by the breakdown voltage of the N+ diffusion, which is dependent on process technology. The LSCR was reported to have a trigger voltage of about ~25 V [4], which is still greater than the gate-oxide breakdown voltage of the input stages in submicron CMOS ICs. Thus, the MLSCR has to still be co-operated with the secondary protection circuit to perform the overall ESD protection function for the input stages. Unsuitable design or layout on the secondary protection circuit still causes the ESD damage located on the secondary protection circuit rather than the MLSCR device [4].

To lower the trigger voltage of the SCR device, the transient-triggering effect on the SCR device had been studied and used to design the on-chip ESD protection circuit with multiple SCR structures [5–9].

2.3. The low-voltage triggering SCR (LVTSCR)

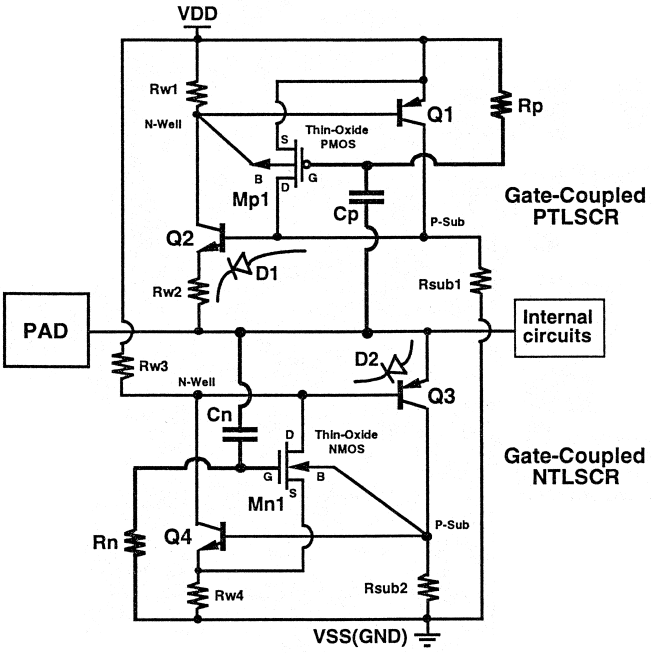
To effectively protect the input stages and even the output buffers in submicron CMOS ICs, the low-voltage triggering SCR (LVTSCR) device had been invented with a much lower trigger voltage [10–16]. The example of using the LVTSCR device as the output ESD protection circuit is shown in Fig. 4(a). The device structure of the LVTSCR is drawn in Fig. 4(b) and the *I–V* characteristics of the LVTSCR is illustrated in Fig. 4(c).

The trigger voltage of the LVTSCR is equivalent to the snapback-trigger voltage of the short-channel NMOS device, which is inserted into the lateral SCR structure, rather than the original switching voltage (about 30–50 V) of the lateral SCR device. By suitable design, the trigger voltage of the LVTSCR can be lowered below the drain breakdown voltage of the output NMOS [11–16]. The typical trigger voltage (current) of the LVTSCR in a 0.6-μm CMOS technology is about ~10 V (~10 mA) [16]. With such a low trigger voltage, the LVTSCR can provide effective ESD protection for both the input stages and the output buffers of CMOS ICs without the support of the secondary protection circuit. Therefore, the total layout area of the ESD protection circuits with the LVTSCR can be significantly reduced.

By using another method, the hot-carrier effect in the short-channel NMOS device was also applied to reduce the trigger voltage of the SCR device. Such a hot-carrier triggered SCR was used as the ESD clamp device between the VDD and VSS power buses [17].

2.4. The gate-coupled LVTSCR

To effectively protect the thinner gate oxide in deep-submicron low-voltage CMOS ICs, the gate-coupling technique was applied to further reduce the trigger voltage of the LVTSCR [18,19]. The gate-coupled LVTSCR ESD protection circuit for the input or output pads is shown in Fig. 5(a). The device structure of the gate-coupled LVTSCR is illustrated in Fig. 5(b) and the *I–V* characteristics of the gate-coupled



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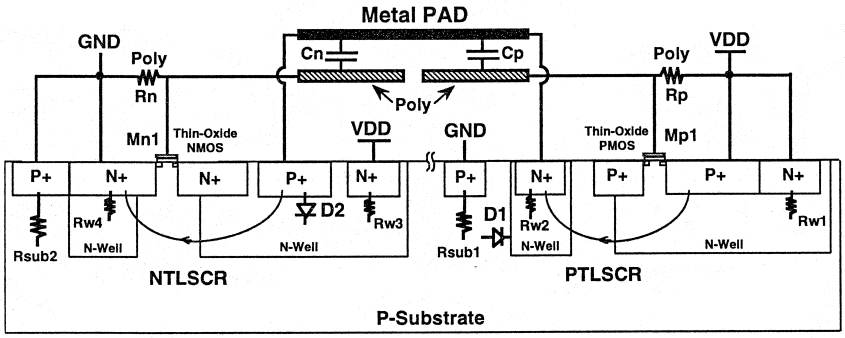

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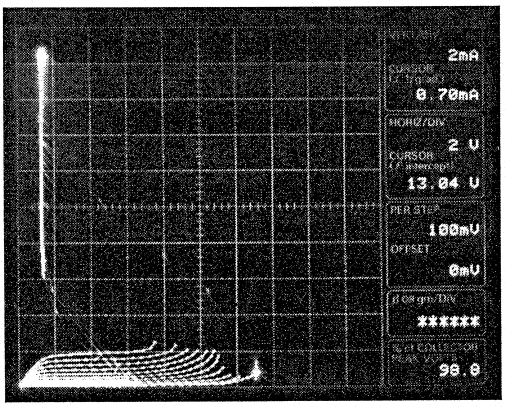
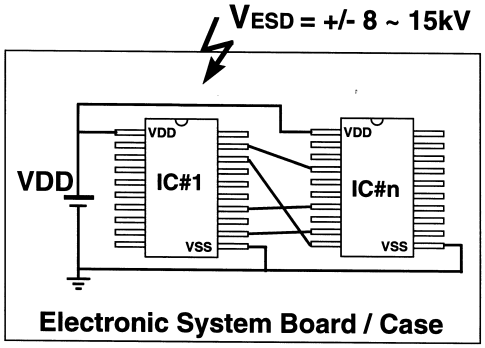


(c)

Fig. 5. (a) The ESD protection circuit with the gate-coupled LVTSCR devices. (b) The device structure of the gate-coupled LVTSCR in CMOS process. (c) The measured *I–V* characteristics of the gate-coupled LVTSCR in a 0.6-μm CMOS process [19].



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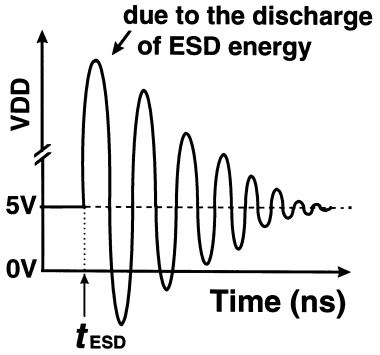


(b)

Fig. 6. (a) The schematic diagram to show the system-level electromagnetic comparability (EMC) ESD test. (b) The transient overshooting/undershooting voltage waveform on the VDD pin of the ICs during the EMC/ESD test.

LVTSCR in a 0.6-μm CMOS process is measured in Fig. 5(c) [19]. The trigger voltage of the gate-coupled LVTSCR can be significantly lowered by the coupled voltage on the gate of the short-channel NMOS in the LVTSCR device. Thus, the thinner gate oxide of the input stages in deep-submicron low-voltage CMOS ICs can be effectively protected by the gate-coupled LVTSCR.

An alternative design by using a circuit technique, rather than by using snapback breakdown, to turn on the LVTSCR device for ESD protection is also reported in [20].

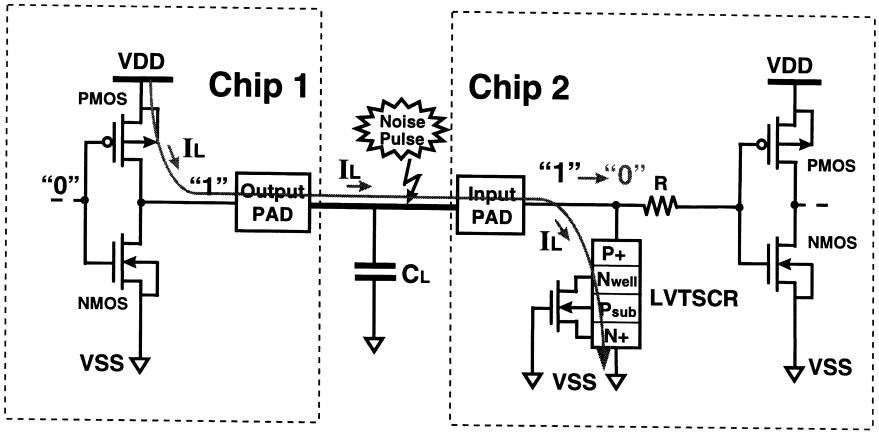
3. Issue of the LVTSCR devices in CMOS ICs

Due to the low trigger voltage (~10 V), the LVTSCR device can perform excellent on-chip ESD protection without the support of the secondary protection circuit. But, its low trigger current (~10 mA) may cause the LVTSCR to be accidentally triggered by the external noise pulses while the CMOS IC is in the normal operating condition. In order to safely apply the LVTSCR for on-chip ESD protection, the LVTSCR in CMOS ICs must have an enough noise margin to the noise glitches in the application environments.

Recently, due to the request of the "*CE*" mark from the *European Community* on the electronics products, an ESD gun with an ESD voltage of ±8–15 kV is used to test the electromagnetic compatibility (EMC) of the electronic products [30–32]. The system-level EMC/ESD test is illustrated in Fig. 6(a). Such EMC/ESD test can cause a heavily overshooting or undershooting voltage ringing on the VDD and VSS pins of the ICs in the system board, as shown in Fig. 6(b). During such a system-level EMC/ESD test, the power lines of ICs in the system board can be coupled with an overstress voltage even up to several hundred volts. Such a system-level EMC/ESD event easily causes the transient-induced latchup failure in CMOS ICs [33–35]. If the lateral SCR or the LVTSCR devices are used as the ESD clamp devices between the VDD and VSS power lines of CMOS ICs [17,29], such ESD-protection SCR devices are easily triggered by the system-level EMC/ESD transient pulses to cause a very serious latchup problem in CMOS ICs.

The LVTSCR devices in the input or output ESD protection circuits are also susceptible to such system-level noise pulses. Because the holding voltage of the LVTSCR is only ~1 V, the voltage levels of the input or output signals can be destroyed if the LVTSCR in the ESD protection circuits is accidentally turned on when the IC is operated in the harsh environments [36]. For example, in Fig. 7(a), the output buffer of Chip 1 is used to drive the input pad of Chip 2, where the input ESD protection circuit in Chip 2 is formed by the LVTSCR. While the output buffer in Chip 1 sends an output signal of logic "1" to the input pad of Chip 2, the output PMOS in Chip 1 is turned on by the pre-buffer circuit with a logic "0". Therefore, the voltage level on the input pad of Chip 2 is charged up to VDD, and the LVTSCR in Chip 2 is initially kept off. But, if there is a system-level noise pulse coupled to the interconnection line between the output pad of Chip 1 and the input pad of Chip 2, the LVTSCR in Chip 2 may be triggered by the overshooting noise pulse and the voltage level on the input pad is clamped to only ~1 V by the turned-on LVTSCR. This causes a logic transition from the state "1" to become the state "0" in the application systems. If the LVTSCR device is used in the output ESD protection circuit, as shown in Fig. 7(b), the LVTSCR could be also triggered by the noise pulse coupled to the output pad.

Because the output PMOS often has a large device dimension to drive an external heavy load, the load



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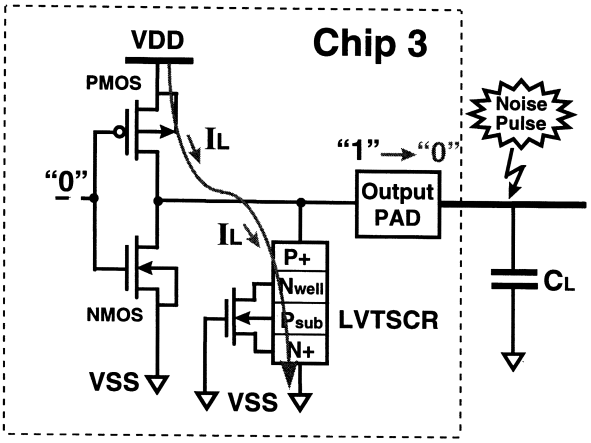

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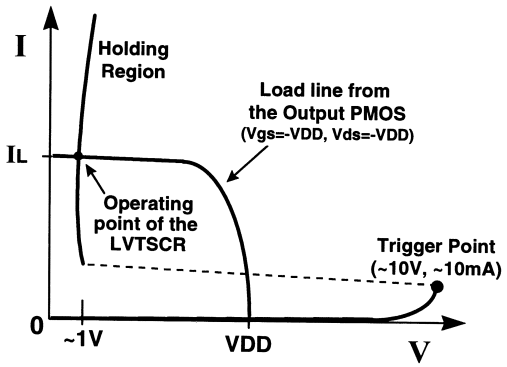


(c)

Fig. 7. The schematic diagram to show the LVTSCR in (a) an input ESD protection circuit in Chip 2, (b) an output ESD protection circuit in Chip 3, being accidentally triggered by the system-level overshooting noise pulses. (c) The intercept point between the *I–V* curves of the output PMOS and the LVTSCR decides the voltage level on the pad and the leakage current I_L from VDD to VSS.

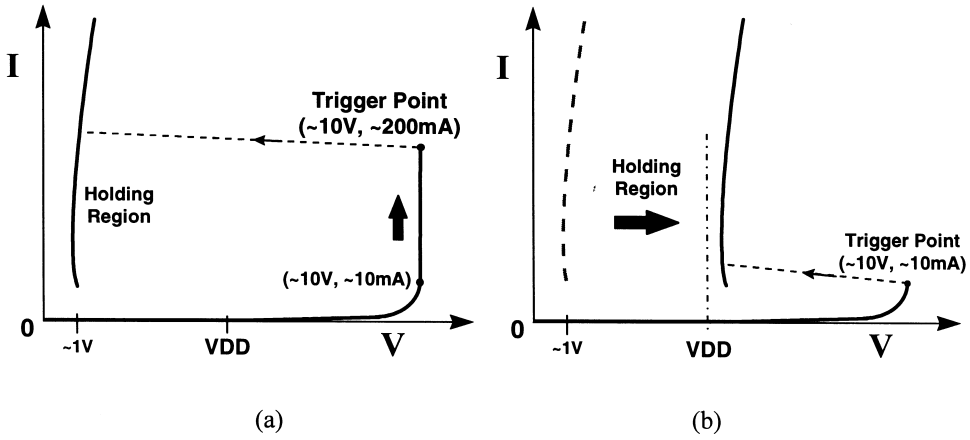


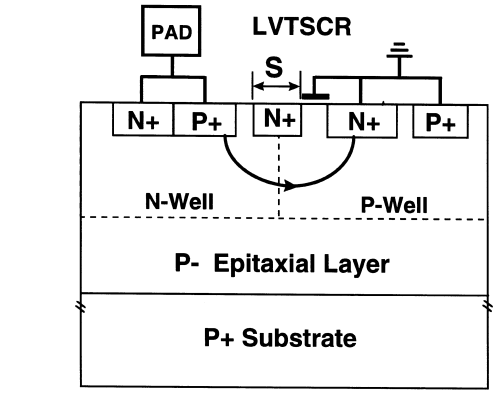
Fig. 8. Two solutions, (a) by increasing the trigger current; (b) by increasing the holding voltage, to avoid the LVTSCR being accidentally triggered by the noise pulses.

line of the output PMOS has a stable intercept point on the I–V curve of the LVTSCR. The intercept point in Fig. 7(c) is the operating point of the LVTSCR, where there is a leakage current I_L flowing from the VDD through the output PMOS and LVTSCR to the VSS. Due to the triggering of noise pulses, the turned-on LVTSCR clamps the voltage level on the input pad of Chip 2 or the output pad of Chip 3 from VDD to ~1 V. This changes the logic state from "1" to "0" on the pad and causes an operation error in the application system. Moreover, the board-level leakage current I_L (~several hundred mA, dependent on the device dimension of the output PMOS) from VDD to VSS consumes more system power. Therefore, some modifications should be designed on the conventional LVTSCR device to guarantee the safe application in CMOS ICs during any system-level reliability test.

4. Solutions to safely apply LVTSCR devices for on-chip ESD protection

There are two solutions to avoid the LVTSCR being accidentally triggered by the noise pulses when the ICs are in the normal operating condition. As shown in Fig. 8(a), the first is to only increase the trigger current of the LVTSCR, but the trigger voltage and the holding voltage are kept the same.

With a higher trigger current, the LVTSCR has enough noise margin against the overshooting or undershooting noise pulses on the pads. An HINTSCR (high-current NMOS-trigger lateral SCR) device had been successfully designed by adding a bypass diode into the LVTSCR device structure to increase its trigger current from ~10 to ~200 mA in a 0.6-μm CMOS process [37–39]. Such an HINTSCR



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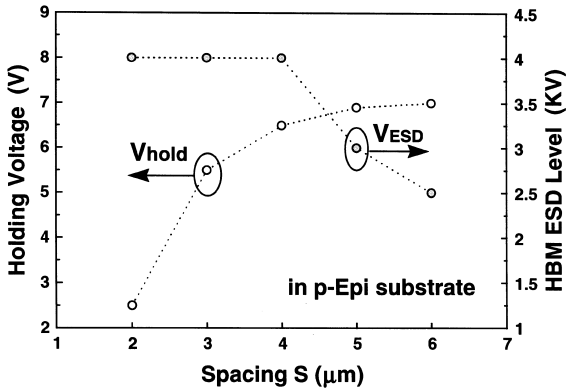
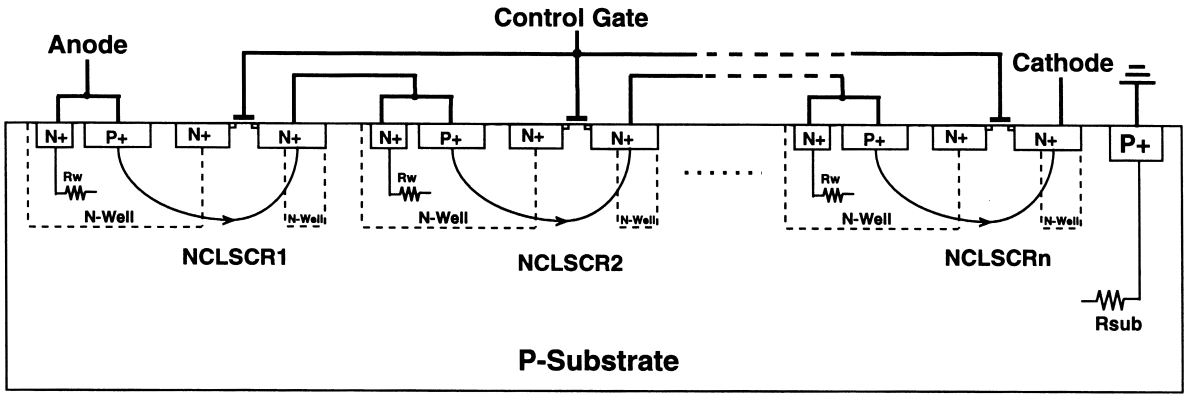


(b)

Fig. 9. (a) The device structure of the LVTSCR in a CMOS process with the p-epitaxial layer. (b) The dependence of the holding voltage and ESD level of the LVTSCR on the layout spacing S [42].



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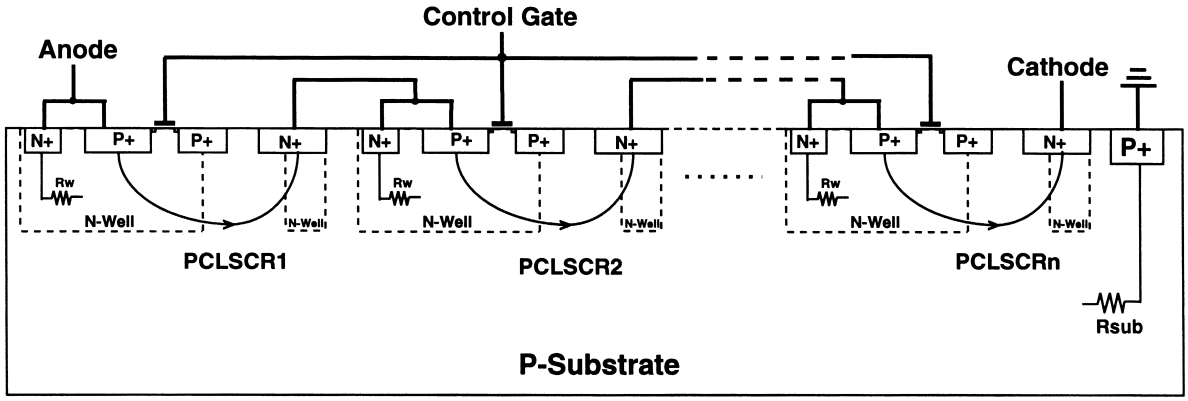


(b)

Fig. 10. The schematic cross-sectional view of (a) the cascoded NCLSCRs, and (b) the cascoded PCLSCRs in a bulk *p*-substrate CMOS process.

has a noise margin greater than VDD + 12 V, whereas a conventional LVTSCR device in the same process has a noise margin of only about VDD + 3 V. The HINTSCR still has a low holding voltage, so it can perform a good ESD robustness as that of an LVTSCR.

The second method is to increase the holding voltage of the LVTSCR greater than the voltage level of VDD in CMOS ICs, as shown in Fig. 8(b). But, the trigger voltage and current is still kept as low as that of an LVTSCR. In the CMOS process with epitaxial substrate, the holding voltage of an SCR device can be easily increased greater than VDD by extending the anode-to-cathode distance in the SCR structure or by reducing the thickness of the epitaxial layer [40,41]. Only increasing the holding voltage of an LVTSCR leads to more power dissipation (Power$\cong I_{ESD} \times V$hold) on the LVTSCR during the ESD stress. This often causes a lower ESD robustness on the LVTSCR. The dependence of layout spacing on ESD performance of an LVTSCR device with a holding voltage greater than VDD had been investigated in a CMOS process with epitaxial substrate [42]. The LVTSCR device realized in the epitaxial substrate is drawn in Fig. 9(a), where the layout spacing S of drain N+ diffusion of the inserted NMOS in the SCR structure has an effect

on the holding voltage of LVTSCR device in the epitaxial substrate. The dependence of the holding voltage and human-body-model (HBM) ESD level of the LVTSCR in the epitaxial substrate on the layout spacing S is redrawn in Fig. 9(b), where a layout spacing of 3–4 μm can increase the holding voltage but still not degrade its ESD robustness [42]. For the CMOS process with different thickness of the epitaxial layer and different doping concentration, the suitable layout spacing to increase the holding voltage should be investigated in detail with the consideration on reasonable process variations.

But, the most CMOS ICs (especially the consumer ICs) are still fabricated in the low-cost bulk CMOS processes without using the epitaxial substrate. It is difficult to increase the holding voltage of an SCR device greater than VDD in such bulk CMOS processes. Using the double guard rings to surround both the anode and the cathode of an SCR device can break the latching path and increase its holding voltage. But, the latchup guard rings often occupy much more layout area and wider layout spacing in the bulk CMOS process. Moreover, such SCR devices with double guard rings in the bulk CMOS process take a much longer time to turn themselves on, so they can not be triggered in time to bypass the fast-transient ESD current.

To overcome this issue, a novel cascoded-LVTSCR structure is designed in the next section to increase its holding voltage (> VDD) without much degrading its ESD robustness in a 0.35-μm silicide bulk CMOS process [43].

5. Characteristics of the cascoded LVTSCRs

To increase the holding voltage of the LVTSCR, a cascode configuration is proposed to achieve both high component-level ESD robustness and safe application without the latchup problem during the system-level EMC/ESD test. The cascoded LVTSCRs with different number of LVTSCR devices have been fabricated in a 0.35-μm bulk CMOS process with both silicided diffusion and LDD structure. The device characteristics, especially including the temperature effect, has been measured and investigated in more detail.

5.1. Device structure

The device structures of the proposed cascoded NCLSCRs (NMOS-Controlled Lateral SCRs) and PCLSCRs (PMOS-Controlled Lateral SCRs) in a bulk p-substrate CMOS process are shown in Fig. 10(a) and (b), respectively. In Fig. 10, the cathode of the NCLSCR1 (PCLSCR1) is connected to the anode of the NCLSCR2 (PCLSCR2), and the cathode of the

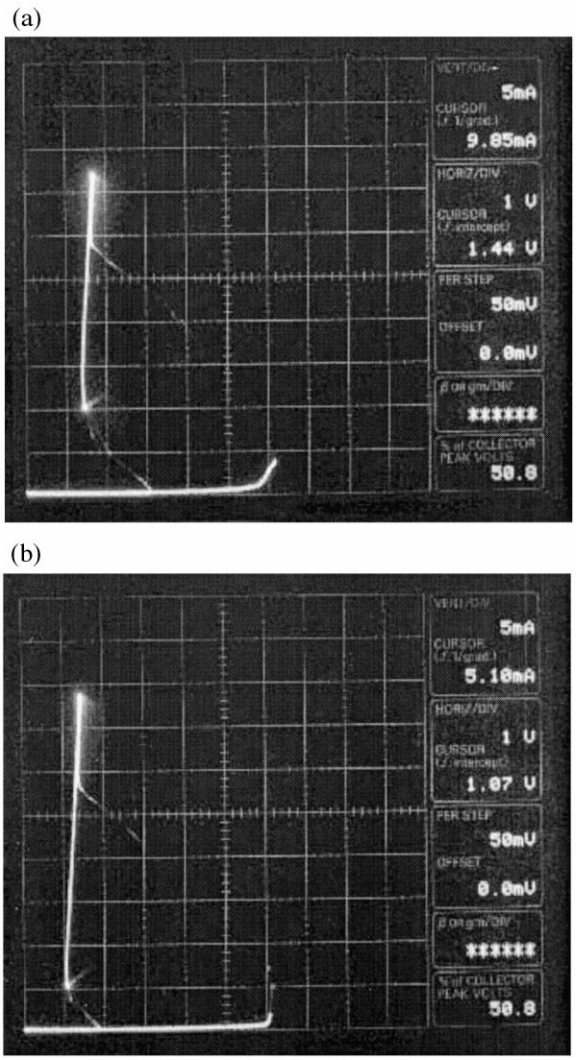


Fig. 11. The I–V curves of a single NCLSCR device in a 0.35-μm bulk CMOS process under the temperature of (a) 25°C, and (b) 150°C.

NCLSCR2 is connected to the anode of the next NCLSCR (PCLSCR) device to configure the cascoded NCLSCRs (PCLSCRs). All the gates of the NCLSCRs (PCLSCRs) are connected together and controlled by a control gate. To save more layout area, the N-well of the cathode in NCLSCR1 (PCLSCR1) can be merged with the N-well of the anode in NCLSCR2 (PCLSCR2), and so on between every two adjacent NCLSCR (PCLSCR) devices. The N+ diffusion of the cathode in NCLSCR1 (PCLSCR1) can be also merged with the N+ diffusion of the N-well bias (R_W) in the anode N-well of NCLSCR2 (PCLSCR2) to further reduce the total area of the cascoded NCLSCRs (PCLSCRs) devices.

By using the cascode configuration, the total voltage

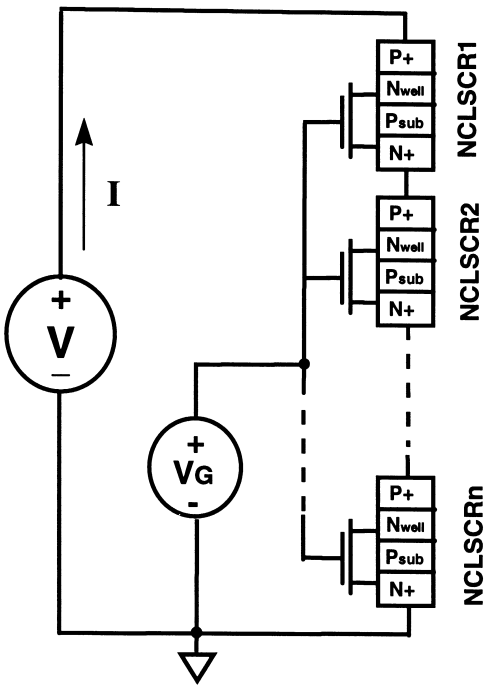


Fig. 12. The experimental setup to measure the *I–V* curves of the cascoded LVTSCRs.

drop across the cascoded NCLSCRs (PCLSCRs) is the sum of the voltage drop across every NCLSCR (PCLSCR) device. Therefore, the total holding voltage of the cascoded NCLSCRs (PCLSCRs) becomes tunable by changing the number of the NCLSCRs (PCLSCRs) in the cascode configuration. If the cascoded NCLSCRs include 3 NCLSCR devices, its total holding voltage can be greater than the 3-V VDD. Each NCLSCR device still has a holding voltage of ~1 V, but the cascoded NCLSCRs have a total holding voltage greater than VDD. So, the cascoded NCLSCRs (PCLSCRs) can be safely applied for effective ESD protection but without causing the accidental operation error or the latchup danger in CMOS ICs. To provide a quick turn-on response in such cascoded NCLSCRs (PCLSCRs) to bypass the fast-transient ESD current, a suitable control circuit has to be designed to simultaneously trigger every NCLSCR (PCLSCR) device in the cascode configuration during the ESD-stress condition. The design examples are demonstrated in section 6 with practical turn-on verification in a 0.35-μm bulk CMOS technology.

5.2. Characteristics of the cascoded NCLSCRs

The *I–V* curves of a single NCLSCR with 0-V gate bias are measured in Fig. 11(a) and (b) under the temperature of 25 and 150°C, respectively. The holding

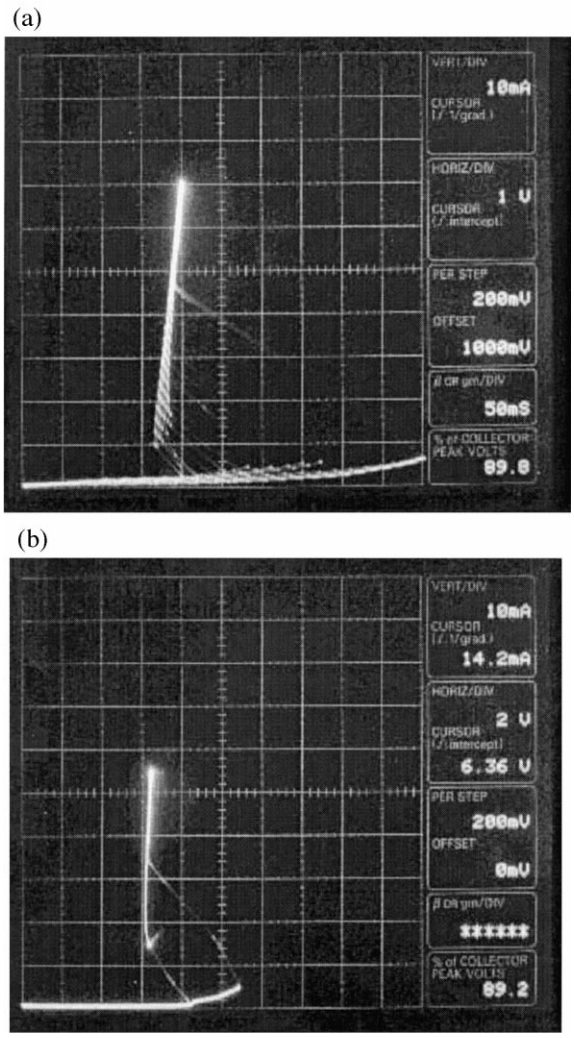


Fig. 13. The *I–V* curves of (a) the cascoded 3-NCLSCRs with different gate biases, and (b) the cascoded 5-NCLSCRs with 0-V gate bias, under the temperature of 125°C.

voltage (current) of a single NCLSCR is reduced from the 1.44 V (9.85 mA) at 25°C to only 1.07 V (5.1 mA) at 150°C, which is much lower than the VDD of CMOS ICs. Such an NCLSCR in the ESD protection circuit is easily triggered by the system-level EMC/ESD test or by the high-temperature high-voltage reliability test to cause failures or malfunctions in the application systems.

The cascoded NCLSCRs have been fabricated in a 0.35-μm bulk CMOS process. The experimental setup to measure the *I–V* characteristics of the cascoded NCLSCRs is shown in Fig. 12, where the *Tektronix* Curve Tracer 370A is used to generate the gate biases and to measure the anode *I–V* curves. The measured *I–V* characteristics of the cascoded NCLSCRs with

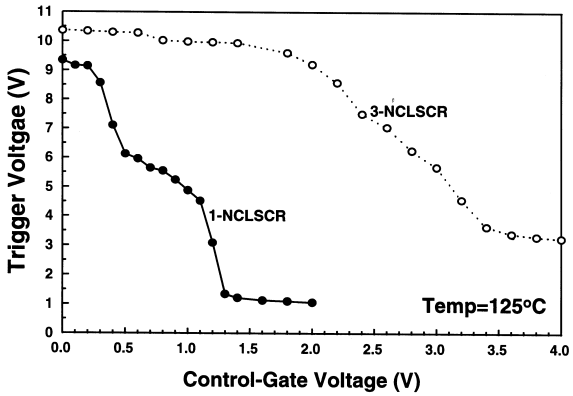


Fig. 14. Dependence of the trigger voltage of the cascoded 3-NCLSCRs and a single NCLSCR on the control-gate voltage under the temperature of 125°C.

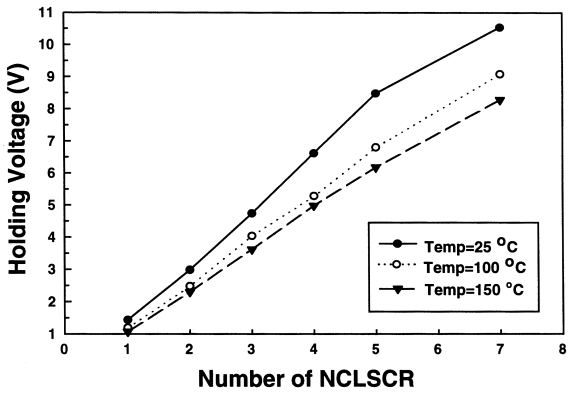


Fig. 16. Dependence of the holding voltage of the cascoded NCLSCRs on the number of the NCLSCR devices.

three and five NCLSCRs at 125°C are shown in Fig. 13(a) and (b), respectively, under different gate biases. The trigger voltage of the cascoded NCLSCRs can be significantly reduced as its gate voltage is increased. With a positive gate voltage, the cascoded NCLSCRs are easily triggered into the holding region. The dependence of the trigger voltage of the cascoded 3-NCLSCRs and a single NCLSCR on the control-gate voltage under the temperature of 125°C is shown in Fig. 14. The larger gate voltage leads to a lower trigger voltage to turn on the cascoded NCLSCRs. So, such cascoded NCLSCRs can be quickly turned on to bypass ESD current, if a suitable gate voltage is generated to bias its control gate during the ESD stress.

In Fig. 13, the holding voltage of the 3-NCLSCRs with 0-V gate bias is 3.82 V, whereas the holding voltage of the 5-NCLSCRs is 6.36 V at the temperature of 125°C. The temperature dependence of the total holding voltage in the cascoded NCLSCRs with different numbers of NCLSCR devices in the cascode configuration is shown in Fig. 15. The dependence of the holding voltage of the cascoded NCLSCRs on the number of the NCLSCR devices under different temperatures is shown in Fig. 16. The holding voltage of the cascoded NCLSCRs is almost linearly increased as the number of the cascoded NCLSCRs is increased. By adjusting the number of the cascoded NCLSCR devices, the holding voltage of the cascoded NCLSCRs becomes tunable to meet different system applications with different VDD voltage levels.

For example, to safely apply the cascoded NCLSCRs for ESD protection in 3-V CMOS ICs without causing latchup danger, three cascoded NCLSCRs have to be used. This provides a practical and useful solution to safely apply the LVTSCR for effective ESD protection, especially in the bulk CMOS process.

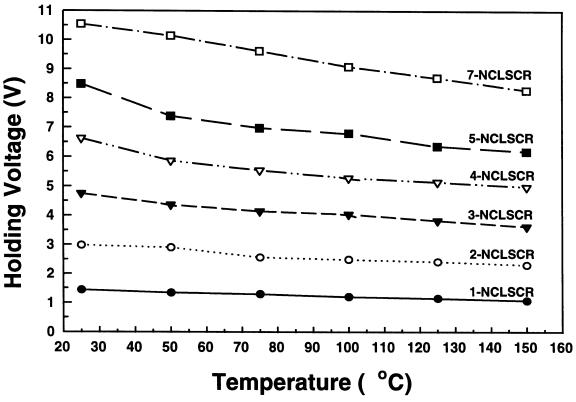


Fig. 15. The temperature dependence of the total holding voltage in the cascoded NCLSCRs with different number of NCLSCR devices.

5.3. Characteristics of the cascoded PCLSCRs

A similar experimental setup but with negative voltage biases is also used to measure the *I–V* characteristics of the cascoded PCLSCRs devices. The *I–V* curves of the cascoded PCLSCRs with two and five PCLSCRs at 150°C are shown in Fig. 17(a) and (b), respectively, under 0-V gate bias. The holding voltage (current) of the 2-PCLSCRs is −2.4 V (−14.1 mA), whereas the holding voltage (current) of the 5-PCLSCRs is −6.7 V (−53.6 mA) at 150°C. The temperature dependence of the holding voltage of the cascoded PCLSCRs with different number of PCLSCR devices in the cascode configuration is shown in Fig. 18. The dependence of the holding voltage of the cascoded PCLSCRs on the number of PCLSCR devices under different temperatures is shown in Fig. 19. The holding voltage of the cascoded PCLSCRs is almost

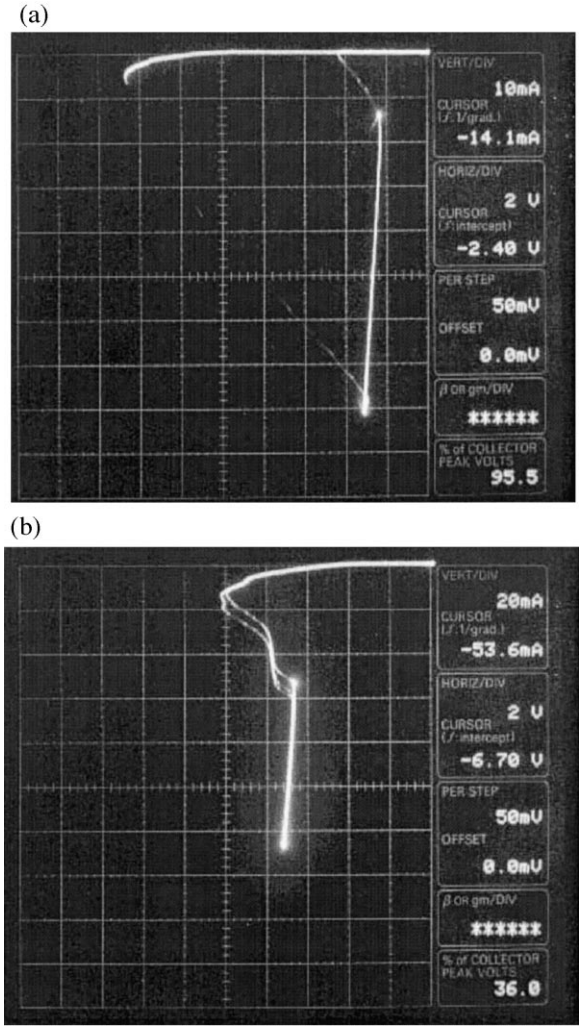


Fig. 17. The I–V curves of the cascoded PCLSCRs with (a) two PCLSCR devices, (b) five PCLSCR devices, under the temperature of 150°C.

linearly increased as the number of the cascoded PCLSCRs is increased. By adjusting the number of the cascoded PCLSCR devices, the total holding voltage of the cascoded PCLSCRs becomes tunable to meet different system applications. For example, to safely apply the cascoded PCLSCRs for ESD protection in the 3-V CMOS ICs without causing latchup danger, three PCLSCRs have to be used in the cascoded PCLSCRs.

5.4. Turn-on resistance

The slope ($\Delta V/\Delta I$) of the measured I–V curves of the cascoded NCLSCRs and PCLSCRs devices can be defined as the turn-on resistance of the cascoded LVTSCRs in their holding regions. The turn-on resistance in the holding region changes slightly while the operating point is moving along the I–V curves in the holding region. For comparison, the slope ($\Delta V/\Delta I$) between the operating currents of 20 and 200 mA in the holding region is used to define the turn-on resistance of the cascoded LVTSCRs. The relations between the turn-on resistance and the number of cascoded LVTSCRs at room temperature are shown in Fig. 20, where every NCLSCR (or PCLSCR) device in the cascoded LVTSCRs has the same device width of 30 μm only. The larger device width leads to a lower turn-on resistance in the cascoded LVTSCRs. In Fig. 20 with the device width of 30 μm, the cascoded 3-NCLSCRs have a turn-on resistance of 9.8 Ω, but the cascoded 3-PCLSCRs have a turn-on resistance of 12.7 Ω. More NCLSCRs or PCLSCRs used in the cascode configuration cause a corresponding higher turn-on resistance in the cascoded LVTSCRs. To further reduce the turn-

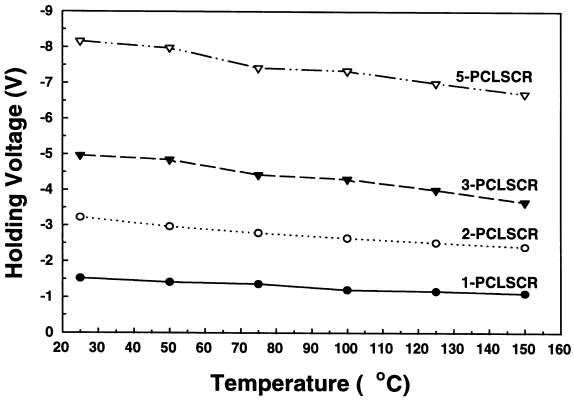


Fig. 18. The temperature dependence of the total holding voltage of the cascoded PCLSCRs with different number of PCLSCRs devices.

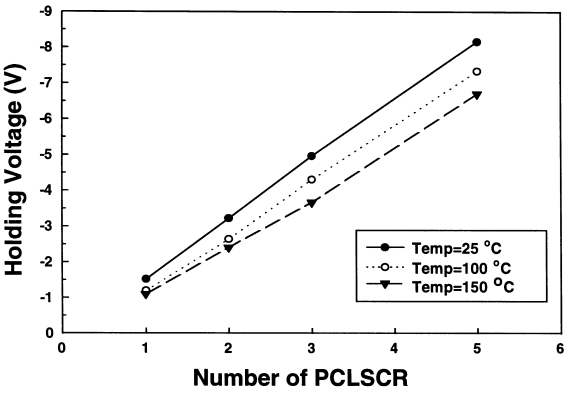


Fig. 19. Dependence of the holding voltage of the cascoded PCLSCRs on the number of PCLSCR devices.

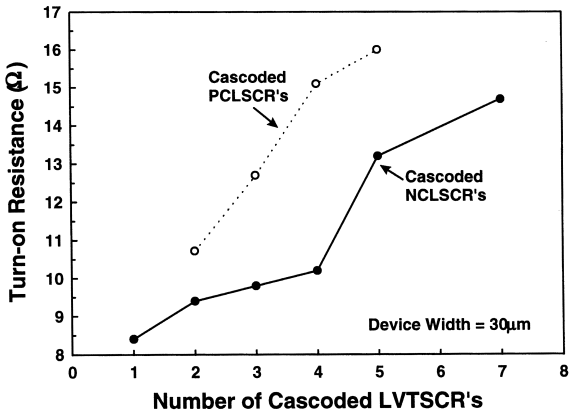


Fig. 20. The relations between the turn-on resistance and the number of cascoded LVTSCRs.

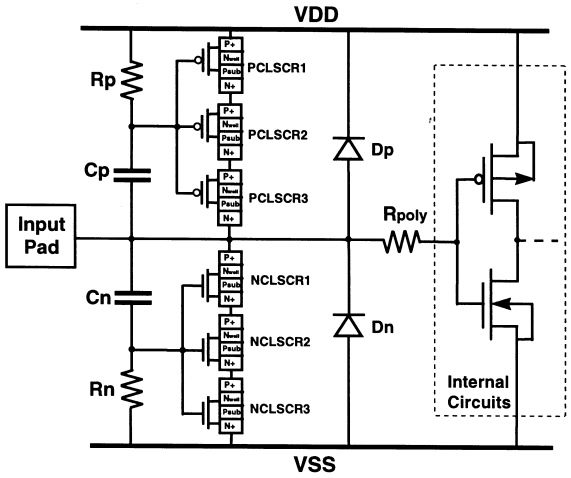
on resistance, the cascoded LVTSCRs have to be designed with wider device widths.

6. Safe applications for whole-chip ESD protection

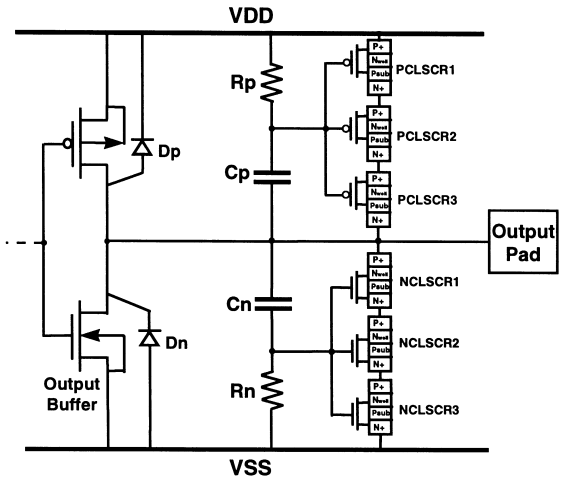
6.1. ESD protection circuits

From the detailed investigation on the device characteristics including the temperature effect, the cascoded LVTSCRs with three NCLSCRs (PCLSCRs) in a 0.35-μm bulk CMOS process have a holding voltage of 4.74 V (−4.96 V) at 25°C and 3.62 V (−3.66) at 150°C. To safely apply the LVTSCRs for ESD protection in 3-V CMOS ICs, three NCLSCRs or PCLSCRs in the cascode configuration are enough. The typical input and output ESD protection circuits using both the cascoded 3-NCLSCRs and cascoded 3-PCLSCRs with the gate-coupled technique [18,19] for 3-V CMOS ICs are shown in Fig. 21(a) and (b), respectively. The gate-coupled technique is used to generate the biased voltage on the control gate of the cascoded NCLSCRs (PCLSCRs), therefore the cascoded NCLSCRs (PCLSCRs) can be quickly turned on to provide effective ESD protection. With a holding voltage greater than VDD, such cascoded NCLSCRs and PCLSCRs in the input/output ESD protection circuits can help to clamp the overshooting or undershooting noise pulses on the input/output pads, but do not cause the latchup danger to destroy the normal input/output signals.

Such cascoded NCLSCRs (or PCLSCRs) can be also applied in the VDD-to-VSS ESD clamp circuits to avoid the ESD failure located in the internal circuits. To simultaneously turn on every NCLSCR device in the cascoded NCLSCRs structure, an ESD-detection circuit should be designed to bias the control gate, which is shown in Fig. 22. A modified design on the



(a)



(b)

Fig. 21. (a) The input ESD protection circuit, and (b) the output ESD protection circuit, using both the cascoded 3-NCLSCRs and the cascoded 3-PCLSCRs with the gate-coupled technique.

VDD-to-VSS ESD clamp circuit with the mixed LVTSCRs in the cascode configuration is shown in Fig. 23. The typical VDD-to-VSS ESD clamp circuits using the cascoded 3-NCLSCRs or cascoded 3-PCLSCRs with the *RC*-based control circuit [25–28] are shown in Fig. 24(a) and (b), respectively. The *RC* time constant in the *RC*-based control circuit is designed around 0.1–1 μs to perform the correct ESD-detection function [28] to trigger the cascoded NCLSCRs (PCLSCRs) during the ESD-stress con-

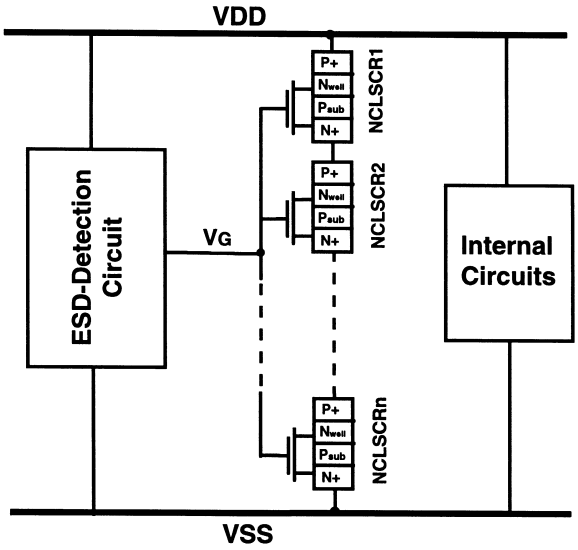


Fig. 22. The VDD-to-VSS ESD clamp circuit with the cascoded NCLSCRs controlled by an ESD-detection circuit.

dition. The number of the cascoded NCLSCRs or PCLSCRs in the ESD clamp circuit is dependent on the voltage level of VDD in the CMOS IC. For the 5-V CMOS ICs, 5-NCLSCRs (5-PCLSCRs) have to be used in the VDD-to-VSS ESD clamp circuit to effectively clamp the ESD voltage across the VDD and VSS power lines but without causing the VDD-to-VSS latchup problem.

By applying such cascoded NCLSCRs (PCLSCRs) in both the input/output ESD protection circuits and the VDD-to-VSS ESD clamp circuits, a whole-chip ESD protection scheme can be constructed to well protect the CMOS ICs in deep-submicron CMOS technologies. In the whole-chip ESD protection scheme, the ESD current paths (indicated by the dashed lines) during the Input-to-VSS ESD stress are illustrated in Fig. 25(a), whereas the ESD current paths during the pin-to-pin ESD stress are illustrated in Fig. 25(b). With the efficient VDD-to-VSS ESD clamp circuit, the ESD current is discharged through the cascoded NCLSCRs (PCLSCRs) in both the input/output ESD protection circuits and the VDD-to-VSS ESD clamp circuits. Thus, the internal circuits including the input stages and output buffers can be fully protected against ESD damage.

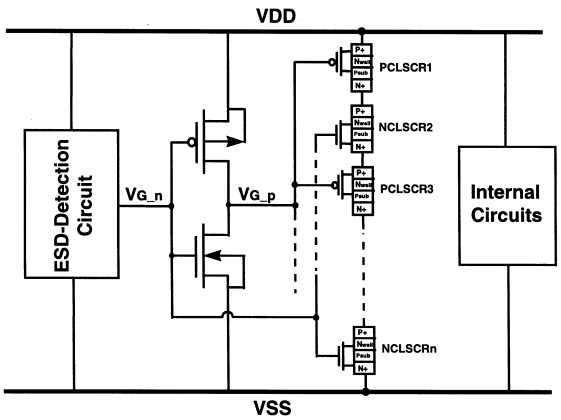
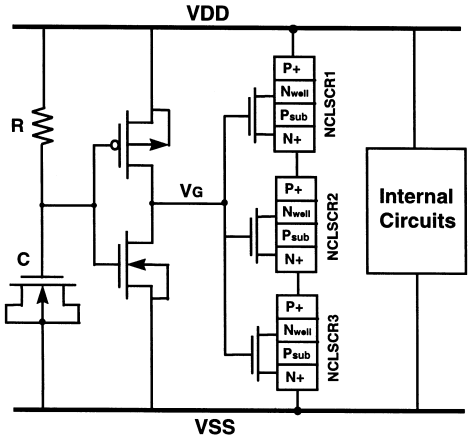
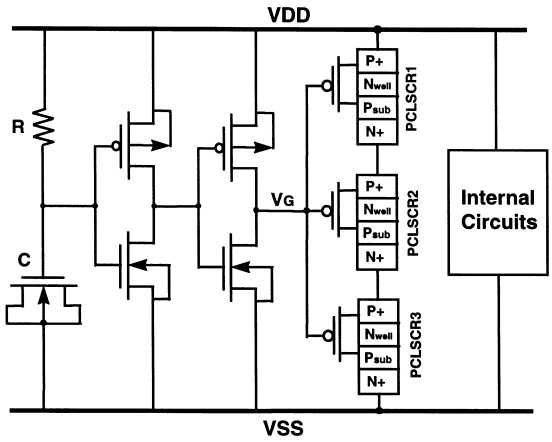


Fig. 23. The modified VDD-to-VSS ESD clamp circuit with the mixed LVTSCRs controlled by an ESD-detection circuit.

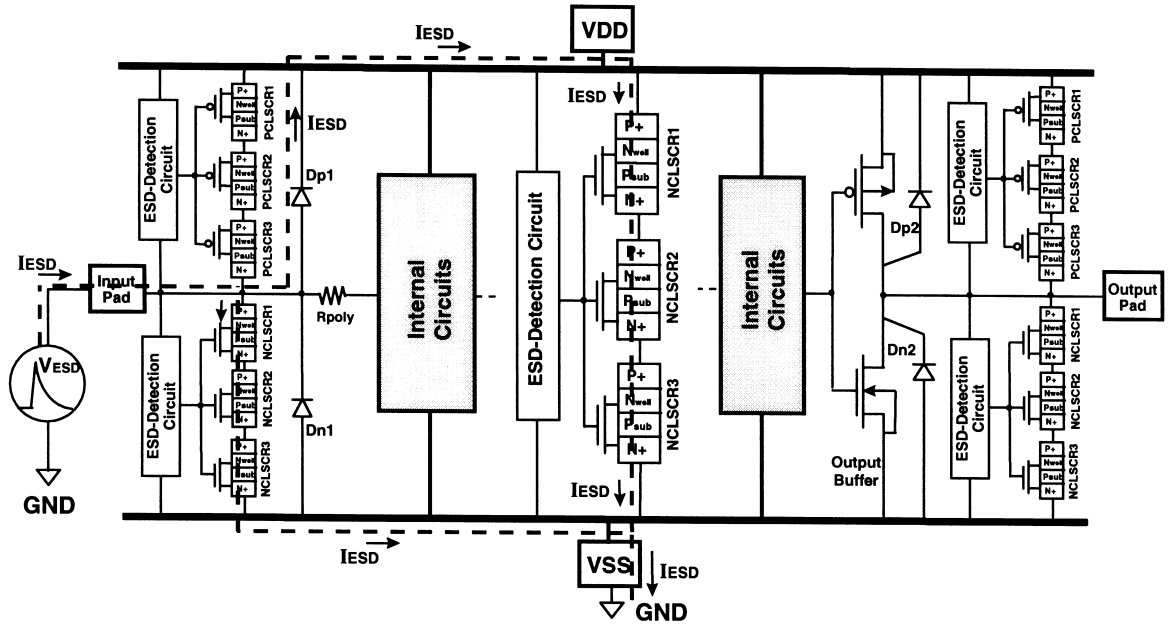


(a)

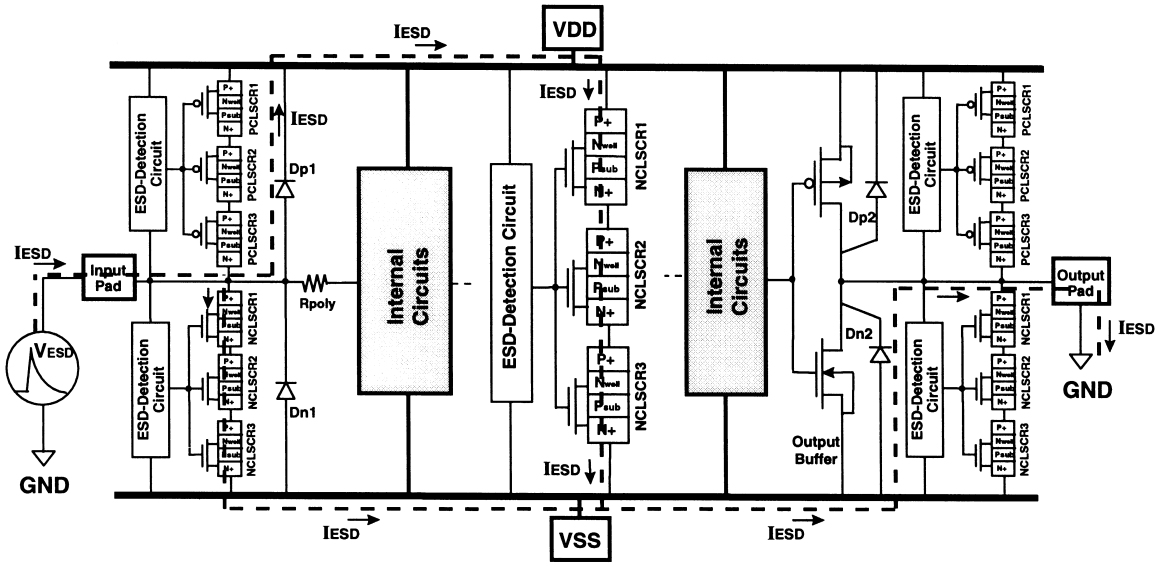


(b)

Fig. 24. The VDD-to-VSS ESD clamp circuit using (a) the cascoded 3-NCLSCRs, and (b) the cascoded 3-PCLSCRs, with the *RC*-based control circuit.



(a)



(b)

Fig. 25. The ESD current paths (shown by the dashed lines) in the whole-chip ESD protection scheme during (a) the Input-to-VSS ESD stress, and (b) the pin-to-pin ESD stress.

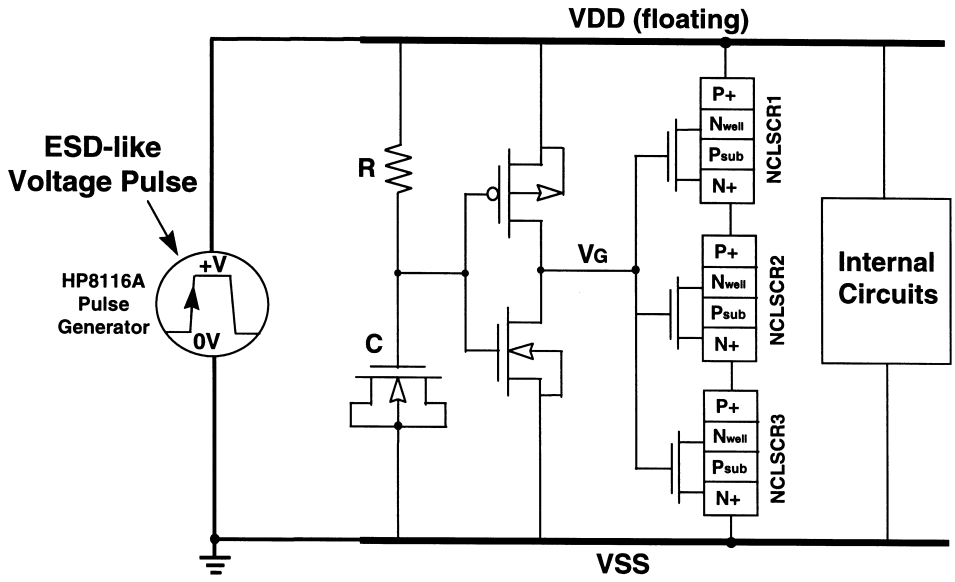


Fig. 26. The experimental setup to verify the turn-on behavior of the VDD-to-VSS ESD clamp circuit with the cascoded LVTSCRs during the ESD-stress condition.

6.2. Turn-on verification

To verify the turn-on behavior of the cascoded NCLSCRs in the VDD-to-VSS ESD clamp circuit, an experimental setup is shown in Fig. 26, where an ESD-like voltage pulse generated from a pulse generator (*hp*8116A) is applied to the VDD power line with the VSS grounded. A 0–8 V voltage pulse with a pulse width of 400 ns and a rise time of ~6 ns is applied to the VDD power line. If the cascoded NCLSCRs in the VDD-to-VSS ESD clamp device are triggered, the 0–8 V voltage pulse will be degraded and clamped to the voltage level around the total holding voltage of the cascoded NCLSCRs. The typical voltage waveform of the 0–8 V voltage pulse degraded by the cascoded 3-NCLSCRs is shown in Fig. 27(a). When the 0–8 V voltage pulse is applied, the cascoded 3-NCLSCRs is triggered and clamps the voltage pulse to the voltage level of 4.75 V, which corresponds to the holding voltage of the cascoded 3-NCLSCRs. From the degraded waveform in Fig. 27(a), it was also shown that the cascoded 3-NCLSCRs have a turn-on time of ~20 ns to fully clamp the applied 0–8 V voltage pulse on the VDD power line. If the ESD clamp circuit only has a single NCLSCR between the VDD and VSS power lines, the applied 0–8 V voltage is clamped to only 1.5 V in Fig. 27(b). In Fig. 27(b), the single NCLSCR also takes a time of ~20 ns to fully turn itself on. From the turn-on time between the Fig. 27(a) and (b), it approves that the turn-on time is not increased when the cascoded NCLSCRs have more NCLSCR devices in the cascode configuration. After the cascoded NCLSCRs are triggered, the clamped voltage level is proportional to the holding voltage of the cascoded NCLSCRs. This has verified the turn-on efficiency of the cascoded NCLSCRs in the ESD-stress condition.

But, in the normal operating condition with 3-V VDD and 0-V VSS power supplies, the cascoded NCLSCRs in the ESD clamp circuit should not stay in the turn-on state after the triggering of the overshooting voltage pulse on the VDD power line. To verify this issue, an experimental setup is shown in Fig. 28, where a 3–4 V overshooting voltage pulse is applied to the VDD power line with the VDD-to-VSS ESD clamp circuit. The measured results at 25°C are shown in Fig. 29(a) and (b) for the ESD clamp circuit with the cascoded 3-NCLSCRs and a single NCLSCR, respectively. In Fig. 29(a), the 3–4 V overshooting voltage pulse on the VDD power line is not degraded, because the cascoded 3-NCLSCRs are not triggered into their holding region by such an overshooting voltage pulse. But, in Fig. 29(b), the 3–4 V overshooting voltage pulse on the VDD power line is degraded and kept at 1.5 V after the triggering of the 3–4 V overshooting voltage pulse, because the single NCLSCR in the VDD-to-VSS ESD clamp circuit is triggered into its latchup state by this overshooting voltage pulse. The turned-on single NCLSCR in the ESD clamp circuit keeps the voltage level on the VDD power line to only 1.5 V. This causes the so-called latchup problem in CMOS ICs. Thus, the VDD-to-VSS ESD clamp circuit or the input/output ESD protection circuits in

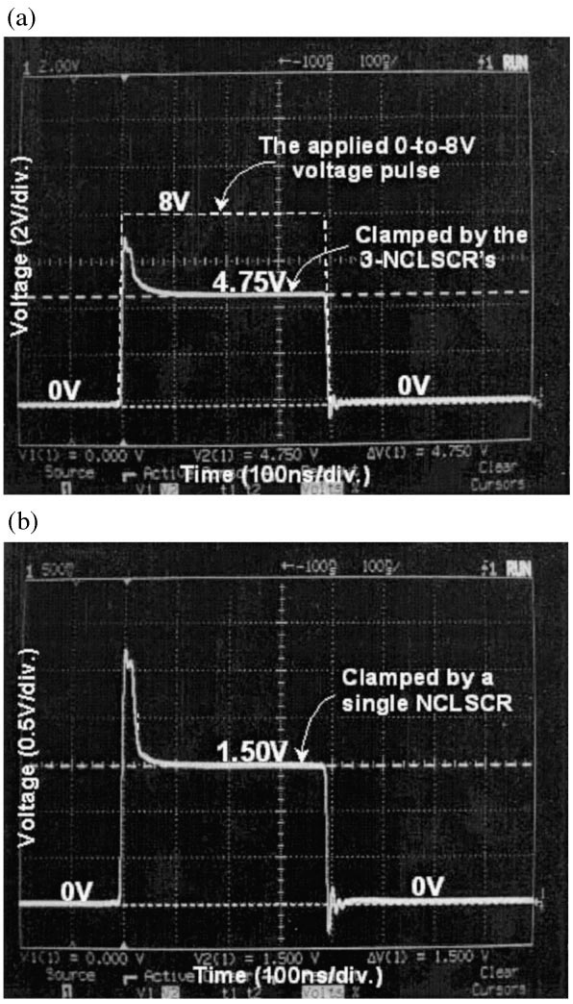


Fig. 27. The degraded voltage waveforms on the 0–8 V voltage pulse clamped by the VDD-to-VSS ESD clamp circuit with (a) the cascoded 3-NCLSCRs, and (b) a single NCLSCR.

CMOS ICs with a single LVTSCR are dangerous to the latchup problem in the noisy environments.

To further verify the safe application of the cascoded LVTSCRs, a larger 3–8 V overshooting voltage pulse is applied to the VDD power line with the VDD-to-VSS ESD clamp circuit, when the IC is in the normal operating condition with 3-V VDD and 0-V VSS power supplies. The measured waveforms at 25°C are shown in Fig. 30(a) and (b) for the ESD clamp circuit with the cascoded 3-NCLSCRs and the cascoded 2-PCLSCRs, respectively. In Fig. 30(a), the 3–8 V overshooting voltage pulse is clamped by the cascoded 3-NCLSCRs to the voltage level of 4.937 V. But, after the triggering of the 3–8 V overshooting voltage pulse, the VDD voltage level is restored to the original 3 V. This means that the 3-NCLSCRs can effectively clamp the overshooting voltage pulse on the VDD power line but do not cause the VDD-to-VSS latchup problem in the ESD clamp circuit when the IC is in the normal operating condition.

In Fig. 30(b), the 3–8 V overshooting voltage pulse is clamped by the cascoded 2-PCLSCRs to the voltage level of 3.625 V. But, after the triggering of the 3–8 V overshooting voltage pulse, the VDD voltage level is also restored to the original 3 V. Because the holding voltage of the cascoded 2-PCLSCRs at 25°C is around 3.22 V, the cascoded 2-PCLSCRs can automatically turn off after the VDD voltage level is returned to 3 V. As shown in Fig. 18, the holding voltage of the cascoded 2-PCLSCRs is decreased to only 2.4 V when the temperature is increased to 150°C. This implies that the cascoded 2-PCLSCRs are somewhat dangerous to the latchup problem, if the CMOS ICs with 3-V VDD are operating in the high-temperature environments.

By changing the number of the PCLSCR (NCLSCR) devices in the cascode configuration, the noise margin of such cascoded LVTSCRs can be adjusted to overcome the system-level overshooting or undershooting noise pulses. To more feasibly adjust the total holding voltage in the cascode configuration, the series diodes can be inserted among the cascoded NCLSCRs or PCLSCRs to achieve different applications [44].

6.3. ESD robustness

The VDD-to-VSS ESD clamp circuits designed in Fig. 24 with different number of cascoded NCLSCRs or cascoded PCLSCRs are tested by the human-body-model (HBM) ESD stress. The failure criterion is defined as that the leakage current under the 5-V bias from VDD to VSS is greater than 1 μA. The HBM ESD robustness per device width (V_{ESD}/W) of the cascoded NCLSCRs or the cascoded PCLSCRs is shown in Fig. 31, where a gate-grounded NMOS (ggNMOS) with a device dimension (W/L) of 480/0.5 (μm/μm) in the same 0.35-μm bulk CMOS process is also tested for reference. All the cascoded NCLSCRs, PCLSCRs, and the ggNMOS are fabricated with neither the ESD-implant process nor the silicide-blocking process. The ESD robustness per device width (V_{ESD}/W) of the cascoded 3-NCLSCRs (ggNMOS) is 50 V/μm (3.13 V/μm) in the 0.35-μm bulk CMOS process. The NMOS (PMOS) inserted in each NCLSCR (PCLSCR) device has a channel length of only 0.35 μm. The ggNMOS (W/L = 480/0.5) occupies a layout area of 80×76 μm^2 can sustain an HBM ESD level of only 1.5 KV. But the cascoded 3-NCLSCRs with a layout area of 60×60 μm^2 can sustain a 3-kV HBM ESD stress, where each NCLSCR has a device dimension (W/L) of only 60/20 (μm/μm). So, the ESD robustness per layout area of the cascoded 3-NCLSCRs (ggNMOS) can be

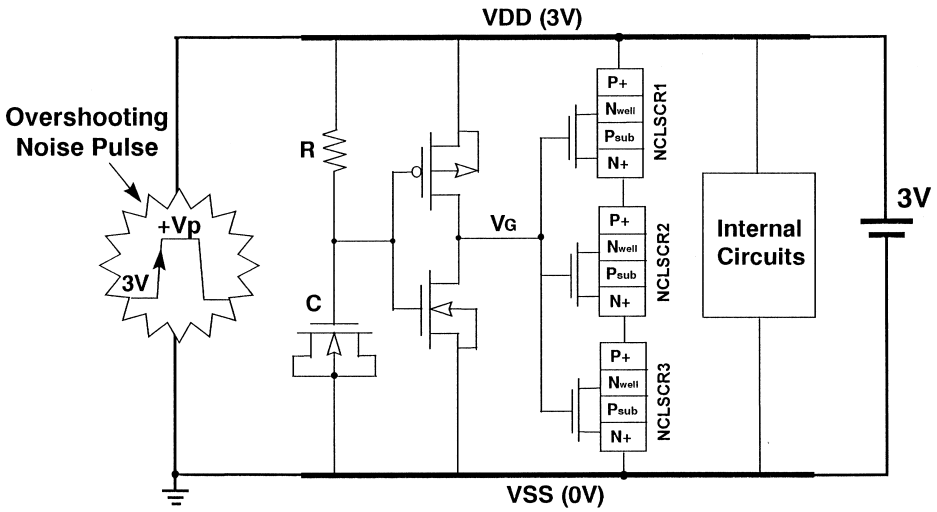


Fig. 28. The experimental setup to verify the turn-on behavior of the VDD-to-VSS ESD clamp circuit with the cascoded LVTSCRs in the normal operating condition with 3-V VDD bias and the overshooting noise pulse.

0.83 V/μm^2 (0.25 V/μm^2) in the 0.35-μm bulk CMOS process without using the extra silicide-blocking and ESD-implant process steps. Although the ESD performance of the cascoded LVTSCRs is degraded while the number of the LVTSCRs in the cascode configuration is increased, the ESD robustness and area efficiency of the cascoded LVTSCRs in 3-V application is still much better than that of the ggNMOS in the 0.35-μm bulk CMOS process.

When the additional silicide-blocking mask is used in the 0.35-μm bulk CMOS process, the HBM ESD level of the ggNMOS (W/L = 480/0.5) can be improved to 6 kV, where the ggNMOS has a silicide-blocking layout clearance of 2.6 μm (0.6 μm) in its drain (source) region. Therefore, the HBM ESD robustness per device width (V_{ESD}/W) of the ggNMOS is improved to around 12.5 V/μm. But, the ESD level of the cascoded LVTSCRs is not significantly improved by the additional silicide-blocking mask in the 0.35-μm bulk CMOS process. Because the ESD current discharging in the LVTSCR is through the SCR deeper current path rather than the NMOS shallow surface current path, the ESD level of the cascoded LVTSCRs is therefore not degraded by the silicided-diffusion process in the 0.35-μm bulk CMOS technology. Although the ESD level of ggNMOS can be rescued by the silicide-blocking mask, the additional mask and process steps increase the cost and fabrication period of IC products.

This work provides a practical and cost-efficient design on the LVTSCRs to still safely apply such LVTSCRs for effective whole-chip ESD protection in the bulk CMOS technologies without additional silicide-blocking and ESD-implanted processes. With a tunable holding voltage greater than the VDD voltage level of CMOS ICs, the cascoded LVTSCRs can help to clamp the overshooting/undershooting noise pulses but do not cause the latchup danger when the IC is operating in the application system even in noisy environments.

7. Conclusion

The LVTSCR had been reported for on-chip ESD protection in CMOS ICs, but such devices can be triggered by the overshooting or undershooting of noise pulses to cause a latchup danger when the ICs are operated under normal conditions. In this work, a practical solution using cascoded LVTSCRs has been successfully designed in the bulk CMOS processes to safely apply the LVTSCR for effective component-level ESD protection but without the fatal latchup trouble when the ICs are operating in system applications or in the system-level ESD/EMC reliability tests. The device characteristics of the cascoded LVTSCRs in a 0.35-μm bulk CMOS process has been experimentally investigated in more detail. The holding voltage of the cascoded LVTSCRs can be linearly adjusted by changing the number of LVTSCR devices in the cascode configuration for different applications. This cascoded-LVTSCRs design has been practically applied to protect the CMOS ICs in a 0.35-μm silicide CMOS technology with the HBM ESD robustness above 3 kV.

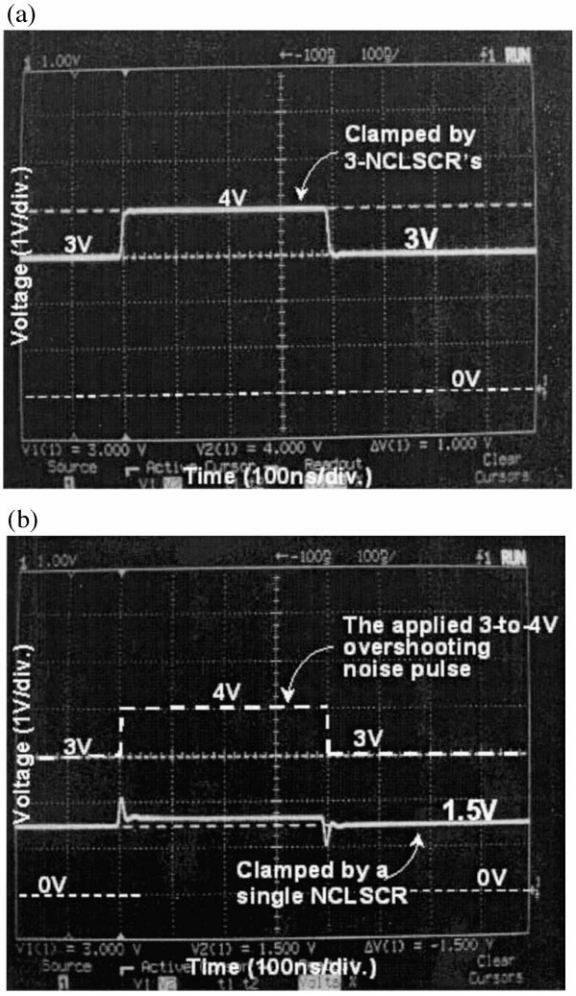


Fig. 29. The voltage waveforms of the 3–4 V overshooting voltage pulse clamped by the VDD-to-VSS ESD clamp circuit with (a) the cascoded 3-NCLSCRs, and (b) a single NCLSCR.

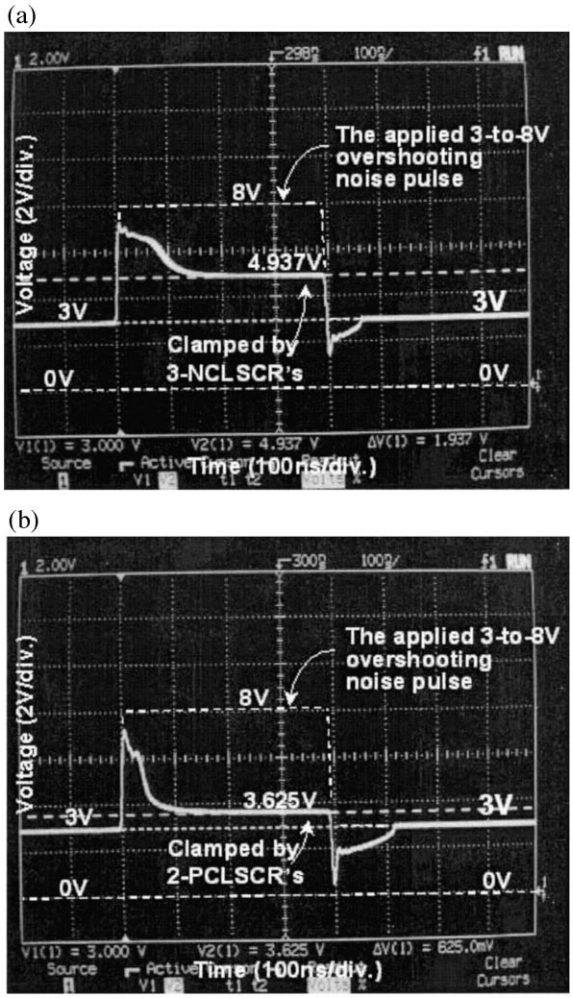


Fig. 30. The degraded voltage waveforms of the 3–8 V overshooting voltage pulse clamped by the VDD-to-VSS ESD clamp circuit with (a) the cascoded 3-NCLSCRs, and (b) the cascoded 2-PCLSCRs.

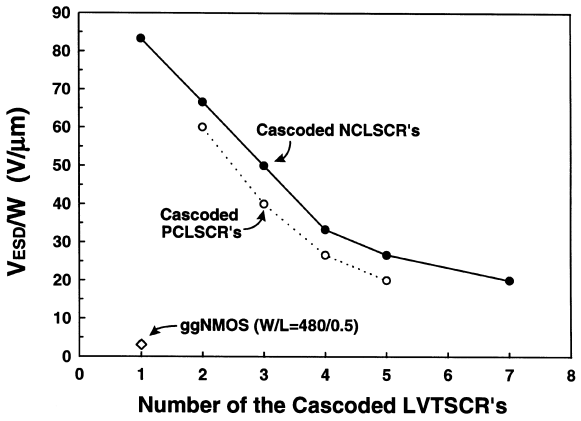


Fig. 31. The HBM ESD robustness per device width (V_{ESD}/W) of the cascoded LVTSCRs with different number of NCLSCR or PCLSCR devices.

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