Gate Oxide Integrity of Thermal Oxide Grown on High Temperature Formed $Si_{0.3}Ge_{0.7}$

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***Abstract*—We have investigated the gate oxide integrity of thermal oxides direct grown on high temperature formed $Si_{0.3}Ge_{0.7}$. Good oxide integrity is evidenced by the low interface-trap density of 5.9×10^{10} $eV^{-1}cm^{-2}$, low oxide charge density of -5.6×10^{10} cm^{-2}, and the small stress-induced leakage current after –3.3 V stress for 10 000 s. The good gate oxide integrity is due to the high temperature formed and strain-relaxed $Si_{0.3}Ge_{0.7}$ that has a original smooth surface and stable after subsequent high temperature process.**

***Index Terms*—Gate oxide integrity, SiGe oxide, stress-induced leakage current.**

I. Introduction

GATE oxide integrity [1]–[6] is one of the most important factors for process integration. Although SiGe channel p-MOSFET's [5]–[11] have improved current-drive capability, operation speed, and package density of CMOS circuits, the gate oxide integrity is still unexamined. To prevent strain relaxation and defect generation, low temperature ($T < 800$) processing is necessary for SiGe p-MOSFET. Unfortunately, both gate oxide integrity and junction leakage are much degraded at the limited low temperature [12], and also obstacles further process integration with modern high-K gate dielectric [13], [14]. Recently, we developed a new SiGe formation process using deposited amorphous Ge followed by rapid thermal annealing (RTA) [15]. Because SiGe is formed by solid phase epitaxy at high temperatures similar to silicide formation [16], better thermal stability can be expected. High hole mobility of 250 cm^2/Vs and low source-drain p^+n junction leakage are obtained using high temperature (950 °C) RTA of B^+ implanted damages [17]. In this letter, we have further investigated the gate oxide integrity of thermal oxide directly grown on high temperature formed SiGe. Good oxide integrity is evidenced by low interface-trap density, smooth surface, and small stress-induced leakage current (SILC), which is attributed to the high SiGe forming temperature and no rough surface or pinholes [9]–[11] are formed during subsequent device processing.

II. Experimental

Standard 4-in p-type (100) Si wafers were used in this work. In addition to SiGe oxides, Si control oxides were also fabricated as references. After device isolation, ~120 Å amorphous Ge layer is deposited on active region. An HF-vapor passivation is used to suppress the native oxide formation before Ge deposition [3], [14]–[17]. A 200 Å $Si_{0.3}Ge_{0.7}$ with good crystalline quality was then formed by RTA at 900 °C as measured by cross-sectional TEM and X-ray diffraction. More detailed material characterization can be found in our previous study [16], [17]. Gate oxides of 50 Å were then grown by dry O_2 at 900 °C for both $Si_{0.3}Ge_{0.7}$ and Si control sample. Gate capacitors were formed after a 3000 Å poly-Si deposition, phosphorus doping and subsequent patterning.

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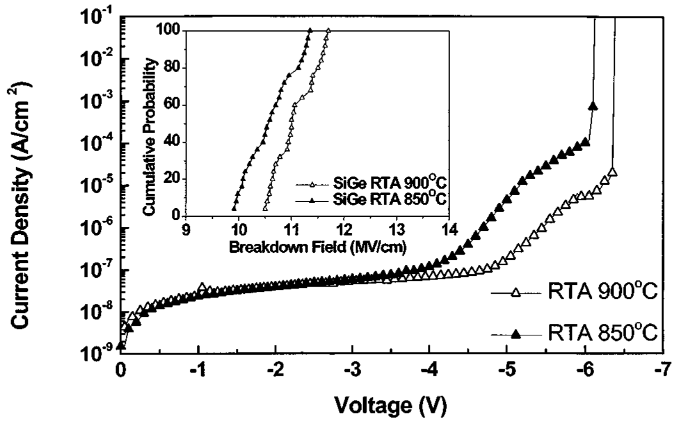

Fig. 1. *I–V* characteristics of 50 Å thermal oxides grown on 850 and 900 °C RTA formed $Si_{0.3}Ge_{0.7}$. The insert figure is the cumulative probability for breakdown electric field.

III. Results and Discussion

Fig. 1 shows current–voltage (*I–V*) characteristics of thermal oxides grown on 850 and 900 °C RTA formed $Si_{0.3}Ge_{0.7}$, respectively. Inset figure is the cumulative probability for breakdown electric field. Note that oxide grown on 850 °C RTA SiGe has lower breakdown electric field as compared to that grown on 900 °C SiGe. The degraded oxide property as decreasing SiGe formation temperature may be due to either strain relaxation or higher defect density by lower formation temperature. However, either mechanism may be a fundamental limitation of gate oxide integrity using low temperature MBE or CVD grown SiGe. A breakdown electric field of 11 MV/cm is obtained from thermal oxide grown on 900 °C formed SiGe that is still lower than conventional SiO_2. Possible reason may be due to the presence of weaker GeO_2 inside the SiO_2 matrix as measured by SIMS similar to literature report [18]. However, the Ge peak decreases an order of magnitude within 10 Å from interface and most part of this oxide is primarily SiO_2 form.

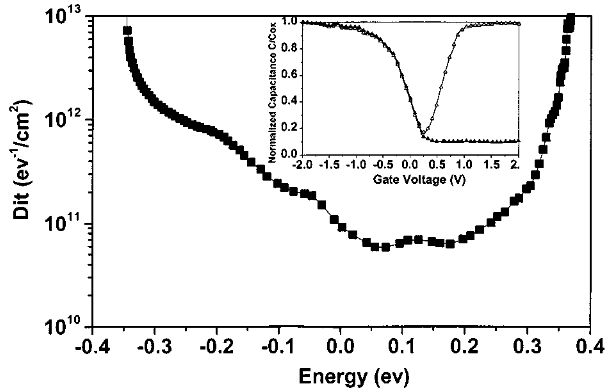

Fig. 2. Interface-trap density of 50 Å thermal oxide as a function of energy obtained from the insert quasistatic and high frequency *C–V* curves.

Oxide charge and interface trap density are other important factors for gate oxide integrity, which are directly related to low frequency device noise [19]. Fig. 2 shows the interface-trap density obtained from the insert capacitance–voltage (*C–V*) curves. A substrate doping concentration of $\sim 5 \times 10^{15}$ cm^{-3} is extracted from *C–V* that is consistent with the measured sheet resistivity on this wafer. A low interface-trap density of 5.9×10^{10} eV^{-1}cm^{-2} and a oxide charge density of -5.6×10^{10} cm^{-2} are obtained that are the lowest reported values on direct thermally oxidized SiGe. The low concentration of oxide traps further explains the measured high interface hole mobility and current drive capability reported previously [17]. The negative oxide charge is believed to be due to the electron traps formed in SiGe oxide.

To further understand the low oxide traps, we have also measured the surface roughness using atomic force microscopy (AFM). Fig. 3(a) and (b) show the AFM images of $Si_{0.3}Ge_{0.7}$ surface before and after oxidation, respectively. RMS roughness values of 1.55 and 1.60 Å are measured on respective $Si_{0.3}Ge_{0.7}$ surface and oxide that indicates the oxidation process did not roughen the initial SiGe surface. It is also important to notice that the surface smoothness of $Si_{0.3}Ge_{0.7}$ is comparable to standard Si surface. The smooth $Si_{0.3}Ge_{0.7}$ surface may be due to the similar solid phase epitaxy as $CoSi_2$ formation [16]. In contrast to previous reports, no rough surface or pinholes are observed even for a high Ge composition up to 70% [9]–[11]. This may be due to the high temperature formed $Si_{0.3}Ge_{0.7}$ that is already strained relaxed as confirmed by the very sharp XRD linewidth after oxidation with near identical peak position and linewidth to as formed $Si_{0.3}Ge_{0.7}$.

Reliability is another important issue for practical process integration of SiGe gate oxide. We have also investigated the reliability using a constant voltage stress. Fig. 4 shows the SILC effect from the insert figure after a -3.3 V stress for 10 000 s. The small SILC indicates excellent gate oxide reliability that is attributed to the smooth oxide surface and related uniform electric field distribution over oxide area [3]. The good reliability also suggests that the high temperature strain relaxed and stable $Si_{0.3}Ge_{0.7}$ is the essential factor to achieve good oxide integrity.

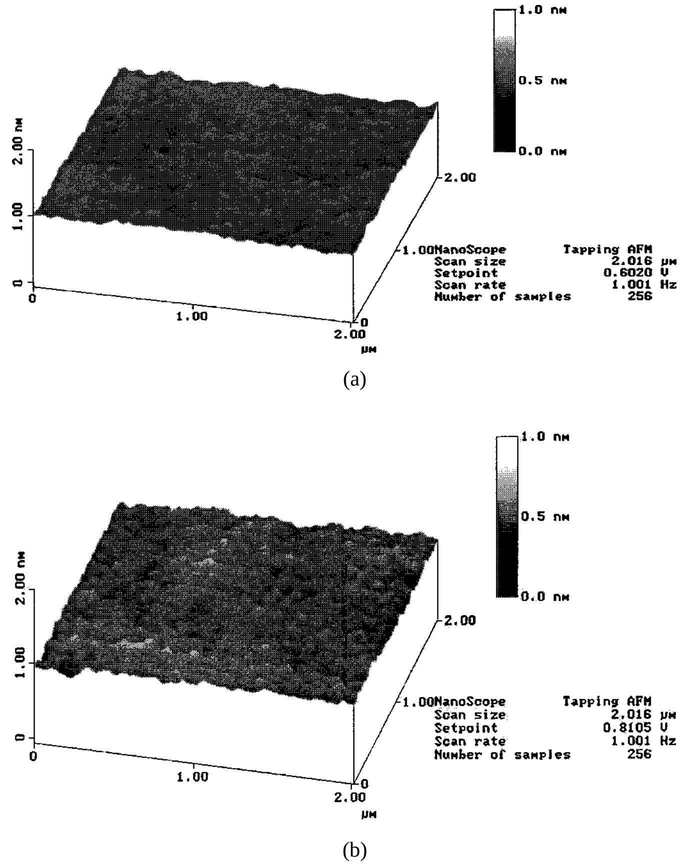

Fig. 3. AFM images of 50 Å thermal oxide grown on $Si_{0.3}Ge_{0.7}$ surface (a) before and (b) after oxidation.

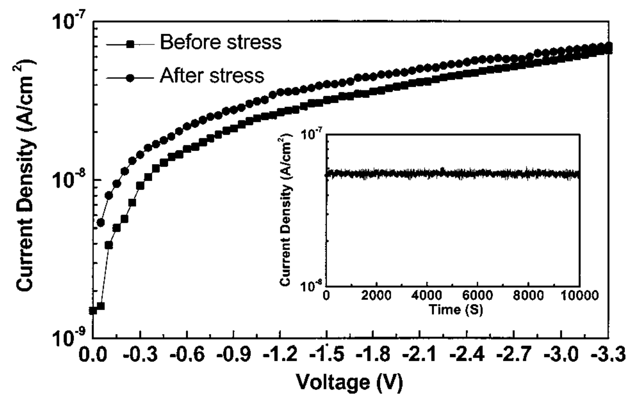

Fig. 4. SILC effect after −3.3 V stress for 10 000 s on 50 Å thermal oxide grown on $Si_{0.3}Ge_{0.7}$. The insert figure is the current density during the stress.

IV. Conclusion

Good oxide integrity is obtained from direct thermally oxidized $Si_{0.3}Ge_{0.7}$. This is evidenced by low oxide-trap density, smooth surface, and small SILC. The good gate oxide integrity is due to the high temperature formed and strain-relaxed $Si_{0.3}Ge_{0.7}$ that has a very smooth surface and stable after subsequent high temperature process

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