A New Observation of Band-to-Band Tunneling Induced Hot-Carrier Stress Using Charge-Pumping Technique

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***Abstract*—The lateral distributions of interface-states ($N_{\rm it}$) and oxide-trapped charges ($Q_{\rm ox}$) generated by band-to-band tunneling (BTBT) induced hot-carrier stress are analyzed by the new charge-pumping method. It is shown that the interface-states and oxide-trapped charges should be originated from different types of carriers due to the separation of the locations of their peak values. The further evidence of the measured distribution of the interface-states in the band-gap shows that the carriers travelled toward the gate edge would be the dominant carrier for the generation of interface-states while the carriers travelled away from the gate edge will generate oxide-trapped charges through the help of the vertical electric field. These results should be very useful for the reliability analysis of flash memories.**

***Index Terms*—BTBT, Charge-pumping technique, interface-states, MOSFET, oxide-trapped charges.**

I. INTRODUCTION

BAND-TO-BAND tunneling induced hot-carrier stress is one of the most serious reliability issues for deep-submicrometer MOSFET's and flash memories. With the continuing scaling down of MOS devices, the electric field under the gate-to-drain overlap region would be very large when the device is operated in off-state, and the significant BTBT current may exist and interface-states and oxide-trapped charges might be generated. For flash memories, among many erase methods, the gate edge Fowler–Nordheim (F–N) tunneling mechanism has been widely used to discharge the floating gate electrode; the source-side erase generates electrons and holes through the surface-field induced band-to-band tunneling in the $\rm N^+$-to-gate overlap region, and some of these holes may gain enough energy from the lateral electric field and can inject into the oxide with the help of a negative gate bias [1], [2]. Some researchers [3], [4] thought that the carriers traveling away from the gate edge would be the dominant effect for the generation of interface-states and oxide-trapped charges, and the damages caused by the carriers traveling toward the gate edge were not be considered. More recently, the electron injection method using band-to-band tunneling induced electrons (BBHE) for flash memory with a p-channel cell was proposed [5], which ensures the realization of high program efficiency, high scalability and hot-hole-injection-free operation. Therefore, the realibility issues of the BBHE deserves further study. In this letter, the new charge-pumping technique was used to profile the interface-state distributions in the band-gap and the lateral distribution of interface-states and oxide-trapped charges, which can help us realize what kind of carriers may be the dominant effect for the generation of the interface-states or oxide-trapped charges.

II. EXPERIMENTAL TECHNIQUE

The recently developed new charge-pumping technique [6] was used to profile the lateral distribution of $N_{\rm it}$ and $Q_{\rm ox}$. Fig. 1 shows the experimental setup for charge-pumping current measurement, where the gate pulse is provided by a HP8110 pulse generator and a HP4145B parameter analyzer is used to monitor the charge-pumping current. Keeping the rising slope (S_r) and falling slope (S_f) constant and varying the high-level ($V_{\rm GH}$) and base-level ($V_{\rm GL}$) of the gate pulse, the lateral distributions of $N_{\rm it}$ and $Q_{\rm ox}$ can be obtained. The equations used to calculate $N_{\rm it}$ and $Q_{\rm ox}$ are given in the insert of Fig. 1, where W is channel width; f is the frequency of the gate pulses; Δx is the effective charge-pumping region defined by $V_{\rm GH1}$ and $V_{\rm GH2}$; $V_{\rm GH,1/2,fresh}$ ($V_{\rm GH,1/2,stress}$) is the half-maximum value of $\Delta I_{\rm cp}/f - V_{\rm GH}$ curve before (after) stress while $V_{\rm GL,1/2,fresh}$ ($V_{\rm GL,1/2,stress}$) is that of $\Delta I_{\rm cp}/f - V_{\rm GL}$ curve before (after) stress. In our new charge-pumping technique, $N_{\rm it}$ relataed to Δx is extracted from the saturation value of $\Delta I_{\rm cp}/f - V_{\rm GH}$ curve. In addition, $V_{\rm GL,1/2,fresh}$ ($V_{\rm GL,1/2,stress}$) is extracted from $\Delta I_{\rm cp}/f - V_{\rm GL}$ curves before (after) stress so that the interference induced by the generated $N_{\rm it}$ for extracting $Q_{\rm ox}$ can be eliminated by our method. Hence, a reliable lateral distribution of $Q_{\rm ox}$ can be obtained.

To profile the distribution of $N_{\rm it}$ in the band-gap, S_r and S_f, which are the rise time (t_r) and fall time (t_f), are varied with fixed $V_{\rm GH}$ and $V_{\rm GL}$ to detect the lower part and upper part of $N_{\rm it}$ in the band-gap, respectively. According to [7], the distribution in the upper part and lower part of the bandgap can be extracted by the equations listed in the insert of Fig. 1, where E_i is the intrinsic Fermi energy; σ_{n0} (σ_{p0}) is the electron (hole) capture-cross-section; $v_{\rm th}$ is the thermal velocity; n_i is the intrinsic carrier concentration, and $t_{\rm eme}$ ($t_{\rm emh}$) is the nonsteady-state electron (hole) emission time. Note that σ_{n0} (σ_{p0}) are extracted from (21) and (22) using our previous work [8].

The test device is a conventional counter-implanted p-MOSFET with the mask length of 0.85 μm, the channel width of 120 μm and the oxide thickness of 110 Å, the

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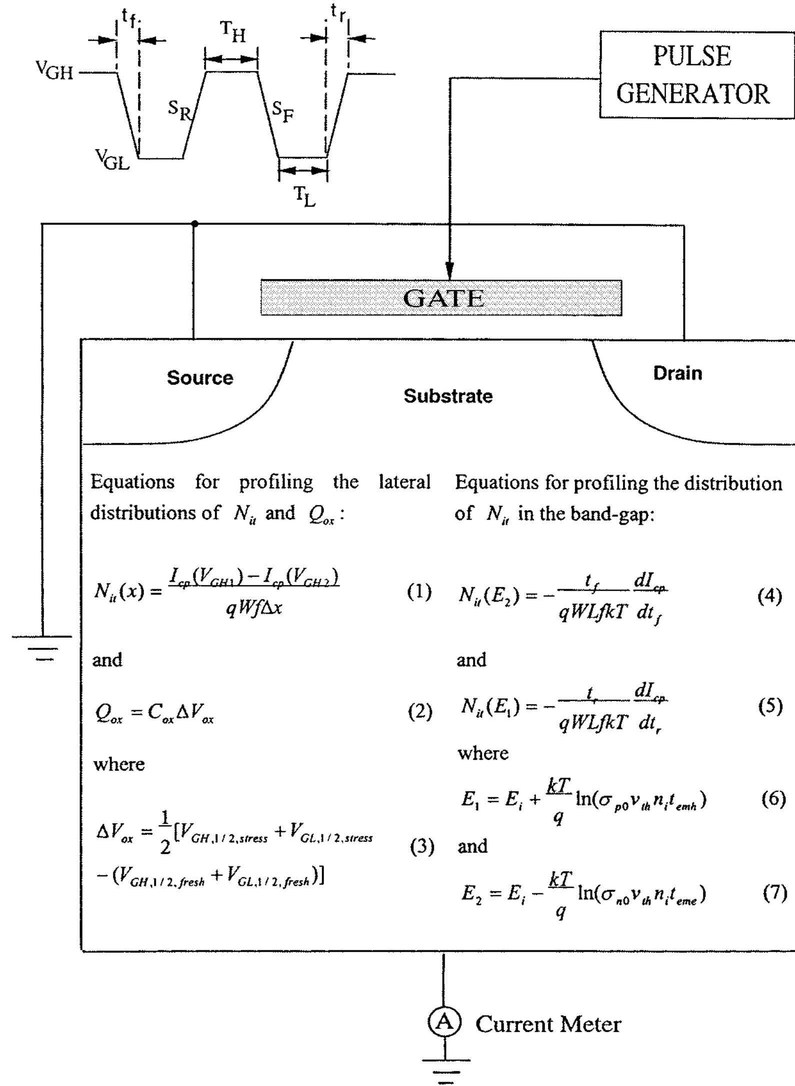

Fig. 1. Experimental setup of the charge-pumping measurement and the shape of the gate pulse. The inserts are the equations used to extract $N_{\rm it}$ and $Q_{\rm ox}$.

device structure parameters used in two-dimensional (2-D) device simulation are extracted by accurately simulating the current–voltage (*I–V*) characteristics of the fresh devices.

In our experiment, the measured data of the BTBT current is simulated by a new quasi–2-D BTBT current model [9] first, then the stress condition of $V_D = -6$ V and $V_G = 3$ V is chosen for the BTBT-induced hot-carrier stress to ensure that the damages are mainly generated by the carriers induced by the BTBT. The simulated result also reveals that the BTBT mainly occurs at the point where the drain concentration N_A is 1.2×10^{18} cm^{-3}.

III. Results and Discussion

Based on our developed new charge-pumping technique, the interface-states and the oxide-trapped charges generated by BTBT-induced hot carrier stress were measured.

Fig. 2 shows that significant interface-states and electron-traps are generated with cumulative stress time. It should be noted that their positions of the peak value do not locate at the same point. This is different to the result shown in [4], where they thought that the interface-states and oxide-trapped charges were generated by the carriers traveling away from the gate edge so that the locations of the peak value of both the interface-states and oxide-trapped charges should be the same and were ahead of the peak electric field. In theory, excluding the measurement errors, the locations of the peak interface-states and oxide-trapped charges should coincide each other if the interface-states and oxide-trapped charges are generated by the same carriers. But, according to our measured distribution of the interface-states in the band-gap shown in Fig. 3, the interface-states are mainly generated near the valance-band edge with cumulative stress time. Because the electrons may travel only in the conduction-band while the holes may travel only in the valance-band. Therefore, the hot electrons may have the higher probability to generate interface-states near the conduction-band edge while the hot holes may have the higher probability to generate those near the valance-band edge. This implies that the dominant carrier for the generation of the interface-states is hole, that is, the carriers traveling toward the gate edge. Therefore, according to Figs. 2 and 3, the mechanism

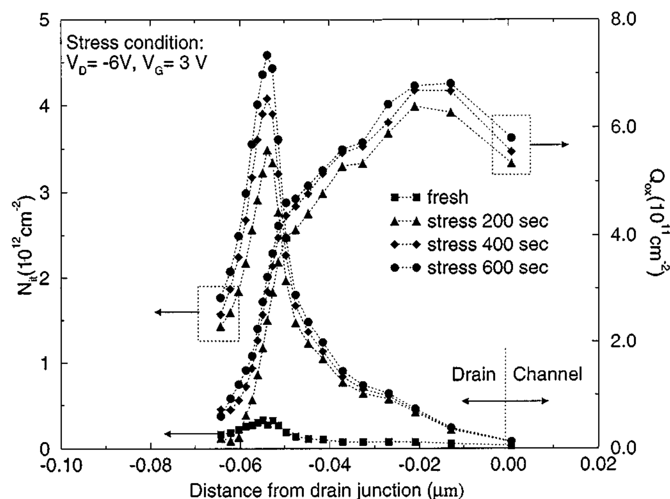

Fig. 2. Lateral distribution of the cumulative interface-states and oxide-trapped charges with the stress condition of $V_D = -6$ V and $V_G = 3$ V.

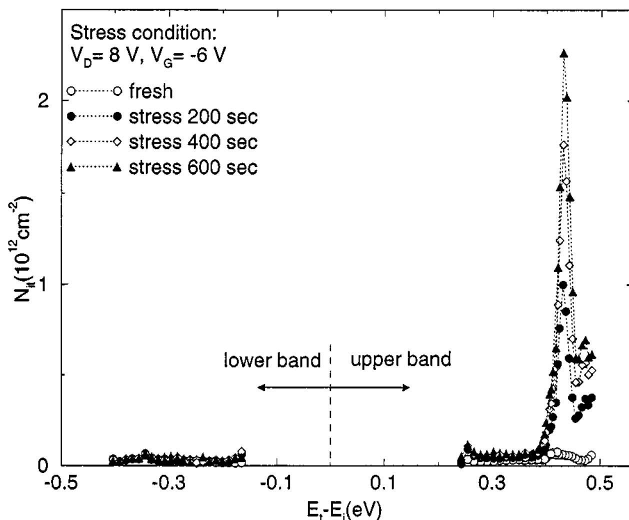

Fig. 4. Distribution of the cumulative interface-states in the band-gap with the stress condition of $V_D = 8$ V and $V_G = -6$ V for LDD n-MOSFET.

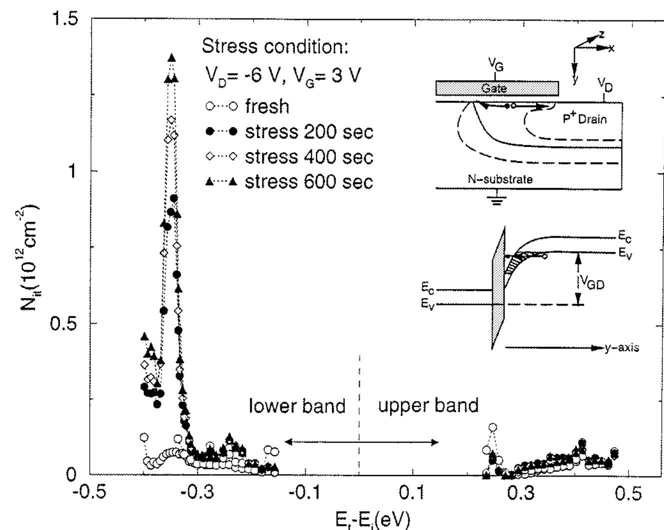

Fig. 3. Distribution of the cumulative interface-states in the band-gap with the stress condition of $V_D = -6$ V and $V_G = 3$ V for conventional counter-implanted p-MOSFET. The inserts are the band structure reflecting the BTBT process and the physical direction of travel for the various carriers involved.

that the generated interface-states and oxide-trapped charges by the BTBT induced hot-carrier stress can be explained as follows. Taking p-MOSFET for example, as mentioned in Section II, the simulated results of BTBT current show that the BTBT mainly occurs at the point where the drain concentration N_A is 1.2×10^{18} cm^{-3}, which just locate between the peak value of the profiled interface-states and oxide-trapped charges shown in Fig. 2, as we inspect the simulated drain profile. Thus, as shown in the insert of Fig. 3, when the electron tunneling from the valance-band to the conduction-band, the electron will travel toward the channel region and may inject into the gate oxide with the help of the vertical electric field and would result in the generated oxide-trapped charges, as noted by many studies [1]–[4], while the generated holes in the valance-band will travel away from the channel region and would be accelerated by an increasing lateral electric field; eventually, the holes will become hot enough and then relax their energy to generate the interface-states.

To further verify our viewpoint, the distribution of interface-states in the band-gap for LDD n-MOSFET with the mask length of 0.8 μm, the channel width of 120 μm and the oxide thickness of 110 Å was measured. As shown in Fig. 4, the interface-states are generated almost near the condution band edge, while those near the valance-band edge are nearly invariant with increasing the stress time. Therefore, the same as p-MOSFET, the generated interface-states are mainly contributed by the carriers traveling toward the gate edge, namely, electrons for LDD n-MOSFET.

IV. Conclusion

The separation of the peak value of the lateral dirstributions of interface-states and oxide-trapped charges generated by the BTBT induced hot-carrier stress reveals that the interface-states and oxide-trapped charges might be originated from different types of carriers. The distribution of interface-states in the band-gap shows that the carriers traveling toward the gate edge may encounter an increasing electric field and become hot to generate the interface-states, while the carriers traveling away from the gate edge may encounter a decreasing lateral electric field and might not be hot enough to generate the interface-states, but have the probability to inject into the gate oxide and generate oxide-trapped charges through the polarity of applied gate bias.

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