# High Performance 0.1 $\mu$m Dynamic Threshold MOSFET Using Indium Channel Implantation

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***Abstract*—In this letter, we demonstrate a high-performance 0.1 $\mu$m Dynamic Threshold Voltage MOSFET (DTMOS) for ultra-low-voltage (i.e., $<0.7$ V) operations. Devices are realized by using super-steep-retrograde indium-channel profile. The steep indium-implanted-channel DTMOS can achieve a large body-effect-factor and a low $V_{\rm th}$ simutaneously, which results in an excellent performance for the indium-implanted DTMOS.**

***Index Terms*—DTMOS, indium SSR.**

## I. Introduction

THE power supply voltage, $V_{\rm DD}$, is scaling at a faster pace than threshold voltage, causing degradation in current driving capability and speed of devices. To enhance the current driving capability of MOSFET's at low supply voltage (e.g., $V_{\rm DD} < 0.7$ V), F. Assaderaghi *et al.* [1] proposed using the **D**ynamic **T**hreshold Voltage **MOS**FET (DTMOS) for ultra-low voltage applications. The dynamic threshold scheme appears to be a very promising candidate for low-power and high-speed circuit applications since it improves the circuit speed without increasing the stand-by power consumption. By shorting its gate to the body, DTMOS operates with normal or high $V_{\rm th}$ in off-state to reduce stand-by power consumption; while operating with reduced $V_{\rm th}$ in on-state to enhance driving capability. Previously reported DTMOS's generally have small body-effect-factor $(\gamma)$ due to the low $V_{\rm th}$ and therefore do not take full advantage of the high current drive inherent in DTMOS [2]–[5]. However, it is very difficult to achieve a large body-effect-factor $(\gamma)$ and a low $V_{\rm th}$ simultaneously in the conventional MOSFET's. In this paper, we propose a DTMOS with super-steep-retrograde (SSR) channel profile by using indium implantation to overcome this problem. Experimental results demonstrate the superiority of indium-implanted DTMOS to conventional $BF_2$-DTMOS both in short- and narrow-channel devices.

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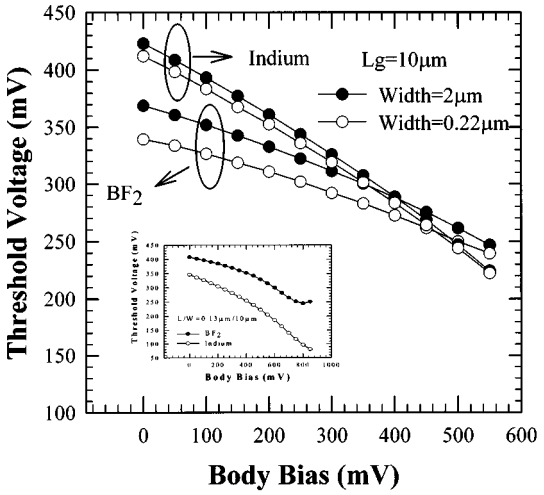


Fig. 1. Dependence of threshold voltage on the body bias for $BF_2$- and indium-implant devices with channel width 0.22 and 2 $\mu$m. Inset shows the result of device with $L/W = 0.13\ \mu{\rm m}/10\ \mu{\rm m}$ case.

## II. Experimental

Devices with channel length down to 0.1 $\mu$m were fabricated on 8-in Si wafers with resistivity of 15–25 $\Omega$-cm using a conventional CMOS twin-well process. Shallow trench isolation (STI) was used for device isolation. To form SSR channel, indium channel implant with a dose of $1\times10^{13}$ cm$^{-2}$, and at an energy of 150 keV was conducted. Conventional devices with $BF_2$-implant (at 50 keV) were also fabricated to serve as the control. Then, a 2.6-nm gate oxide was grown using rapid thermal oxidation (RTO), followed by the deposition of a 200-nm poly-silicon gate. After gate patterning, a 20-nm offset-space was used to reduce gate-to-drain capacitance. Ultra-shallow extensions were formed by a 4 keV As implant, followed by a boron pocket implant (20 keV, $1\times10^{13}$ cm$^{-2}$). After the formation of 0.1 $\mu$m sidewall spacer, a deep source/drain junction was formed by As ion implantation at 40 keV. Finally, wafers were annealed by rapid thermal processing (RTP) at 1000 °C for 20 s, followed by $CoSi_2$ salicidation process. Wafers were then processed through a standard backend flow to completion.

## III. Results and Discussion

Fig. 1 shows the body effects of n-channel MOSFET's with indium-implant and $BF_2$-implant (i.e., control). The device threshold voltage $V_{\rm th}$ is plotted as a function of the body bias for long channel transistors with narrow and wide channel widths. We found that the $V_{\rm th}$ of indium-implanted split is

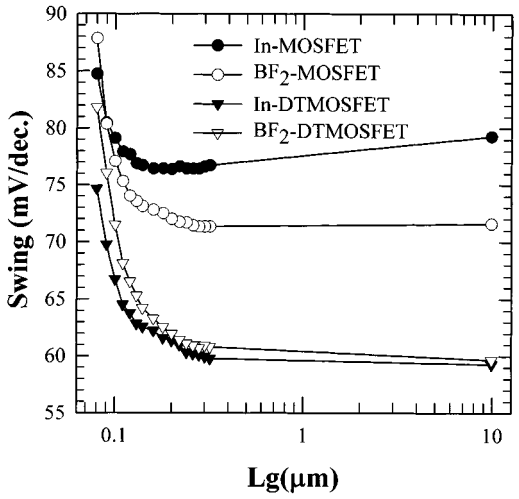


Fig. 2. Subthreshold swing as a function of channel length for conventional and DTMOS by using $BF_2$- and Indium-implant.

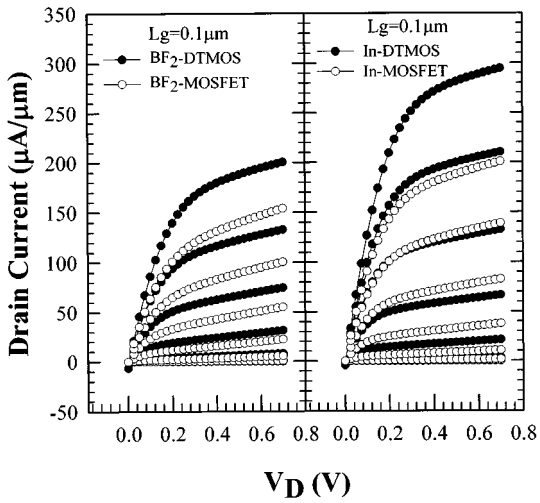


Fig. 4. Drain current of the 0.1 $\mu$m $BF_2$- and indium-implant DTMOS. $V_g$ varies from 0 to 0.7 V in 0.1 V steps.

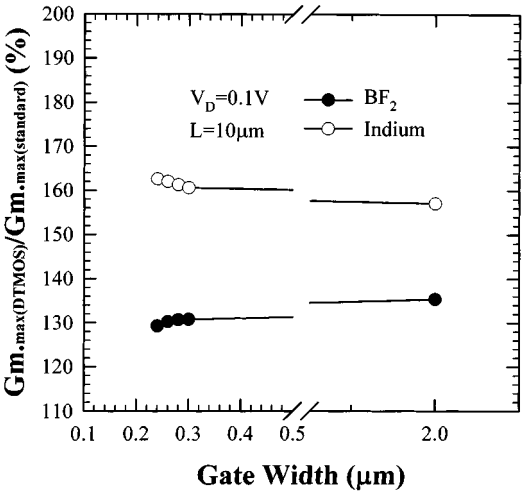


Fig. 3. Transconductance ratio versus gate width for $BF_2$- and indium-implant DTMOS.

more sensitive to body bias, i.e., it depicts a larger $\gamma$, for both wide and narrow transistors than $BF_2$-implanted control. This is primarily due to the steep indium dopant profile in the channel depletion layer, which has been confirmed from SIMS analyses (not shown). In addition, the $V_{\rm th}$ of indium-implanted device shows a less dependence on channel width compared to $BF_2$-implanted control. The reduced $\gamma$ value and $V_{\rm th}$ in the narrow channel devices for the $BF_2$-implanted control are believed to be due to the boron diffusion and segregation into the edge in the channel width direction [6]. In the insert of Fig. 1, we show the $V_{\rm th}$ as a function of body bias for a short channel (i.e., 0.13 $\mu$m) device. It is found that indium-implanted device indeed depicts a larger body effect, albeit its $V_{\rm th}$ is lower than that of $BF_2$-implanted control. Hence indium-implanted SSR channel profile depicts a unique attribute of fully exploiting the high current drive and low standby power features of DTMOS. It is worthy to note here that we have chosen an indium implant dose of $1 \times 10^{13}$ cm$^{-2}$, because it has been previously reported that the achievable body effect factor saturates at around this dose, with a corresponding doping concentration of no more than 7–8 $\times$ $10^{17}$ cm$^{-3}$ [7]. The subthreshold swing factors are plotted as a function of channel length $L_g$ in Fig. 2. It can be seen that the indium-implanted devices depict worse subthreshold swing than the $BF_2$-implanted counterparts under normal operation (i.e., non-DTMOS mode). This is because of a shallower channel depletion layer in the indium-implanted channel, resulting in a larger depletion capacitance and therefore a larger subthreshold swing. However, the subthreshold swing of the indium-implanted devices operating under DTMOS mode is significantly improved, and becomes even better than that of the $BF_2$-implanted controls operating under DTMOS mode (i.e., 15.6% reduction), due to a larger $\gamma$. Fig. 3 shows the plot of linear transconductance $(G_m)$ ratio $(G_{m_{\rm DTMOS}}/G_{m_{\rm Standard}})$ of DTMOS versus the coded channel width $W_{\rm coded}$. Compared to the $BF_2$-implanted counterpart, indium-DTMOS shows a higher $G_m$ ratio. The ratio of $BF_2$-implanted devices shows a 6% reduction when the $W_{\rm coded}$ reduces from 2 to 0.22 $\mu$m, while a 5.5% increase is found for indium-implanted devices. Fig. 4 shows the drain current vs. drain voltage characteristics for 0.1 $\mu$m Indium- and $BF_2$-implant devices. The linear $V_{\rm th}$ ($V_D = 0.1$ V) for indium- and $BF_2$-implant devices are 0.311 V and 0.328 V, respectively. Current driving capability of DTMOS and standard MOSFET's are compared. The drive current (measured under $V_D = V_G = 0.7$ V) of $BF_2$-implanted device is 1.3 times larger when operating under DTMOS mode than under normal operation (i.e., non-DTMOS mode). In contrast, the drive current of In-implanted device is 1.5 times larger when operating under DTMOS mode than under normal operation, again because of the larger body effect factor. So because of a smaller threshold voltage (under normal operation mode) and a larger dynamic threshold efficiency, the drain current as high as 300 $\mu$A/$\mu$m at $V_G = V_{\rm DD} = 0.7$ V is achieved for the indium-DTMOS. In short, indium-DTMOS devices show improved performance in terms of driving current, dynamic threshold property, subthreshold swing $(S), G_m$, compared to the conventional $BF_2$-DTMOS.

## IV. Conclusion

High performance DTMOS for low supply voltage (e.g., $V_{\rm DD} < 0.7$ V) applications has been realized by using super-steep-retrograde indium-channel-implantation. The indium-implanted DTMOS has a large dynamic threshold efficiency at low $V_{\rm th}$ due to its low surface concentration and steep substrate dopant distribution. The indium-DTMOS also shows a significant improvement in narrow channel devices as compared to $BF_2$ counterpart. The improved narrow channel characteristic is mainly attributed to less dopant diffusion and segregation into the isolation edge oxide. The indium-implanted devices thus fully exploit the advantages of DTMOS not only in short channel but also in narrow channel devices, as compared to conventional $BF_2$-DTMOS. It thus appears to be a very promising candidate for ultra-low voltage applications.

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