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Search of optimum bias voltage for oxide patterning on Si using scanning tunneling microscopy in air*

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Nanometer-scale oxide patterns were fabricated on H-passivated Si using a scanning tunneling microscopy (STM) in air. We found that the optimum bias voltage to generate clean and uniform oxide patterns depends on the composition of the tip material rather than on the tip head sharpness. For tungsten tips, oxide patterns with the desired geometrical features can be obtained at bias voltages ranging from -0.8 to -1.2 V, while for platinum–iridium tips, the bias voltages lie between -1.5 and -2.5 V at a fixed tunneling current of 2.0 nA. These biases correspond to the working voltage generating the oxide pattern with the lowest apparent depth. Beyond these voltage ranges, tip scratching on the sample surface or field-induced mass transfer from the tip might occur, as evidenced by tip wearing and the contamination of debris of tip material in the vicinity of the patterns. On the other hand, the tip head sharpness affects the width and the height of line patterns. When extremely fine oxide lines were desired, a sharp tip has to be used for STM patterning. [S0734-211X(00)08202-0]

I. INTRODUCTION

Nanometer-scale lithography has attracted a lot of interest as the sizes of integrated circuits (ICs) shrink. Among the various nanoscale fabrication techniques reported so far, lithography using scanning probe microscope (SPM) is one of the promising tools due to its advantages of being able to proximity focus and its low equipment cost. Many related studies have been reported since Dagata *et al.*[1] presented the modification of H-passivated Si(111) in air using scanning tunneling microscopy (STM). Similar work on Si and oxide strips 10–50 nm wide was performed.[2–8] In addition to STM, atomic force microscopy (AFM), associated with bias voltages, was also used to generate oxide patterns on Si (Refs. 9–15) as well as on metallic substrates such as Ti (Refs. 16–18) and Al.[19] Established processing techniques were used to fabricate nanoscale electronic devices, e.g., single electron transistors (SETs),[16] ultrafast photoconductive switches,[17] lateral tunneling function,[18] metal–oxide–semiconductor field effect transistors (MOSFETs),[20] side-gated FETs,[21] etc.

In this article we report the formation of oxide patterns on H-passivated Si using a STM under various bias voltage conditions. The effects of the composition of the tip material and the sharpness of the features of oxide patterns were also explored. We demonstrate that the composition of the tip material plays an important role in determining the optimum bias voltages to generate clean and uniform oxide patterns on Si. As to the tip head sharpness, it affects the linewidth and the height of oxide patterns. A sharp tip is required to generate oxide lines with finite linewidth and height.

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II. EXPERIMENT

Si(100) single crystalline wafers, 0.008–0.02 Ω cm, *n* type, were used as the substrates for our experiments. They were first cleaned by standard RCA procedures and dipped into a 10% HF solution for 60 s to attain hydrogen passivation. The Si substrate was then glued onto a disk-like sample holder by silver paste and transferred to a Digital Instruments' D3100 SPM that provides functions of both STM and AFM. Oxide patterning was carried out in air at a temperature of $\sim 25\,^{\circ}$C with a relative humidity (RH) of $\sim 60\%$. Square oxide patterns were formed at negative bias voltages relative to the sample with fixed tunneling current $I_t = 2.0$ nA in STM mode. Both W and PtIr tips were employed for patterning. The morphology of the oxide patterns was characterized by the SPM in AFM mode and by a field emission scanning electron microscope (FE-SEM) (Hitachi S-4000) equipped with an energy dispersive spectrometer (EDS).

III. RESULTS AND DISCUSSION

A. Effect of bias voltages

Figures 1(a) and 1(b) show the AFM and SEM images of 1 μm$\times$1 μm oxide patterns formed at bias voltages ranging from -0.4 to -2.0 V, respectively, using a W tip. The emergence of small perturbations at the edges of the patterns formed at low and high bias is observed. In order to identify these perturbations, we generated a 3 μm$\times$3 μm oxide pattern on Si at -2.5 V using a W tip. Figure 2(a) is the SEM image of such a pattern and corresponding W-element mapping using EDS is shown in Fig. 2(b). The exaggerated W signal shown in Fig. 2(b) reveals the existence of W agglom-

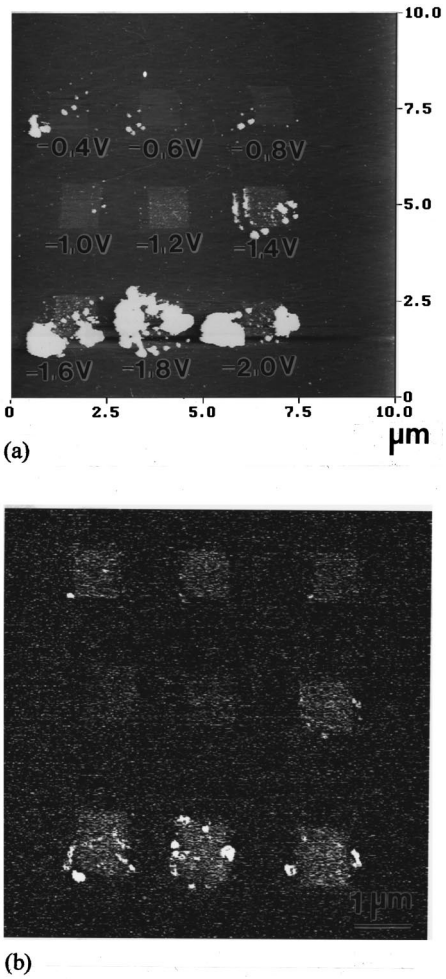

FIG. 1. (a) AFM and (b) SEM images of 1 μm$\times$1 μm oxide patterns formed at bias voltages ranging from -0.4 to -2.0 V using a W tip.

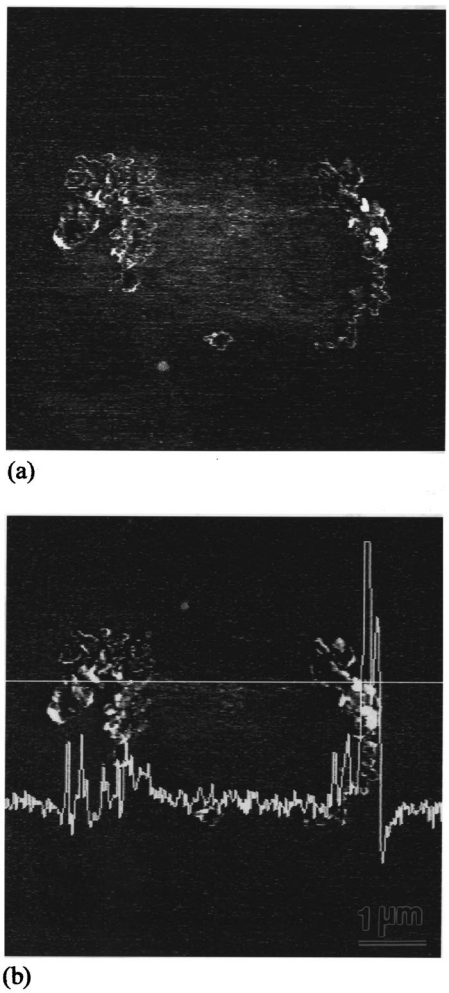

FIG. 2. (a) SEM image and (b) W-element mapping of a 3 μm$\times$3 μm oxide pattern on Si at -2.5 V using a W tip.

erates on the two vertical sides of the pattern. Since horizontal back-and-forth motion of the tip generates the oxide pattern, it implies that W tends to accumulate at the positions where the tip reverses its scanning direction. We also examined the tip by SEM before and after the STM patterning and the tip configurations are shown in Figs. 3(a) and 3(b). The obtuseness of the tip implies that it has become duller during patterning and validates the W perturbations depicted in Fig. 2. Since W contamination frequently occurrs in high bias voltage patterning, the field-induced mass transfer from the tip to Si is a possible cause of tip wearing. The W deposition at the edges of the oxide patterns was also attributed to the reverse motion of tip scanning. It might cause a sudden change in the highly concentrated electric field at the tip head and disrupt the constant tunneling current condition. The resulting tip height instability, hence, caused the tip to crash and left W debris on sample surface.

Although not as extensive as in the cases of high bias voltage patterning, debris of tip material was also observed in the patterns generated by low bias voltages. An example of this is given in Fig. 4 which depicts EDS maps of Pt and Ir elements of an oxide pattern generated at -0.1 V using the PtIr tip. When the bias voltage was low, the tip had to be brought close to the Si surface to achieve constant tunneling current. This raised the possibility of tip scratching of the sample surface and pattern contamination occurring.

We also recorded the apparent depth[1] of the square oxide patterns shown in Fig. 1 during STM imaging. The apparent depths of the patterns generated using W and PtIr tips as a function of bias voltage are shown schematically in Figs. 5(a) and 5(b), respectively. In Fig. 5, the U-shape curves indicate the lowest apparent depth at a particular bias voltage. At fixed tunneling current of 2 nA, the pattern generated by the W tip with voltage of -1.0 V has the lowest apparent depth, while for the pattern generated with the PtIr tip the lowest apparent depth occurs at -2.0 V.

The experimental results presented above reveal that at the bias condition generating the pattern with the lowest apparent depth, the contamination resulted from tip mass transfer and scratching on the sample surface could be minimized. One may adopt such a bias voltage to form a clean and uniform oxide pattern on Si. This finding also enables us to identify the optimum bias voltage for STM patterning.

We carried out -1.0 V bias voltage patterning with another W tip and this bias condition generated oxide patterns

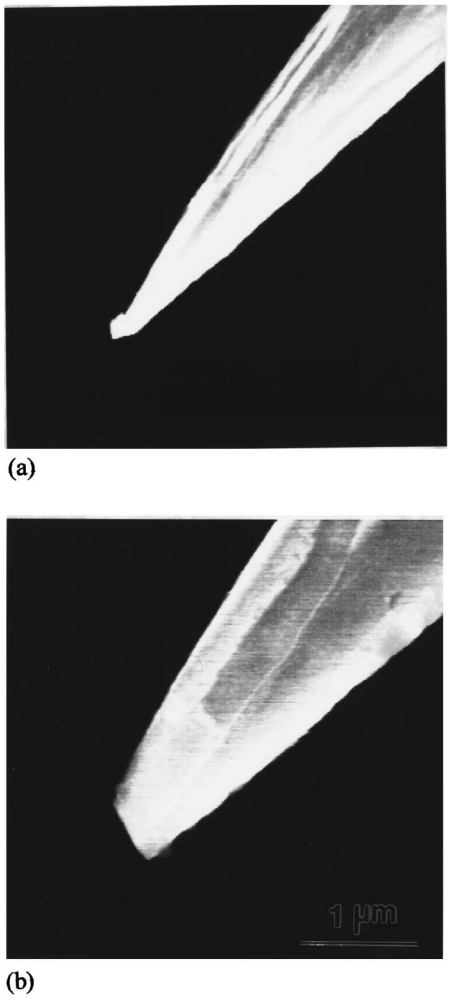

FIG. 3. Configuration of a W tip (a) before and (b) after patterning at bias voltage of −2.5 V.

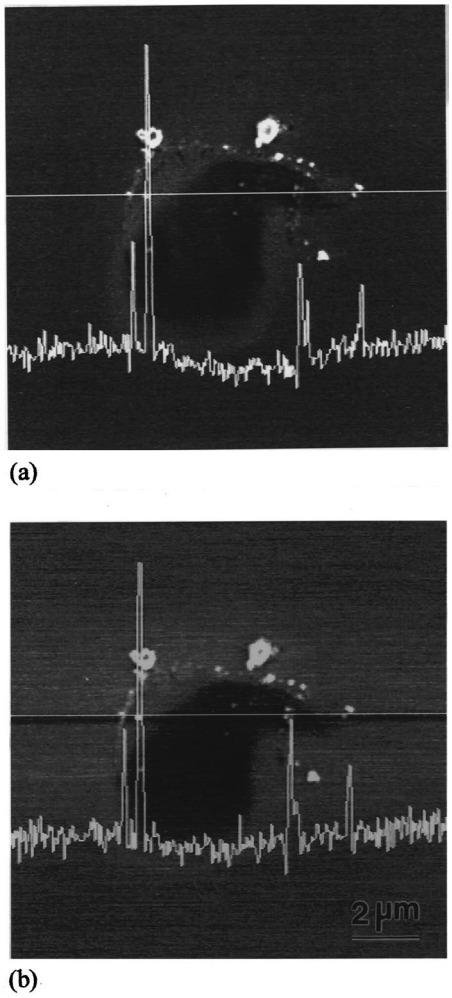

FIG. 4. EDS maps of (a) Pt and (b) Ir elements of an oxide pattern generated at −0.1 V using a PtIr tip.

with the desired morphology. After patterning the tip was immediately transferred to a SEM to examine its change in morphology and no tip wear and tear was observed. By repeating the STM patterning shown in Fig. 1 several times, we concluded that the optimum bias voltages for W tips to generate oxide patterns with satisfactory features ranged from −0.8 to −1.2 V at a fixed tunneling current of 2.0 nA. In addition to W tips, PtIr tips were also used for STM patterning. It was found that the optimum bias voltages for PtIr tips to generate clean and uniform oxide patterns ranged from −1.5 to −2.5 V at a fixed tunneling current of 2.0 nA.

W and PtIr tips with various degrees of sharpness were employed to perform STM patterning. By inspecting the morphology of the oxide patterns and all the W and PtIr tips before and after patterning, we found that the sharpness of the tip head has only a minor effect on the optimum bias voltage range.

B. Effect of tip sharpness

Our experiment revealed that the tip sharpness affected the width and height of the pattern when oxide lines formed. As shown in Figs. 6(a) and 6(b), the oxide lines are narrower in width when sharp tips are used. The average height of the pattern is also higher for those formed by a sharp tip. Therefore, the effect of the tip head geometry should not be ignored when extremely fine oxide line patterns of satisfactory quality are desired.

After writing, the SPM was immediately switched to AFM mode to examine the patterns. The heights of the oxide patterns formed by these W and PtIr tips were also measured. From the results shown in Fig. 7, it is clear that the W tips have better patterning efficiency. Our SEM characterization found that the W tips were in general sharper than the PtIr tips. Since the electric field strength was intensified by a decrease in the tip head radius, the W tips hence exhibited a better ability for oxide patterning. The result above is further supported by the theory of STM operation. The one-dimensional model of quantum tunneling predicts that the tunneling current I between two electrodes is related to the local work function ϕ by the expression[22]

$$I \propto \exp\left(-\sqrt{\frac{2m\phi}{\hbar^2}}d\right).$$

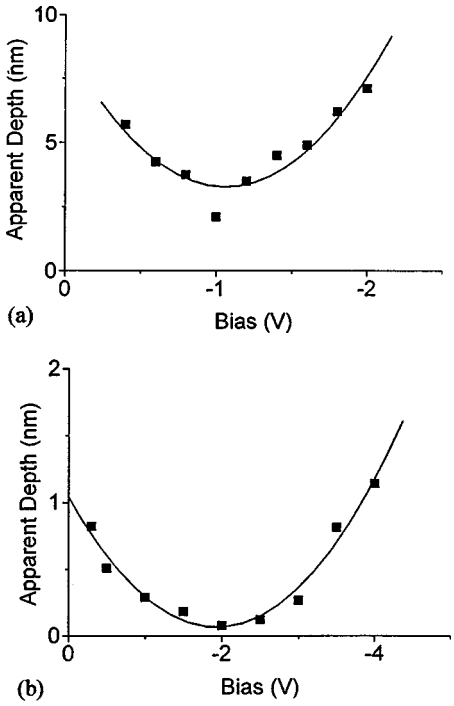

FIG. 5. Apparent depths of the patterns generated by (a) W and (b) PtIr tips as a function of bias voltage.

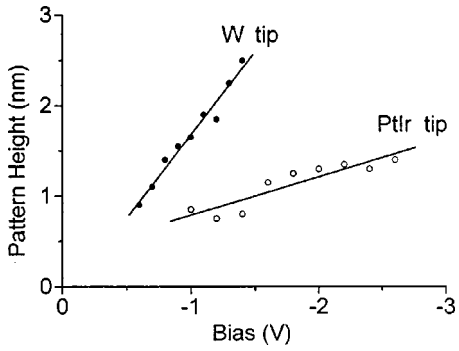

FIG. 7. Height of an oxide pattern generated by W and PtIr tips as a function of applied bias voltage.

Although the actual work function of the PtIr alloy is not known, our available data show that the work functions for W, Pt and Ir are 4.5, 5.29 and 4.57 eV,[23] respectively. With a work function value lower than that of Pt and Ir, the W tip may emit a higher tunneling current and hence provide better patterning efficiency.

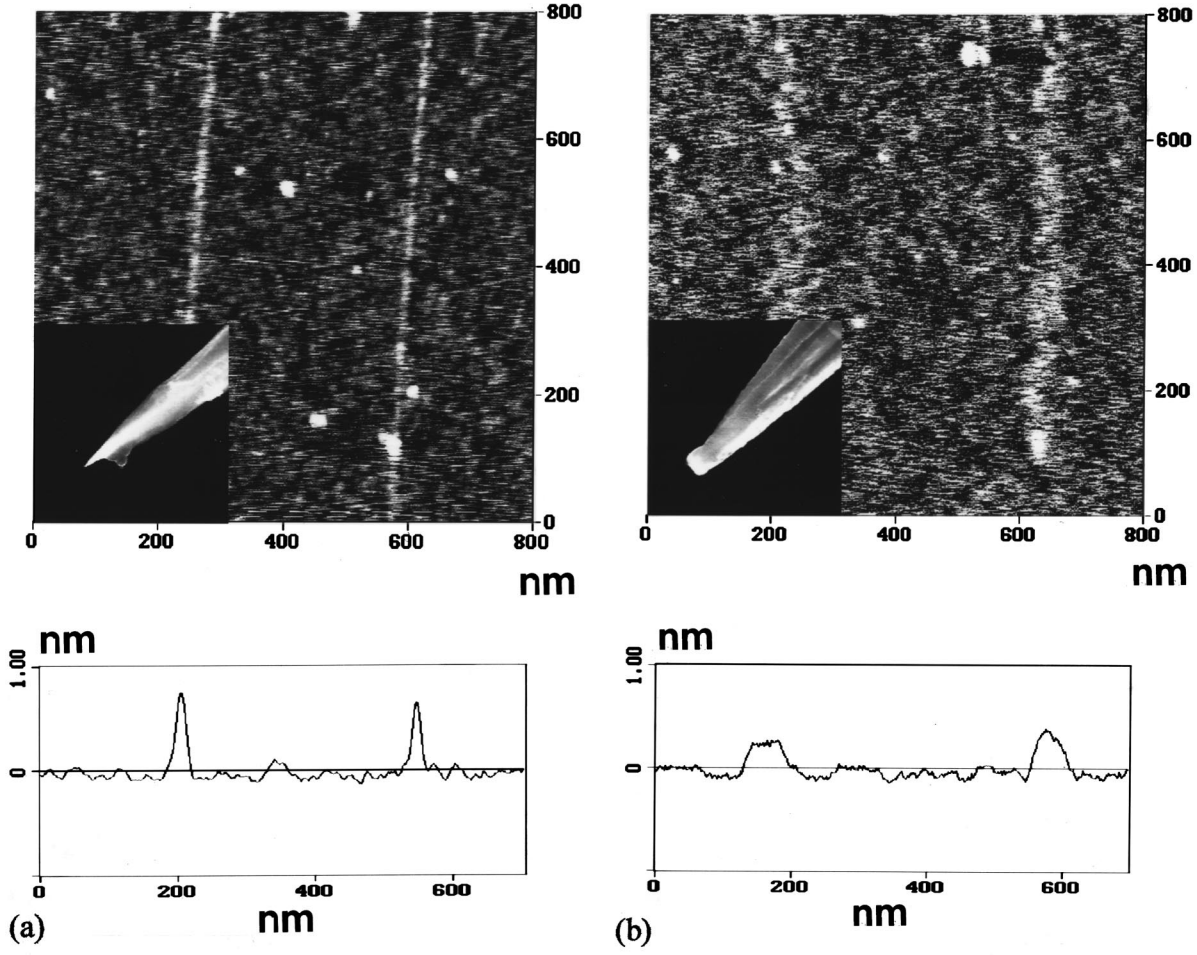

FIG. 6. Oxide lines and average height of a pattern generated by (a) a sharp tip and (b) a blunt tip. The pattern height was measured by AFM immediately after writing.

IV. CONCLUSIONS

In this article we reported the fabrication of oxide patterns on H-passivated Si by STM in air using W and PtIr tips. We found that the material that makes up the tip is an important factor that affects the optimum bias voltages for STM patterning. At a fixed tunneling current of 2.0 nA, the bias voltages lies between -0.8 and -1.2 V for W tips, whereas the bias voltages lie between -1.5 and -2.5 V for PtIr tips. When working under optimum bias conditions, oxide patterns with clean and uniform features can be obtained without wearing out the tip. Furthermore, the optimum bias voltage corresponds to the voltage generating the oxide pattern that has the lowest apparent depth. On the other hand, the sharpness of the tip affects the width and height of the oxide lines. Both the composition of the material and the geometry of the tip head are important parameters that affect nanofabrication in the SPM process.

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