Optimised integrated CMOS optical receiver for optical interconnects

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Indexing terms: Optical interconnects, CMOS optical receivers

Abstract: The optimisation of an optical receiver is discussed and transient charcteristics of two basic simple integrated receivers in CMOS systems are analysed and compared in detail. In analysis, a maximum current parameter is developed and used for optimisation design. Among these two receivers, the low-impedance configuration is presented for high-speed operation. SPICE simulation and preliminary experimental results with discrete devices are also illustrated and discussed.

1 Introduction

Since optical interconnects was suggested as a method to improve the performance of VLSI systems [1–11], many researchers have investigated its application in CMOS systems [12–18, 21]. Bergman *et al.* started to use a simple receiver with a saturation pMOS load to implement optical interconnects in a CMOS VLSI system [13, 15, 16]. However, the long switching fall time of this receiver significantly limited the operation speed of the system. Although the simulation evaluation for this receiver was reported and two other different receivers with two more devices were presented to improve the switching speed by Wu *et al.* [17], the detailed analysis of transient characteristics of these receivers were not discussed and the long-tail problem of the switching waveform was still not efficiently improved. One of these two receivers gave a long switching fall time, and the other gave a smaller output logic swing and consumed more power. Some improvements were presented by Chou *et al.* [18] although a detailed analysis and optimisation of this receiver design were not discussed. As will be shown, optimisation is necessary to achieve high-speed operation.

In addition to high speed and large output swing considerations, another important aspect for optical interconnects is to minimise optical receiver complexity for practical applications in compatible CMOS technologies. In this paper, we first discuss the basic integrated CMOS optical receiver, a very simple structure which only contains one photodetector and one biasing load device, and the concept for optimising this circuit. Two different configurations, a saturation load and a low-impedance load, are then discussed. The transient characteristics of these configurations are analysed and compared in detail. The low-impedance configuration is presented for high-speed optical interconnect applications and an optimised design is proposed. Analytical results and SPICE simulations for typical examples are also provided. Finally, preliminary experimental results with discrete devices are given and conclusions are summarised.

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2 Basic integrated CMOS optical receiver

The structure of a basic CMOS optical receiver without any gain stage is shown in Fig. 1. V_{DD} is the supply

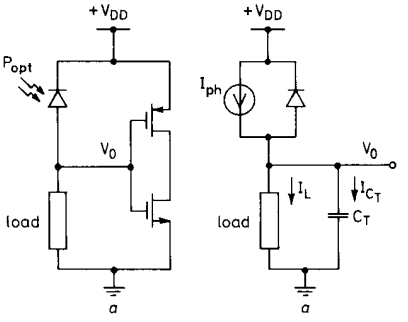

Fig. 1 *CMOS optical receiver*
a the basic structure
b the equivalent circuit

voltage, V_0 is the output voltage, C_T represents the total effective capacitance (which includes CMOS inverter input capacitance C_i, the detector capacitance C_{det} and the biasing load device output capacitance C_0), I_{ph} is the photocurrent of the detector during an illumination pulse, I_L is the load current, and I_{C_T} is the capacitor charging current. This structure only contains one photodetector and one biasing load device to provide a desired output logic swing. The rise and fall times, and output logic swing are functions of the type and the effective resistance of the biasing load. When a light pulse illuminates the detector, a photocurrent I_{ph} is generated and

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divided between I_L and I_{C_T}. Therefore, the capacitor charging current I_{C_T} becomes $I_{ph} - I_L$. A small load resistance with large I_L decreases I_{C_T}, and requires a long rise time to charge the capacitor to a desired voltage level. On the other hand, when the light is turned off, no photocurrent is generated and the load current I_L discharges the capacitor. A smaller load will have a higher discharging current $|I_{C_T}|$ and a shorter fall time. By suitably adjusting the effective load resistance, the average capacitor charging and discharging currents can be equalised, providing a symmetric signal waveform with equal rise and fall times. In this case, the total switching time, which is the sum of the rise and fall times, is minimised and the functional signal frequency is maximised [19].

In addition to the symmetric waveform, another consideration for a signal is a large output swing, which provides good noise immunity and fast switching response of the receiving inverter. If we use a linear passive resistor as the biasing load, to have a full logic swing, the resistance value is given by $R = V_{DD}/I_{ph}$. For a 40% efficient integrated detector with 0.5 mW optical input power at 780 nm wavelength, and a typical V_{DD} of 5 V, the photocurrent I_{ph} is 0.126 mA and the required resistance for a full-swing output is approximately 40 kΩ. In an integrated circuit, a resistor of this value requires a large fraction of the limited area and is not appropriate. We use an enhancement-mode nMOS transistor in a standard CMOS process as the biasing load to provide a nonlinear resistance characteristic. Using this device as the biasing load, the receiver has two different configurations: one is connecting the gate of this nMOS transistor to the drain output, i.e. $V_{GS} = V_{DS} = V_0$ (a similar structure has been used and briefly discussed in References 13, 15 and 16), and the other is connecting the gate to the most positive potential V_{DD}, i.e. $V_{GS} = V_{DD}$.

In the subsequent discussions, V_{0L} is defined as the low steady-state output voltage and V_{0H} as the high steady-state out-put voltage. To analyse the transient characteristics of these circuits, a maximum-current parameter m is defined as the ratio of the photocurrent I_{ph} to the maximum transistor current $I_{DS}(V_{GS} = V_{DD})$, which is

$$m \equiv \frac{I_{ph}}{I_{DS}(V_{GS} = V_{DD})} \tag{1}$$

where $I_{DS}(V_{GS} = V_{DD})$ is the drain saturation current for a gate bias of V_{DD} and the maximum current of this transistor (neglecting small geometry effects), which is given by

$$I_{DS}(V_{GS} = V_{DD}) = k\frac{(V_{DD} - V_T)^2}{2} \tag{2}$$

where k is the transconductance parameter and V_T is the threshold voltage. A normalisation time, T, is defined as

$$T \equiv \frac{V_{DD}}{I_{ph}} C_T \tag{3}$$

3 Transient analysis and optimal design

3.1 Saturation CMOS optical receiver ($V_{GS} = V_{DS}$)

The equivalent circuit of the first configuration mentioned above is shown in Fig. 2, where V_{DS}, V_{GS}, and I_D are the drain bias, gate bias, and drain current of the nMOS load transistor, respectively. For this configuration $V_{GS} = V_{DS} = V_0$ and the drain saturation voltage is given by $V_{DSS} = V_{GS} - V_T = V_{DS} - V_T$. With an enhancement-mode nMOS transistor ($V_T > 0$), $V_{DS} > V_{DSS}$, therefore the transistor operates in the saturation region when $V_0 > V_T$, and the drain current is given by

$$I_D = I_{DS} = k\frac{(V_{GS} - V_T)^2}{2} = k\frac{(V_0 - V_T)^2}{2} \tag{4}$$

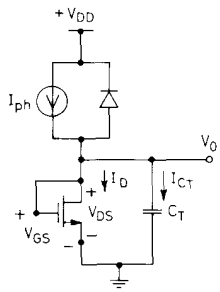

Fig. 2 *Saturation CMOS optical receiver ($V_{GS} = V_{DS}$)*

where I_{DS} is the drain saturation current of the nMOS load transistor. The output capacitance of the transistor includes the gate-substrate capacitance (C_{gs}) and drain-substrate capacitance (C_{ds}). Typical current–voltage characteristics of this saturation structure are shown in Fig. 3.

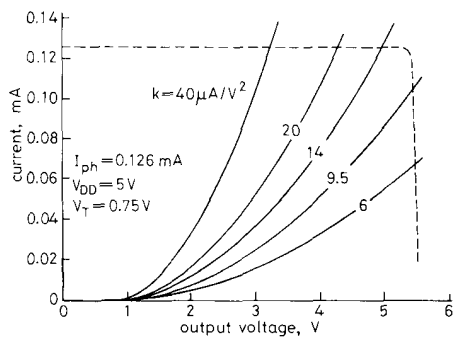

Fig. 3 *SPICE simulation I–V characteristics of a saturation receiver for different bias conditions*

When the light is off, V_{0L} is V_T, since the output cannot be discharged to a value lower than the threshold voltage. When the light is on, I_{ph} is generated and V_{oH} is determined by the value of m, which will be discussed below.

3.1.1 $m \leqslant 1$, i.e. $I_{ph} \leqslant I_{DS}$: In this case,

$$I_{ph} = I_{DS}(V_{GS} = V_{0H}) = \frac{k(V_{0H} - V_T)^2}{2} \tag{5}$$

and

$$V_{0H} = V_T + \sqrt{\left(\frac{2I_{ph}}{k}\right)} = V_T + \sqrt{(m)}(V_{DD} - V_T) \leqslant V_{DD} \tag{6}$$

The rise time t_r for V_0 to change from V_T to $V_T + 0.9(V_{0H} - V_T)$ and the fall time for V_0 to drop from V_{0H} to $V_T + 0.1(V_{0H} - V_T)$, solved in Appendix 8.1.1, are given by

$$t_r = \frac{\sqrt{(m)}}{2}\left(1 - \frac{V_T}{V_{DD}}\right)T \ln 19 \tag{7a}$$

and

$$t_f = 9\sqrt{(m)}\left(1 - \frac{V_T}{V_{DD}}\right)T \tag{7b}$$

3.1.2 $m > 1$, i.e. $I_{ph} > I_{DS}$: In this case, $V_{0H} \simeq V_{DD}$. The rise time t_r for V_0 to change from V_T to $V_T + 0.9(V_{DD} - V_T)$ and the fall time for V_0 to drop from V_{DD} to $V_T + 0.1(V_{DD} - V_T)$, solved in Appendix 8.1.2, are given by

$$t_r = \frac{\sqrt{(m)}}{2}\left(1 - \frac{V_T}{V_{DD}}\right)T \ln\left[\frac{\sqrt{(m)} + 0.9}{\sqrt{(m)} - 0.9}\right] \tag{8a}$$

and

$$t_f = 9m\left(1 - \frac{V_T}{V_{DD}}\right)T \tag{8b}$$

Using $T \equiv (V_{DD}/I_{ph})C_T$ as the normalisation time, normalised t_r and t_f are only functions of V_T/V_{DD} and m. Due to the parabolic form of the transistor current in eqn. 8, the average discharging current at OFF state is much smaller than the average charging current at ON state, therefore the rise and fall times can not be equalised, and the fall time is much longer than the rise time, which can be seen from eqns. 7 and 8.

In summary, there are three disadvantages of the saturation load CMOS receiver:

(i) the output offset voltage of the OFF state is V_T

(ii) the output capacitance of the biasing transistor ($C_0 = C_{gs} + C_{ds}$) is much larger than the other configuration to be considered

(iii) the switching waveform has a long tail with a slow falling response which limits high-speed performance.

3.2 Low-impedance CMOS optical receiver ($V_{GS} = V_{DD}$)

The equivalent circuit of a low-impedance CMOS receiver is shown in Fig. 4. In this configuration $V_{GS} =$

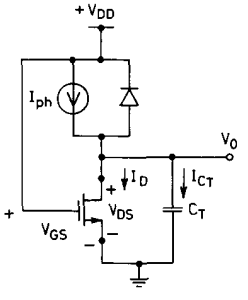

Fig. 4 *Low-impedance CMOS optical receiver ($V_{GS} = V_{DD}$)*

V_{DD} and $V_0 = V_{DS}$ which biases the gate to the most positive potential, and produces a low effective channel resistance. The drain saturation voltage V_{DSS} is therefore equal to $V_{DSS} = V_{DD} - V_T$. The output capacitance of the biasing transistor only includes the drain-substrate capacitance (C_{ds}), which is negligible compared with the gate-substrate capacitance (C_{gs}) [20]. Typical current–voltage characteristics of this low-impedance structure are shown in Fig. 5.

When the light is off, V_{0L} is 0 V. When the light is on, I_{ph} is generated and V_{0H} is determined by the value of m, which will be discussed below.

3.2.1 $m \leqslant 1$, i.e. $I_{ph} \leqslant I_{DS}$: In this case, the transistor operates in the triode region with a drain current I_D given by

$$I_D = k\left(V_{DSS}V_{DS} - \frac{V_{DS}^2}{2}\right) = k\left(V_{DSS}V_0 - \frac{V_0^2}{2}\right) \tag{9}$$

V_{0H} is determined from the photocurrent

$$I_{ph} = I_D(V_0 = V_{0H}) = k\left(V_{DSS}V_{0H} - \frac{V_{0H}^2}{2}\right) \tag{10}$$

which can be rearranged to have

$$V_{0H} = V_{DSS} - \sqrt{\left(V_{DSS}^2 - \frac{2I_{ph}}{k}\right)}$$
$$= [1 - \sqrt{(1 - m)}]V_{DSS} \leqslant V_{DSS} \tag{11}$$

The rise time t_r for V_0 to change from 0 V to $0.9V_{0H}$ and

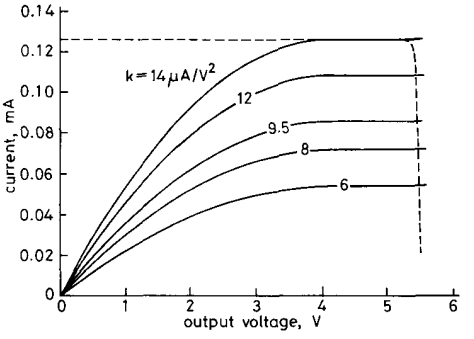

Fig. 5 *SPICE simulation I–V characteristics of a load-impedance receiver for different bias conditions*

the fall time t_f for V_0 to drop from V_{0H} to $0.1V_{0H}$, solved in Appendix 8.2.1, are given by

$$t_r = \frac{m}{2\sqrt{(1 - m)}}\left(1 - \frac{V_T}{V_{DD}}\right)T \ln\left[\frac{1 + 19\sqrt{(1 - m)}}{1 + \sqrt{(1 - m)}}\right] \quad \text{for } m < 1 \tag{12a}$$

or

$$= 9\left(1 - \frac{V_T}{V_{DD}}\right)T \quad \text{for } m = 1 \tag{12b}$$

and

$$t_f = \frac{m}{2}\left(1 - \frac{V_T}{V_{DD}}\right)T \ln\left[\frac{19 + \sqrt{(1 - m)}}{1 + \sqrt{(1 - m)}}\right] \tag{12c}$$

3.2.2 $m > 1$, i.e. $I_{ph} > I_{DS}$: In this case, $V_{0H} \simeq V_{DD}$. The rise time t_r for V_0 to change from 0 V to $0.9V_{DD}$ and the fall time t_f for V_0 to drop from V_{DD} to $0.1V_{DD}$, solved in Appendix 8.2.2, are given by

$$t_r = \left\{\frac{0.9}{m - 1} + \left[\frac{1}{\sqrt{(m - 1)}}\tan^{-1}\left[\frac{1}{\sqrt{(m - 1)}}\right] - \frac{1}{m - 1}\right] \times \left(1 - \frac{V_T}{V_{DD}}\right)\right\}mT \tag{13a}$$

and

$$t_f = \left\{\frac{V_T}{V_{DD}} + \frac{1}{2}\left(1 - \frac{V_T}{V_{DD}}\right)\ln\left[19 - 20\,\frac{V_T}{V_{DD}}\right]\right\}mT \tag{13b}$$

Similar to the first configuration, normalised t_r and t_f are only functions of V_T/V_{DD} and m. To have a full output logic swing, m must be greater than 1. The optimisation

condition of equalising t_r and t_f gives the following relation

$$\frac{0.9}{m-1}-\frac{V_T}{V_{DD}}+\left\{\frac{1}{\sqrt{(m-1)}}\tan^{-1}\left[\frac{1}{\sqrt{(m-1)}}\right]-\frac{1}{m-1}-\frac{1}{2}\ln\left[19-20\frac{V_T}{V_{DD}}\right]\right\}\left(1-\frac{V_T}{V_{DD}}\right)=0 \quad (14)$$

When V_T/V_{DD} is given, the optimised m can be obtained from eqn. 14.

In an available CMOS process, the threshold voltage V_T and the minimum feature-size transconductance parameter k_0 of the biasing transistor are fixed. Therefore, an optimised m can be obtained for an operation V_{DD}, and the corresponding gate aspect ratio (W/L) for a specific I_{ph} can be designed to achieve this desired m value from the following relation

$$I_{DS}=k_0\left(\frac{W}{L}\right)\frac{(V_{DD}-V_T)^2}{2}=\frac{I_{ph}}{m} \quad (15)$$

where W and L are the gate width and channel length of the biasing transistor, respectively.

4 Analytical, SPICE simulation results and design examples

For given illumination and bias conditions, the output voltage and the switching times can be calculated from analytical results in Section 3. Using the supply voltage V_{DD} as the normalisation voltage, the normalised high state voltage (V_{0H}/V_{DD}) is only function of the maximum current parameter m defined by eqn. 3, and is shown in Fig. 6 for $m \leqslant 1 (V_{0H} \simeq V_{DD}$ for $m > 1)$. Using $T \equiv V_{DD}C_T/I_{ph}$ in eqn. 7 as the normalisation time, normalised rise and fall times are only functions of the normalised threshold voltage (V_T/V_{DD}) and the maximum current parameter m, and are shown in Fig. 7 with a typical value of 0.15 for V_T/V_{DD}. The results show that the fall time of a saturation configuration is always much longer than the rise time and the photocurrent is not efficiently utilised. For the low-impedance configuration, the rise and fall times can be equalised, which maximises the functional clock frequency. Making comparison of the normalised switching times between two configurations shown in Fig. 7, and also taking into account the additional output capacitance of the first configuration, the optimised low-impedance receiver has at least one order higher switching speed.

We used SPICE to simulate our circuits and the results were in good agreement with our analysis. Figs. 8 and 9 show SPICE simulation examples of transient response for our saturation and low-impedance receivers

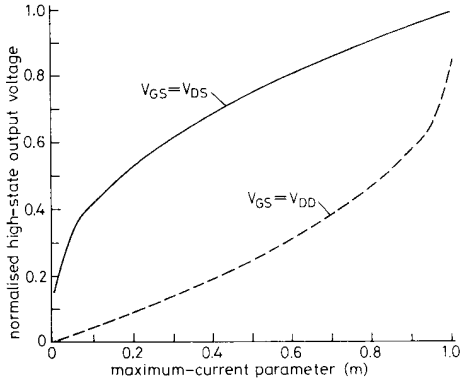

Fig. 6 *Analytic normalised high steady-state output voltages for $I_{ph} \leqslant I_{DS}$, i.e. $m \leqslant 1$*

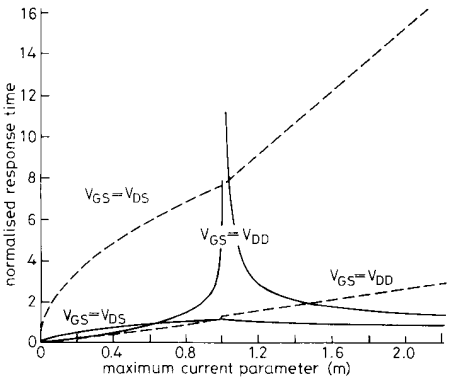

Fig. 7 *Analytic normalised response times for different bias conditions*

rise time
fall time

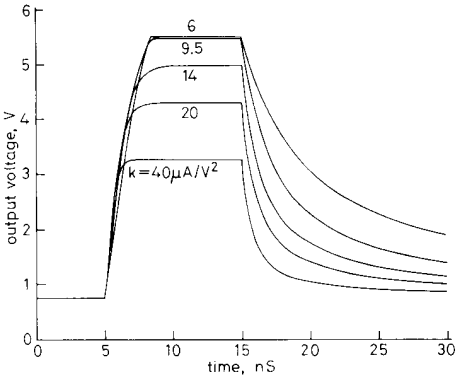

Fig. 8 *SPICE simulation switching response of a saturation receiver for different bias conditions*

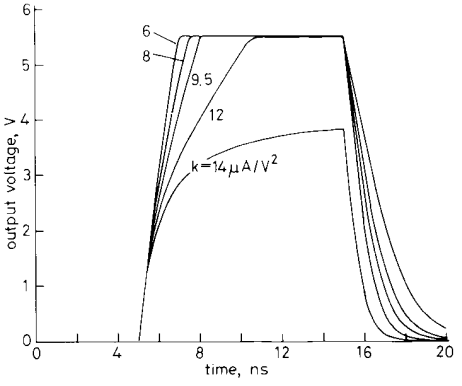

Fig. 9 *SPICE simulation switching response of a low-impedance receiver for different bias conditions*

with a typical 2 μm CMOS process: $V_{DD} = 5$ V, $V_T = 0.15V_{DD}$, $k_0 = 56\ \mu A/V^2$, $C_i = 16.6$ fF, $C_{gs} = 4.16$ fF, $C_{ds} = 0.80$ fF, and C_{det} is $0.025\ fF/\mu m^2$ (with $2 \times 10^{14}\ cm^{-3}$ epilayer doping concentration) [20] and 12.3 fF for a detector with 25 μm diameter. The detector efficiency η_{det} can be expressed by

$$\eta_{det} = 1 - \exp(-\alpha d) \tag{16}$$

and is about 40% in our example, where $1/\alpha$ is the light penetration depth, which is 10 μm in silicon material for a 780 nm wavelength, and d is the junction depletion depth. For a 0.5 mW optical input power at 780 nm wavelength, the photocurrent I_{ph} is 0.126 mA. Corresponding parameter values are listed in Table 1. Fig. 8 shows that the logic swing of a saturation configuration is reduced by V_T in the OFF state, and that the fall time is very long as discussed in Section 3.1. Fig. 9 shows that the rise and fall times of a low impedance configuration can be equalised, and the switching speed is one order of magnitude higher than a saturation configuration for full-swing output.

As indicated the low-impedance receiver is more suitable for high-speed operation. Since the optimised m and the corresponding normalised time ($\tau = t_r = t_f$) of this configuration are only functions of V_T/V_{DD} (eqns. 13 and 14), we illustrate their relationships in Fig. 10 to provide

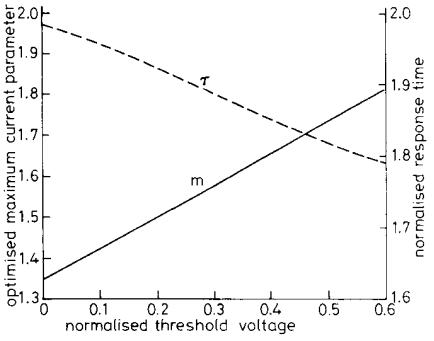

Fig. 10 *Optimised maximum-current parameter m values and corresponding normalised response times of a low-impedance receiver for different normalised threshold voltages*

design information. In our SPICE simulation example with $V_T/V_{DD} = 0.15$, the optimised m is 1.46 and the response time τ is $1.94T$, which is 2.3 ns ($V_{DD} = 5$ V, $I_{ph} = 0.126$ mA, $C_T = 29.7$ fF, and $T \equiv V_{DD}C_T/I_{ph}$), and also seen in Fig. 9 by SPICE simulation. These results show that this optimised simple low-impedance configuration can provide high-speed operation with a reasonable optical input power ($P_{op} = 0.5$ mW). Table 1 shows that a transistor with 2 μm gate width and 11.8 μm channel length provides this optimised biasing condition.

5 Preliminary experimental results

Optical receivers were implemented with discrete components to evaluate circuit characteristics. The threshold voltage V_T of the biasing transistor was 0.6 V. The supply voltage V_{DD} was set at 4 V to give a value of $V_T/V_{DD} = 0.15$ corresponding to the example in the previous discussions. A typical switching response of a saturation CMOS optical receiver is shown in Fig. 11. The low state

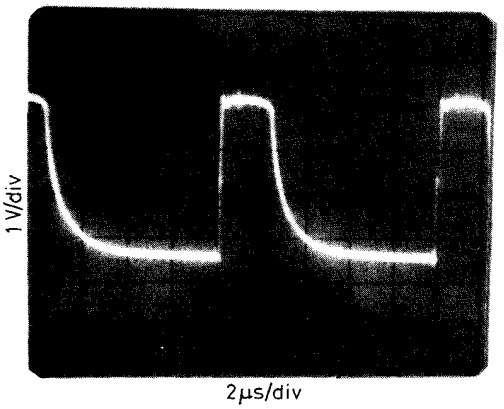

Fig. 11 *Experimental result of a saturation CMOS optical receiver*

is V_T, which reduces the output logic swing by V_T, and the switching waveform has a long tail with a long fall time of 4 μs as discussed in previous analytical results. Fig. 12 shows the switching response of an optimised low-impedance CMOS optical receiver. The result shows that the rise and fall times are equalised, and the photo-

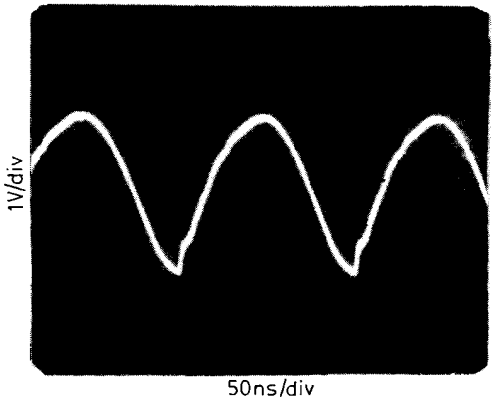

Fig. 12 *Experimental result of a low-impedance CMOS optical receiver*

Table 1: Corresponding parameter values for different m

k, $\mu A/V^2$	6.00	8.00	9.50	12.0	14.0	20.0	40.0
m	2.33	1.74	1.46	1.16	0.997	0.698	0.349
W/L	0.107	0.143	0.170	0.214	0.250	0.357	0.714
L, μm	18.7	14.0	11.8	9.3	8.0	5.6	2.8
C_{gs}, fF	38.8	29.1	24.5	18.7	16.6	11.6	5.8
C_{ds}, fF	0.8	0.8	0.8	0.8	0.8	0.8	0.8
C_O, fF ($V_{GS} = V_{DS}$)	39.6	29.9	25.3	19.5	17.4	12.4	6.6
C_T, fF ($V_{GS} = V_{DS}$)	68.5	58.8	54.2	48.4	46.3	41.3	35.5
C_O, fF ($V_{GS} = V_{DD}$)	0.8	0.8	0.8	0.8	0.8	0.8	0.8
C_T, fF ($V_{GS} = V_{DD}$)	29.7	29.7	29.7	29.7	29.7	29.7	29.7

$W = 2$ μm, $k_0 = 56\ \mu A/V^2$, $V_{DD} = 5$ V, $V_T = 0.75$ V, $I_{ph} = 0.126$ mA; $C_{gs} = 1.04\ fF/\mu m^2$, $C_{ds} = 0.20\ fF/\mu m^2$, $C_i = 16.6$ fF, $C_{det} = 12.3$ fF

current is efficiently utilised. The total effective capacitance C_T of this example is about 45 pF, the photocurrent I_{ph} is 6 mA, and the response time (t_r and t_f) is 75 ns, which shows much faster switching speed than the saturation configuration shown in Fig. 11. Since the response time is proportional to $V_{DD}C_T/I_{ph}$, projecting these experimental results to an integrated receiver with a capacitance of 29.7 fF and a photocurrent of 0.126 mA as used in the analysis of Section 4, the response time is about 2.4 ns, which is close to the analytical result. This result shows that the optimised integrated low-impedance receiver can operate at high rates with a reasonable optical input power ($P_{op} = 0.5$ mW) [21].

6 Conclusions

In order to efficiently apply optical interconnects in an electronic computing system, a simplified optical receiver must be used. In a CMOS process, saturation and low-impedance configurations are two basic integrated optical receivers without any gain stage. The transient characteristics of these two receivers have been discussed in detail. A design parameter, maximum current parameter m, which describes the relation between the photocurrent of the detector and the maximum current of the biasing device was developed for analysis and design. The low-impedance receiver was presented for high-speed operation. This receiver when optimised provides a symmetrical switching waveform with a full logic output voltage swing and efficiently utilities the available photocurrent. This optimised receiver can operate at high-speed with a practical optical input powers ($\tau = 2.3$ ns with $P_{op} = 0.5$ mW for 2 μm feature size). Preliminary experiments were performed with discrete devices and projected to integrated receivers by scaling capacitance values. The results verified the analytical and SPICE simulation predictions.

7 References

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8 Appendix

8.1 Transient analysis of a saturation CMOS optical receiver ($V_{GS} = V_{DS} = V_O$)

The circuit is shown in Fig. 2, and all parameters are defined in Sections 2 and 3. For this configuration, $V_{0L} = V_T$, and $V_{0H} = V_T + \sqrt{(m)}(V_{DD} - V_T) \leqslant V_{DD}$ for $m \leqslant 1$ or $V_{0H} \simeq V_{DD}$ for $m > 1$ as discussed in Section 3.1.

8.1.1 $m \leqslant 1$ ($I_{ph} \leqslant I_{DS}$):

(i) *Rise time:* Suppose the light pulse is turned on at the time $t = 0$, and the initial output state $V_0(0)$ is $V_{0L} = V_T$, then the relation between the output voltage $V_0(t)$ and the time t can be obtained from the following derivation

$$I_{C_T}(t) = C_T \frac{dV_0(t)}{dt} = I_{ph} - I_D(t)$$

$$= I_{ph} - k\frac{[V_0(t) - V_T]^2}{2} \tag{17}$$

$$t = \int_0^t dt' = \int_{V_T}^{V_0(t)} \frac{C_T\, dV_0(t')}{I_{ph} - k[V_0(t') - V_T]^2/2}$$

$$= \frac{\sqrt{(m)}}{2}\left(1 - \frac{V_T}{V_{DD}}\right)T \times \ln\left[\frac{\sqrt{(m)}(V_{DD} - V_T) + (V_0(t) - V_T)}{\sqrt{(m)}(V_{DD} - V_T) - (V_0(t) - V_T)}\right] \tag{18a}$$

and

$$V_0(t) = V_T + \sqrt{(m)}(V_{DD} - V_T) \times \left\{\frac{1 - \exp\left[-\dfrac{2t}{\sqrt{(m)}(1 - V_T/V_{DD})T}\right]}{1 + \exp\left[-\dfrac{2t}{\sqrt{(m)}(1 - V_T/V_{DD})T}\right]}\right\} \tag{19a}$$

where m and T are defined by eqns. 1 and 3 in Section 2, respectively. Therefore, the rise time t_r required to charge

$V_0(t)$ from V_T to $V_T + 0.9(V_{0H} - V_T)$ can be solved from eqn. 18*a* and is given by

$$t_r = \frac{\sqrt{(m)}}{2}\left(1 - \frac{V_T}{V_{DD}}\right)T \ln 19 \tag{20a}$$

where $V_{0H} = V_T + \sqrt{(m)}(V_{DD} - V_T)$.

(ii) *Fall time:* Suppose the light pulse is turned off at the time $t = 0$, and the initial output state $V_0(0)$ is V_{0H}, then the relation between the output voltage $V_0(t)$ and the time t can be obtained from a derivation similar to case (i) with $I_{ph} = 0$

$$t = \int_0^t dt' = \int_{V_{0H}}^{V_0(t)} \frac{C_T\, dV_0(t')}{-k[V_0(t') - V_T]^2/2}$$

$$= \sqrt{(m)}\left(1 - \frac{V_T}{V_{DD}}\right)T\left[\frac{\sqrt{(m)}(V_{DD} - V_T)}{V_0(t) - V_T} - 1\right] \tag{18b}$$

and

$$V_0(t) = V_T + \frac{V_{0H} - V_T}{1 + \dfrac{k(V_{0H} - V_T)}{2C_T}\, t}$$

$$= V_T + \frac{\sqrt{(m)}(V_{DD} - V_T)}{1 + \dfrac{t}{\sqrt{(m)}(1 - V_T/V_{DD})T}} \tag{19b}$$

Therefore, the fall time t_f for $V_0(t)$ to drop from V_{0H} to $V_T + 0.1(V_{0H} - V_T)$ can be solved from Eq. 18*b* and is given by

$$t_f = 9\sqrt{(m)}\left(1 - \frac{V_T}{V_{DD}}\right)T \tag{20b}$$

where $V_{0H} = V_T + \sqrt{(m)}(V_{DD} - V_T)$.

8.1.2 $m > 1$ ($I_{ph} > I_{DS}$): The relation between the output voltage and the rise or fall time is similar to the case for $m \leqslant 1$ in Section 9.1.1 except that $V_{0H} \simeq V_{DD}$.

(i) *Rise time:* The rise time t_r for $V_0(t)$ to charge from V_T to $V_T + 0.9(V_{DD} - V_T)$ can be solved from eqn. 18*a* with $V_0(t)$ given by V_{DD}, and is

$$t_r = \frac{\sqrt{(m)}}{2}\left(1 - \frac{V_T}{V_{DD}}\right)T \ln\left[\frac{\sqrt{(m)} + 0.9}{\sqrt{(m)} - 0.9}\right] \tag{21a}$$

(ii) *Fall time:* Substituting $V_0(0) = V_{0H}$ to eqns. 18*b* and 19*b* in Section 9.1.1 with $V_0(0) = V_{DD}$ yields

$$t = m\left(1 - \frac{V_T}{V_{DD}}\right)T\left[\frac{V_{DD} - V_T}{V_0(t) - V_T} - 1\right] \tag{22}$$

and

$$V_0(t) = V_T + \frac{V_{DD} - V_T}{1 + \dfrac{k(V_{DD} - V_T)}{2C_T}\, t}$$

$$= V_T + \frac{V_{DD} - V_T}{1 + \dfrac{t}{m(1 - V_T/V_{DD})T}} \tag{23}$$

Therefore, the fall time t_f for $V_0(t)$ to drop from V_{DD} to $V_T + 0.1(V_{DD} - V_T)$ can be solved from eqn. 22, and is

$$t_f = 9m\left(1 - \frac{V_T}{V_{DD}}\right)T \tag{21b}$$

8.2 Transient analysis of a low-impedance CMOS optical receiver ($V_{GS} = V_{DD}$, $V_{DS} = V_0$)

The circuit is shown in Fig. 4, and all parameters are defined in Sections 2 and 3. For this configuration, $V_{0L} = 0$ V, and $V_{0H} = [1 - \sqrt{(1 - m)}]V_{DSS} \leqslant V_{DSS}$ for $m \leqslant 1$ or $V_{0H} \simeq V_{DD}$ for $m > 1$ as discussed in Section 3.2. The drain saturation voltage is $V_{DSS} = V_{GS} - V_T = V_{DD} - V_T$, and the drain saturation current is $I_{DS} = kV_{DSS}^2/2$.

9.2.1 $m \leqslant 1$ ($I_{ph} \leqslant I_{DS}$): In this case, since $V_{0H} \leqslant V_{DSS}$, the transistor operates in the triode region, and the drain current is

$$I_D(t) = k\left[V_{DSS}V_0(t) - \frac{V_0^2(t)}{2}\right] \tag{24}$$

(i) *Rise time:* Suppose the light pulse is turned on at the time $t = 0$, and the initial output state $V_0(0)$ is $V_{0L} = 0$ V, then the relation between the output voltage $V_0(t)$ and the time t can be obtained from the following derivation

$$I_{C_T}(t) = C_T\frac{dV_0(t)}{dt} = I_{ph} - I_D(t)$$

$$= k\left[V_{DSS}\,V_0(t) - \frac{V_0^2(t)}{2}\right] \tag{25}$$

$$t = \int_0^t dt' = \int_{V_{0(0)}}^{V_0(t)} \frac{C_T\, dV_0(t')}{I_{ph} - k[V_{DSS}\,V_0(t') - V_0^2(t')/2]}$$

$$= \frac{C_T}{k/2}\int_{0\,V}^{V_0(t)} \frac{dV_0(t')}{[V_{DSS} - V_0(t')]^2 - (V_{DSS}^2 - 2I_{ph}/k)} \tag{26}$$

When $m < 1$, i.e. $I_{ph} < I_{DS}$, eqn. 26 becomes

$$t = \frac{m}{2\sqrt{(1 - m)}}\left(1 - \frac{V_T}{V_{DD}}\right)T$$

$$\times \ln\left\{\frac{[1 - \sqrt{(1 - m)}][1 - V_0(t)/V_{DSS} + \sqrt{(1 - m)}]}{[1 + \sqrt{(1 - m)}][1 - V_0(t)/V_{DSS} - \sqrt{(1 - m)}]}\right\} \tag{27a}$$

and the output is

$$V_0(t) = \frac{\left\{1 - \exp\left[-\dfrac{2\sqrt{(1 - m)}t}{m(1 - V_T/V_{DD})T}\right]\right\}mV_{DSS}}{[1 + \sqrt{(1 - m)}] - [1 - \sqrt{(1 - m)}]}$$

$$\times \exp\left[-\frac{2\sqrt{(1 - m)}t}{m(1 - V_T/V_{DD})T}\right] \tag{28a}$$

Therefore, the rise time t_r for $V_0(t)$ to charge from 0 V to $0.9V_{0H}$ can be solved from eqn. 27*a*, and is

$$t_r = \frac{m}{2\sqrt{(1 - m)}}\left(1 - \frac{V_T}{V_{DD}}\right)T \ln\left[\frac{1 + 19\sqrt{(1 - m)}}{1 + \sqrt{(1 - m)}}\right] \tag{29a}$$

When $m = 1$, i.e. $I_{ph} = I_{DS}$, $V_{0H} = V_{DSS}$, eqn. 26 becomes

$$t = \left(1 - \frac{V_T}{V_{DD}}\right)T\left[\frac{1}{1 - V_0(t)/V_{DSS}} - 1\right] \tag{27b}$$

and the output is

$$V_0(t) = V_{DSS}\left[1 - \frac{1}{1 + t/(1 - V_T/V_{DD})T}\right] \tag{28b}$$

Therefore, the rise time t_r for $V_0(t)$ to charge from 0 V to $0.9V_{DSS}$ can be solved from eqn. 27*b*, and is

$$t_r = 9\left(1 - \frac{V_T}{V_{DD}}\right)T \tag{29b}$$

(ii) *Fall time:* Suppose the light pulse is turned off at the time $t = 0$, and the initial output state $V_0(0)$ is V_{0H}, then the relation between the output voltage $V_0(t)$ and the time t can be obtained from the derivation similar to eqn. 26 with $I_{ph} = 0$

$$t = \int_0^t dt' = \int_{V_{0H}}^{V_0(t)} \frac{C_T\, dV_0(t')}{-k[V_{DSS}V_0(t') - V_0^2(t')/2]}$$
$$= \frac{m}{2}\left(1 - \frac{V_T}{V_{DD}}\right)T \ln\left\{\left[\frac{2V_{DSS}}{V_0(t)} - 1\right]\frac{[1 - \sqrt{(1-m)}]}{[1 + \sqrt{(1-m)}]}\right\} \tag{30}$$

and

$$V_0(t) = \frac{2V_{DSS}}{1 + \dfrac{1 + \sqrt{(1-m)}}{1 - \sqrt{(1-m)}}\exp\left[\dfrac{2t}{m(1 - V_T/V_{DD})T}\right]} \tag{31}$$

Therefore, the fall time t_f for $V_0(t)$ to drop from V_{0H} to $0.1V_{0H}$ can be solved from eqn. 30, and is

$$t_f = \frac{m}{2}\left(1 - \frac{V_T}{V_{DD}}\right)T \ln\left[\frac{19 + \sqrt{(1-m)}}{1 + \sqrt{(1-m)}}\right] \tag{32}$$

8.2.2. $m > 1$ ($I_{ph} > I_{DS}$:

(i) *Rise time:* Suppose the light pulse is turned on at the time $t = 0$, and the initial output state $V_0(0)$ is $V_{0L} = 0$ V, then the output starts at 0 V and changes to V_{0H} as the capacitance is charged.

When $V_0(t) \leqslant V_{DSS}$, the transistor operates in the triode region, and the relation between the output voltage $V_0(t)$ and the time t can be obtained from the derivation similar to eqn. 26 in Section 9.2.1 except for $m > 1$

$$t = \frac{C_T}{k/2}\int_{0\,\mathrm{v}}^{V_0(t)} \frac{dV_0(t')}{(2I_{ph}/k) - 2V_{DSS}V_0(t') + V_0^2(t')}$$
$$= \frac{m}{\sqrt{(m-1)}}\left(1 - \frac{V_T}{V_{DD}}\right)T$$
$$\times \tan^{-1}\left\{\frac{V_0(t)/\sqrt{(m-1)}}{V_{DSS} + [V_{DSS} - V_0(t)]/(m-1)}\right\} \tag{33}$$

and

$$V_0(t) = \frac{m(V_{DD} - V_T)}{1 + \sqrt{(m-1)}\Big/\tan\left[\dfrac{\sqrt{(m-1)}t}{m(1 - V_T/V_{DD})T}\right]} \tag{34a}$$

The time t_{r1} for $V_0(t)$ to charge from 0 V to V_{DSS} is

$$t_{r1} = \frac{m}{\sqrt{(m-1)}}\left(1 - \frac{V_T}{V_{DD}}\right)T \tan^{-1}\left[\frac{1}{\sqrt{(m-1)}}\right] \tag{35a}$$

When $V_0(t)$ is charged to be greater than V_{DSS}, the transistor operates in the saturation region, and the drain current is $I_D(t) = I_{DS}$. Here we use V_{DSS} as the new initial state, i.e. $V_0(0) = V_{DSS}$, then the output voltage $V_0(t)$ is given by

$$V_0(t) = V_{DD}\left[\left(1 - \frac{V_T}{V_{DD}}\right) + \left(1 - \frac{1}{m}\right)\frac{t}{T}\right] \tag{34b}$$

The time t_{r2} for $V_0(t)$ to be charged from V_{DSS} to $0.9V_{DD}$ can be solved from eqn. 34*b*, and given by

$$t_{r2} = \frac{m}{m-1}\left(\frac{V_T}{V_{DD}} - 0.1\right)T \tag{35b}$$

Therefore, the rise time for V_0 to charge from 0 V to $0.9V_{DD}$ is

$$t_r = t_{r1} + t_{r2}$$
$$= \left\{\frac{0.9}{m-1} + \left[\frac{1}{\sqrt{(m-1)}}\tan^{-1}\left[\frac{1}{\sqrt{(m-1)}}\right] - \frac{1}{m-1}\right]$$
$$\times \left(1 - \frac{V_T}{V_{DD}}\right)\right\}mT \tag{36}$$

(ii) *Fall time:* Suppose the light pulse is turned off at the time $t = 0$, and the initial output state $V_0(0)$ is V_{DD}, then the output starts at V_{DD} and approaches 0 V as the capacitance is discharged.

When $V_0(t)$ is greater than V_{DSS}, the transistor operates in the saturation region, and the drain current is $I_D(t) = I_{DS}$. The output voltage $V_0(t)$ is then

$$V_0(t) = V_{DD}\left(1 - \frac{t}{mT}\right) \tag{37a}$$

and the time t_{f1} for $V_0(t)$ to drop from V_{DD} to V_{DSS} can be solved from eqn. 37*a*, and given by

$$t_{f1} = \left(1 - \frac{V_{DSS}}{V_{DD}}\right)mT = \frac{V_T}{V_{DD}}\,mT \tag{38a}$$

When V_0 is smaller than V_{DSS}, the transistor operates in the triode region again. Here, we use V_{DSS} as the new initial state, i.e. $V_0(0) = V_{DSS}$, then the relation between the output voltage $V_0(t)$ and the time t can be obtained from the derivation similar to eqn. 30 in Section 8.2.1(i) except for $V_0(0) = V_{0H}$ given by $V_0(0) = V_{DSS}$ and $m > 1$

$$t = \int_0^t dt' = \frac{C_T}{k/2}\left\{-\int_{V_{DSS}}^{V_0(t)} \frac{dV_0(t')}{[2V_{DSS} - V_0(t')]V_0(t')}\right\}$$
$$= \frac{m}{2}\left(1 - \frac{V_T}{V_{DD}}\right)T \ln\left[\frac{2V_{DSS}}{V_0(t)} - 1\right] \tag{39}$$

and

$$V_0(t) = \frac{2V_{DSS}}{1 + \exp\left[\dfrac{2t}{m(1 - V_T/V_{DD})T}\right]} \tag{37b}$$

The time t_{f2} for V_0 to drop from V_{DSS} to $0.1V_{DD}$ can be solved from eqn. 39, and is given by

$$t_{f2} = \frac{m}{2}\left(1 - \frac{V_T}{V_{DD}}\right)T \ln\left(19 - 20\,\frac{V_T}{V_{DD}}\right) \tag{38b}$$

Therefore, the fall time for $V_0(t)$ to drop from V_{DD} to $0.1V_{DD}$ is

$$t_f = t_{f1} + t_{f2}$$
$$= \left[\frac{V_T}{V_{DD}} + \frac{1}{2}\left(1 - \frac{V_T}{V_{DD}}\right)\ln\left(19 - 20\,\frac{V_T}{V_{DD}}\right)\right]mT \tag{40}$$