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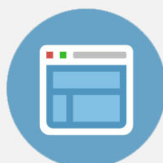

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Carrier depletion by defects levels in relaxed $In_{0.2}Ga_{0.8}As/GaAs$ quantum-well Schottky diodes

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An increase in leakage current accompanied by a drastic carrier depletion is found for InGaAs/GaAs Schottky diodes when the InGaAs thickness is larger than its critical thickness. Due to drastic carrier depletion, free-carrier concentration around the InGaAs region for relaxed samples cannot be obtained from capacitance–voltage data but from resistance–capacitance time constant effect observed in capacitance–frequency measurement. A trap at 0.33 to 0.49 eV is observed for relaxed samples by deep-level transient spectroscopy. The resistance caused by carrier depletion has an activation energy close to that of the trap, supporting that the carrier depletion is caused by capture from the trap. © *2000 American Institute of Physics.* [S0021-8979(00)00603-4]

I. INTRODUCTION

The InGaAs/GaAs material system has many important applications for electronic and optoelectronic devices. However, due to lattice mismatch between InGaAs and GaAs, there exists a critical thickness[1–4] of InGaAs, beyond which, strain relaxes and generates misfit dislocations, resulting in the degradation of device performance. Therefore, there is an obvious interest in investigating the defect states associated with strain relaxation. Different techniques such as the Hall effect,[5,6] photoluminescence,[7,8] deep-level transient spectroscopy (DLTS),[9–13] and cross-sectional transmission electron microscopy (TEM)[14–16] have been applied to study this material system. However, there still remains ambiguities about the nature of traps (electron or hole traps) and the exact location of the traps. Moreover, the correlation between carrier depletion and defect levels has not been studied in detail. Significant carrier depletion has been found when relaxation occurs, which will complicate the capacitance measurement. In this article, we will show the effects of carrier depletion on the capacitance–voltage measurement and DLTS. These two methods are usually used to obtain the free-carrier and trap concentrations. Also, we will show how to derive the properties of carrier depletion by capacitance–frequency ($C–F$) measurement.

II. EXPERIMENT

Five $In_{0.2}Ga_{0.8}As/GaAs$ quantum well structures with InGaAs thickness of 100, 200, 300, 400 and 1000 Å were grown on n^+-GaAs(001) substrates by Varian Gen II molecular beam epitaxy. The InGaAs quantum well was 0.3 μm from the surface to allow the depletion edge to sweep across it by applying voltage. Both the InGaAs region and the total 0.6-μm-thick GaAs epilayer were all Si-doped with a concentration of $6\times10^{16}\,cm^{-3}$. The whole structure was grown at 550 °C. The thickness and composition of InGaAs were determined by oscillation of reflection high energy electron diffraction. For the cases of 100 and 200 Å, the InGaAs thickness were further confirmed by the interference patterns observed in x-ray (004) diffraction.[17] Schottky diodes were fabricated by evaporating Al on samples with a dot diameter of 1500 μm.

III. MEASUREMENT AND RESULTS

A. Current–voltage characteristics

Figure 1 shows typical rectified forward current–voltage plot ($I–V$) characteristics at 300 K for all samples. Detail examination revealed that the saturation current J_s was related to the InGaAs thickness. The saturation current J_s was determined by extrapolating each curve to the current at zero volt. As shown, J_s is about 3×10^{-9} Å for 100 and 200 Å cases and increases to 10^{-8} A for 300 Å, to 2×10^{-8} Å for 400 Å and then to 4×10^{-8} A for 1000 Å. Leakage current is known to be contributed by defect states related to misfit dislocations, this result seems to indicate that the 100 and 200 Å samples are not yet relaxed while 300, 400 and 1000 Å samples are relaxed and their degree of relaxation increases with InGaAs thickness. Therefore, the InGaAs critical thickness should be between 200 and 300 Å. This critical thickness is consistent with our previous results from double-crystal x-ray diffraction.[17] It should be noted that the 1000 Å sample has a relatively large series resistance, as can be seen

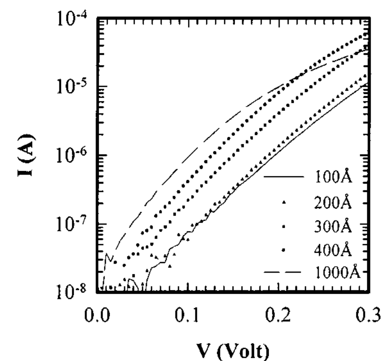

FIG. 1. The forward $I–V$ characteristics at 300 K for $In_{0.2}Ga_{0.8}As/GaAs$ Schottky diodes with InGaAs thickness of 100, 200, 300, 400, and 1000 Å.

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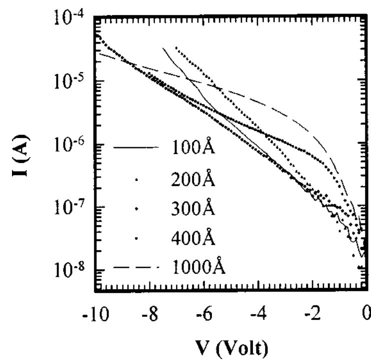

FIG. 2. The reverse $I-V$ characteristics at 300 K for $In_{0.2}Ga_{0.8}As$/GaAs Schottky diodes with InGaAs thickness of 100, 200, 300, 400, and 1000 Å.

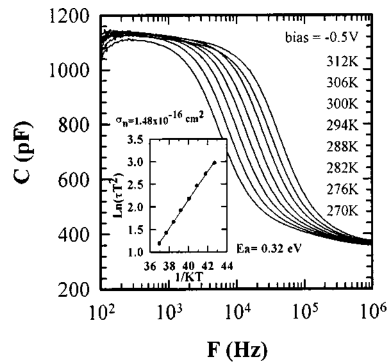

FIG. 4. The temperature-dependent $C-F$ spectra at $V=-0.5$ V for 1000 Å case. Shown in the inset is its Arrhenius plot of R determined from its inflexion frequency.

from the bending of current at large bias. The origin of this large resistance is due to a significant carrier depletion.

Figure 2 shows that under a small reverse bias ($|V|<2$ V), the reverse-bias current increases with increasing InGaAs thickness, similar to the forward saturation current, indicating that the leakage current at small reverse bias can also be used to determine the critical thickness. For $|V|<2$ V the $C-V$ measurement shows that the InGaAs layer is outside the Schottky depletion region. The increase in the leakage current with increasing InGaAs thickness suggests that the effects of the defect states introduced by relaxation extend to the depletion region. For large reverse voltages ($|V|>4$ V), the slope of current with voltage decreases for 400 and 1000 Å samples, especially for 1000 Å samples. This is due to the same resistance loading effect from carrier depletion as in forward current.

B. Capacitance–frequency measurement

Samples were previously examined by $C-V$ measurement.[17] For completeness, the apparent carrier concentration derived from it is shown in Fig. 3. In contrast to a carrier confinement in the quantum well for 100 and 200 Å samples, carriers are depleted for 300, 400 and 1000 Å samples. A drastic carrier depletion seems to occur when InGaAs thickness increases from 200 to 300 Å. Carrier depletion is so significant that it goes beyond the InGaAs region and spreads to GaAs layers on both sides. Carrier depletion is accompanied by an increase in leakage current, indicating that both deteriorations probably result from the same defect states. Present results also illustrate that leakage current and carrier depletion can be used to determine the critical thickness.

In this article, we are particularly interested in the carrier depletion in the relaxed samples. A significant carrier depletion will introduce a high-resistive layer. The series resistance R observed in both forward and reverse current for 1000 Å case will introduce a RC time constant which can reduce the high-frequency capacitance in $C-F$ spectra. Figure 4 shows the temperature-dependent $C-F$ spectra for the 1000 Å case, which shows a clear capacitance step. Let us assume that an acceptor level exists in the InGaAs region which can capture free-carriers and produce a relatively high-resistive layer. A band diagram pertaining to this effect is shown in Fig. 5(a), which contains a Schottky barrier with

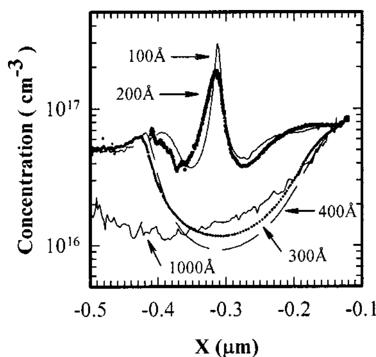

FIG. 3. The apparent carrier depth profiles converted from $C-V$ data for $In_{0.2}Ga_{0.8}As$/GaAs structures with InGaAs thickness of 100, 200, 300, 400, and 1000 Å.

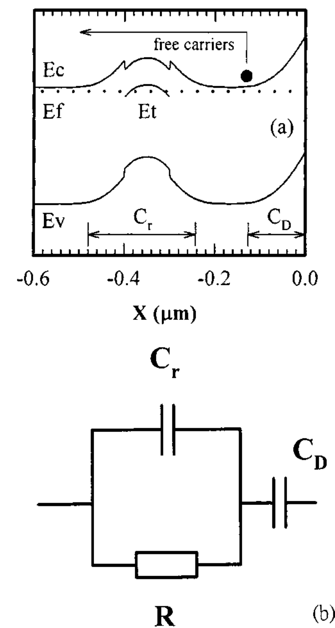

FIG. 5. (a) The band diagram contains a Schottky barrier with a depletion capacitance C_D and a high-resistive InGaAs region represented by a resistance R in parallel with capacitance C_r. (b) The corresponding equivalent circuit.

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a depletion capacitance C_D and a high-resistive layer which can be represented by a large resistance R in parallel with capacitance C_r.

An equivalent circuit corresponding to the band diagram in Fig. 5(a) is shown in Fig. 5(b), which will give rise to step-like capacitance spectra as shown in Fig. 4. At high frequencies where $1/\omega \ll (C_D + C_r)R$, free carriers cannot follow the frequency to traverse through the high-resistive layer, the observed high-frequency capacitance C_h is the series combination of C_D and C_r. From Fig. 4, at $V = -0.5\,\mathrm{V}$, C_h is about 400 pF corresponding to 0.51 μm which, as expected, is less than the total epitaxial thickness of 0.7 μm. At low frequencies where $1/\omega \gg R(C_D + C_r)$, the free carriers can traverse through the high-resistive layer so that the observed low-frequency capacitance is the Schottky depletion capacitance C_D. Figure 4 shows that C_D is about 1100 pF which corresponds to a thickness of 0.18 μm. Thus, the effective thickness of the high-resistive layer is 0.32 μm obtained from C_r using $C_h = C_D C_r/(C_D + C_r)$. The inflexion frequency ω at which the capacitance drops from high to low plateaus corresponds to the RC time constant effect: $\omega = 1/R(C_D + C_r)$. By fitting to the experimental data in Fig. 4, we obtained $R = 3000\,\Omega$ for $T = 300\,\mathrm{K}$, which is close to a series resistance of 2800 Ω obtained from fitting the forward $I-V$ in Fig. 1 using $I = I_s \exp[q(V-RI)/nkT]$. The activation energy of R determined from its Arrhenius plot was 0.32 eV for $V = -0.5\,\mathrm{V}$ as shown in the inset of Fig. 4. Assuming the acceptor's concentration is higher than the incorporated Si dopants, Fermi level is almost pinned to the acceptor level and this activation energy should be close to the energy position of the acceptor level.

Using 0.32 eV for the energy position of the acceptor trap, assuming a concentration of $2\times10^{17}\,\mathrm{cm}^{-3}$ in the InGaAs region and a background Si donor concentration of $6\times10^{16}\,\mathrm{cm}^{-3}$, a numerical simulation resembling that used by Missous and Rhoderick[18] was undertaken on the $C-V$ and depth profile by solving the Poisson equation. Figure 6(a) shows the band diagram for 1000-Å-thick InGaAs and its corresponding free electron concentration. Figure 6(b) shows the simulated $C-V$ and its converted depth profile. During the simulation, it is assumed the trap cannot follow the frequency of the ac measuring signal. This assumption is justified by the experimental condition. In the $C-V$ experiment, the ac frequency was taken to be 2 kHz to avoid the series resistance effect. From DLTS which will be discussed later, the emission time (at 300 K) of the trap is about 0.02 s which is two orders of magnitude longer than the period of the ac measuring frequency. Depending on the sweeping rate of the dc bias for $C-V$ measurement, the solid curve in Fig. 6(b) shows the simulated $C-V$ when the trap can follow the sweeping rate of the dc bias for $C-V$ measurement, while the dotted curve cannot. The simulated $C-V$ is almost the same for both cases. In our experiment, our measured $C-V$ is believed to be between these two conditions.

It can be seen from Fig. 6(b) that the simulated depth profile is similar to the measured concentration profile shown in Fig. 3. Both cases show that the apparent carrier concentration in the InGaAs region is about $1\times10^{16}\,\mathrm{cm}^{-3}$ which is more than four orders of magnitude higher than the real free-

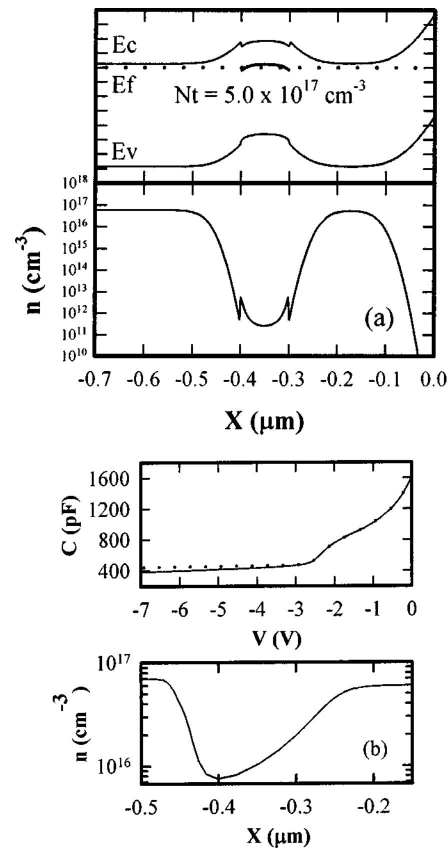

FIG. 6. (a) The band diagram assuming $5\times10^{17}\,\mathrm{cm}^{-3}$ for the trap concentration in the InGaAs region (1000 Å) and its corresponding free electron concentration. (b) The solid curve is simulated $C-V$ when the trap can follow the sweeping rate of the dc bias and its converted depth profile. The dotting $C-V$ curve is the simulated $C-V$ when the trap cannot follow the sweeping rate of the dc bias.

carrier concentration (about $10^{12}\,\mathrm{cm}^{-3}$). This low concentration gives a Debye length larger than 1 μm. Because of this resolution limitation, the measured concentration around the InGaAs region does not give the real free-carrier concentration. On the other hand, the range of carrier depletion from the experiment is broader than that from the simulation. This is because the trap is only assumed in the InGaAs region during simulation. But in reality, the trap extends beyond the InGaAs region, especially into the bottom GaAs layer. This result shows that the real carrier concentration around the InGaAs region cannot be obtained from $C-V$ data but can be estimated from the resistance R as observed in $C-F$ spectra. Although this simulation is undertaken for the 1000 Å case, because measured $C-V$ also shows a significant carrier depletion, a similar result can be applied to 300 and 400 Å cases.

C. Deep-level transient spectroscopy

Figures 7(a), (b), (c), (d), and (e) shows the DLTS spectra for 100, 200, 300, 400, and 1000 Å cases measured by a HP4194 gain-phase analyzer. The DLTS spectra were taken after sweeping the voltage from 0 to -4 V. The fill time was set at 5 s at 0 V. From $C-V$ data, this sweeping voltage enables us to probe the region including the quantum well. Except for the 1000 Å case, a DLTS signal always appeared

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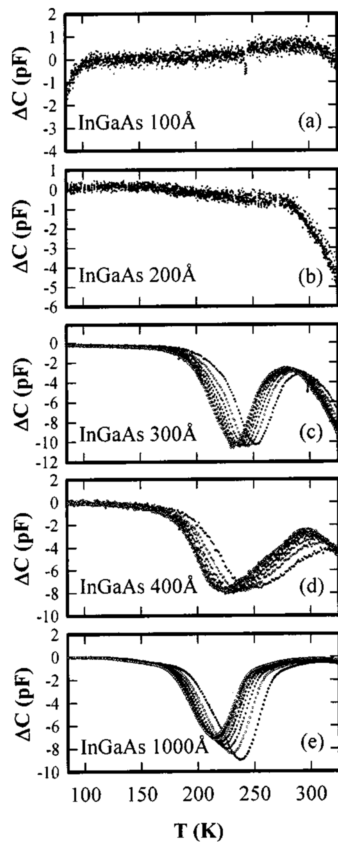

FIG. 7. (a), (b), (c), (d), and (e) show the DLTS spectra for 100, 200, 300, 400, and 1000 Å cases. The DLTS spectra were taken after sweeping the voltage from 0 to −4 V. The fill time was set at 5 s at 0 v. The rate window is 0.59, 1.18, 1.78, 2.37, 2.97, 3.56, 4.16, 4.75 s^{-1} for each curve.

at high temperatures around 325 K. Because of its high temperature, we could not determine its parameters. This high-temperature defect is suspected to be EL2, which has been reported to exist in InGaAs.[19]

Besides this high-temperature defect, no detectable DLTS signals were observed for 100 and 200 Å cases. However, a dominating DLTS signal was observed at temperatures around 200–250 K for 300, 400, and 1000 Å cases. Figure 8 shows the modified emission time τT^2 vs $1000/T$, the activation energies (capture cross section) of the traps were determined to be $E_a = 0.49\,\text{eV}(8\times10^{-16}\,\text{cm}^2)$ for 300 Å, $E_a = 0.33\,\text{eV}(7.3\times10^{-19}\,\text{cm}^2)$ for 400 Å, and $E_a = 0.33\,\text{eV}(1.4\times10^{-18}\,\text{cm}^2)$ for 1000Å. The reason why the activation energy is larger for 300 Å is not clear at this point, but is suspected to be related to the InGaAs thickness. We have measured several diodes of the 300 Å sample, their activation energies were always around 0.49 eV with variations no more than 0.05 eV. Although their activation energies are somewhat different, from their positions in Arrhenius plot, they should belong to the same trap. Because it is only observed in the relaxed samples, this trap is related to defect states associated with the misfit dislocations introduced by lattice relaxation. A similar trap at 0.395 eV has been observed by Uchida *et al.*[10] on a 700-Å-thick $In_{0.2}Ga_{0.8}As$.

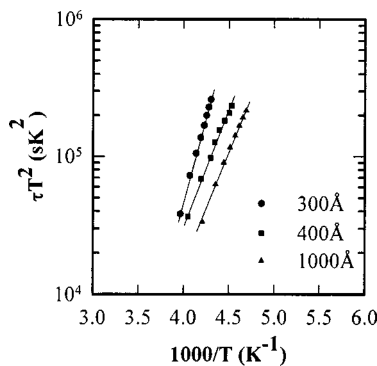

FIG. 8. The modified emission time τT^2 vs 1000/T for the DLTS spectra. The activation energies were determined to be $E_a = 0.49$ eV for 300 Å, $E_a = 0.33$ eV for 400 Å, and $E_a = 0.33$ eV for 1000 Å.

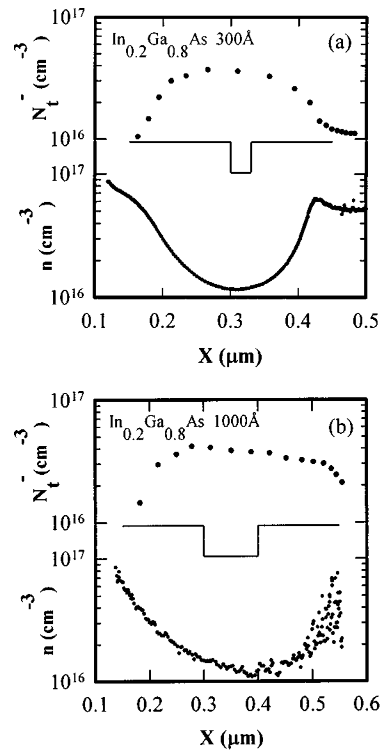

FIG. 9. The ionized acceptor N_A^- profiles from DLTS for (a) 300 Å and (b) 1000 Å cases along with their apparent carrier concentrations.

In order to obtain the trap distribution, we reduced the sweeping voltage to 0.2 V, that is from 0 to −0.2 V, from −0.2 to −0.4 V and so on, in the DLTS experiment. The results of the ionized acceptor N_A^- are shown in Figs. 9(a) and 9(b) for 300 and 1000 Å, respectively. The concentration of N_A^- was estimated by using

$$N_A^- = N_D^+(\Delta C/C)\left(\frac{C_0}{C_0 - C_i}\right),$$

here $N_D^+ = 6\times10^{16}\,\text{cm}^{-3}$, C_0 was the steady-state capacitance before the sweeping voltage was applied, and C_i was the capacitance right after the sweeping voltage was applied. In both cases, N_A^- starts to increase from the top GaAs cap layer, showing maximum values of 4.2×10^{16} and $3.7\times10^{16}\,\text{cm}^{-3}$ for 300 and 1000 Å cases around the quantum well, and falls off into the GaAs bottom layer.

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In general, the profile of N_A^- and its magnitude are quite similar for 300 and 1000 Å cases. If N_A^- is due to the misfit dislocations, a similar N_A^- for both 300 and 1000 Å cases seems to be contradictory to the results of TEM previously reported,[11] where a higher density of misfit dislocations is expected for 1000 Å. Also the very broadness of N_A^- profile does not reflect the fact that misfit dislocations are mostly confined to the bottom interface as seen in TEM.[10] However, if we compare the N_A^- profile with the apparent carrier concentration [also shown in Figs. 9(a) and 9(b)], we find that their general shape are very similar, leading us to believe that the resolution of the N_A^- profile is also limited by Debye length. Any detailed variation of trap concentration around the InGaAs region cannot be obtained. Although the N_A^- profile is not correct around the InGaAs region, its order of magnitude is more or less reliable. In addition, the concentration away from the InGaAs region on both sides is still correct to a certain extent. Therefore, we still can draw several conclusions. First, although the detailed profile is not accurate around the InGaAs region, the order of magnitude of traps is able to capture most of the incorporated free electrons ($6\times10^{16}\,\mathrm{cm}^{-3}$), resulting in a significant carrier depletion. Second, the activation energy (0.32 eV) of the high-resistive layer determined from $C-F$ spectra is close to that of the traps from DLTS, suggesting that the resistance is due to the trap seen in DLTS. Therefore, we conclude that the carrier depletion is caused by capture from the trap at 0.33–0.49 eV.

IV. CONCLUSIONS

In summary, an increase in the leakage current and a dramatic carrier depletion are found when InGaAs thickness increases beyond its critical thickness. Critical thickness determined from leakage current, carrier depletion, and x-ray diffraction are in agreement with one another. Due to a significant carrier depletion, the free-carrier concentration around the InGaAs region for the relaxed samples cannot be obtained from $C-V$ measurement. Instead its concentration is estimated from the resistance of the depleted InGaAs region which introduces a RC time constant effect in the capacitance–frequency spectra. The activation energy of the resistance is close to that observed in DLTS, indicating that the carrier depletion is caused by the trap at 0.33–0.49 eV.

ACKNOWLEDGMENT

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