A New Charge-Pumping Technique for Profiling the Interface-States and Oxide-Trapped Charges in MOSFET's

Yu-lin Chu, *Student Member, IEEE*, Da-Wen Lin, and Ching-Yuan Wu, *Member, IEEE*

***Abstract*—A new charge-pumping method has been developed to characterize the hot-carrier induced local damages. By holding the rising and falling slopes of the gate pulse constant and then varying the high-level $(V_{\rm GH})$ and base-level $(V_{\rm GL})$ voltages, the lateral distribution of interface-states $(N_{\rm it}(x))$ and oxide-trapped charges $(Q_{\rm ox}(x))$ can be profiled. The experimental results show that during extracting $Q_{\rm ox}(x)$ after hot-carrier stress, a contradictory result occurs between the extraction methods by varing the high-level $(V_{\rm GH})$ and base-level $(V_{\rm GL})$ voltages. As a result, some modifications are made to eliminate the perturbation induced by the generated interface-states after hot-carrier stress for extracting $Q_{\rm ox}(x)$.**

***Index Terms*—Charge-pumping method, interface-states, MOSFET, oxide-trapped charges.**

I. INTRODUCTION

THE charge-pumping technique has become a powerful tool to quantitatively measure the energy and lateral distribution of interface-states and the oxide-trapped charges [1]–[5], and has been utilized extensively to invesigate the hot carrier degradation induced by localized interface-states and the oxide-trapped charges [6], [7]. Some researchers [4], [8], [9] had assumed that the initial interface-states of a fresh device were uniformly distributed on the Si–SiO$_2$ interface and the position of the interface-states generated by hot-carried stress could be easily extracted by some simple transformations. Actually, the initial interface-states are not necessary to be uniformly distributed and hence these methods used to extract the damaged position might not be correct. In some other papers [9], [10], the "charge-neutralization" technique was used to compensate the stress-induced oxide-trapped charges, in which carriers of opposite polarity were injected into oxide layer to make the damaged region neutralized (i.e. hot-electron injection for hole traps and hot-hole injection for electron traps). It is extremely difficult to inject hot-carriers into the gate oxide without generating extra interface-states. Therefore, the hot-carrier neutralization process may introduce errors and the accuracy of this technique is doubtful. In fact, it is well known that even no extra interface-states are generated by the hot-carrier neutralization process, the injected carriers are not stable and would leak away as time passed [11], [12]. Besides, charge-pumping measurement is very time-consuming, there is no way to ensure that the injected carriers would not leak away during charge-pumping measurement.

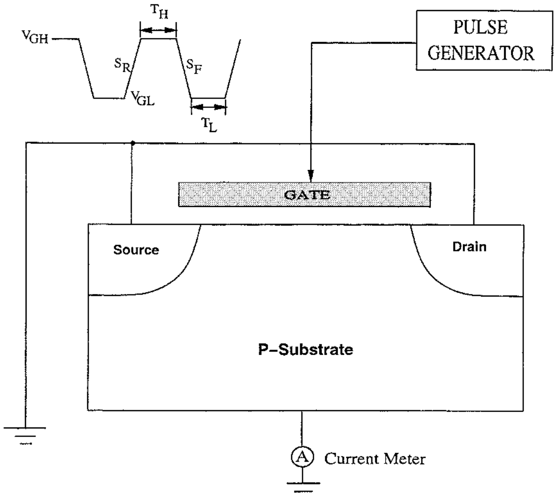

Fig. 1. Experimental setup of the charge-pumping measurement and the shape of the gate pulse.

In this paper, a new charge-pumping technique for profiling both interface-states and oxide-trapped charges is presented, and some unreasonable assumptions are removed.

II. BASIC PRINCIPLE

In this section, the basic principle of the charge-pumping technique is described, some questionable assumptions are discussed, and the methods for further improvement are then made. The experimental setup for charge-pumping current measurement is shown in Fig. 1, where the gate pulse is provided by a HP 8110A pulse generator, and a HP 4145B parameter analyzer is used to monitor the charge-pumping current. In this work, the source/drain and substrate electrodes are always grounded to prevent any undesirable stress caused by measurement.

The charge-pumping current contributed by a local area can be written as

$$I_{\rm cp} = q \cdot W \cdot f \cdot \int_0^{L'} N_{\rm it}(x)\, dx \tag{1}$$

where W is the channel width, f is the gate pulse frequency;, $N_{\rm it}(x)$ is the local interface-state density per area, and the

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The authors are with the Advanced Semiconductor Device Research Laboratory and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C.

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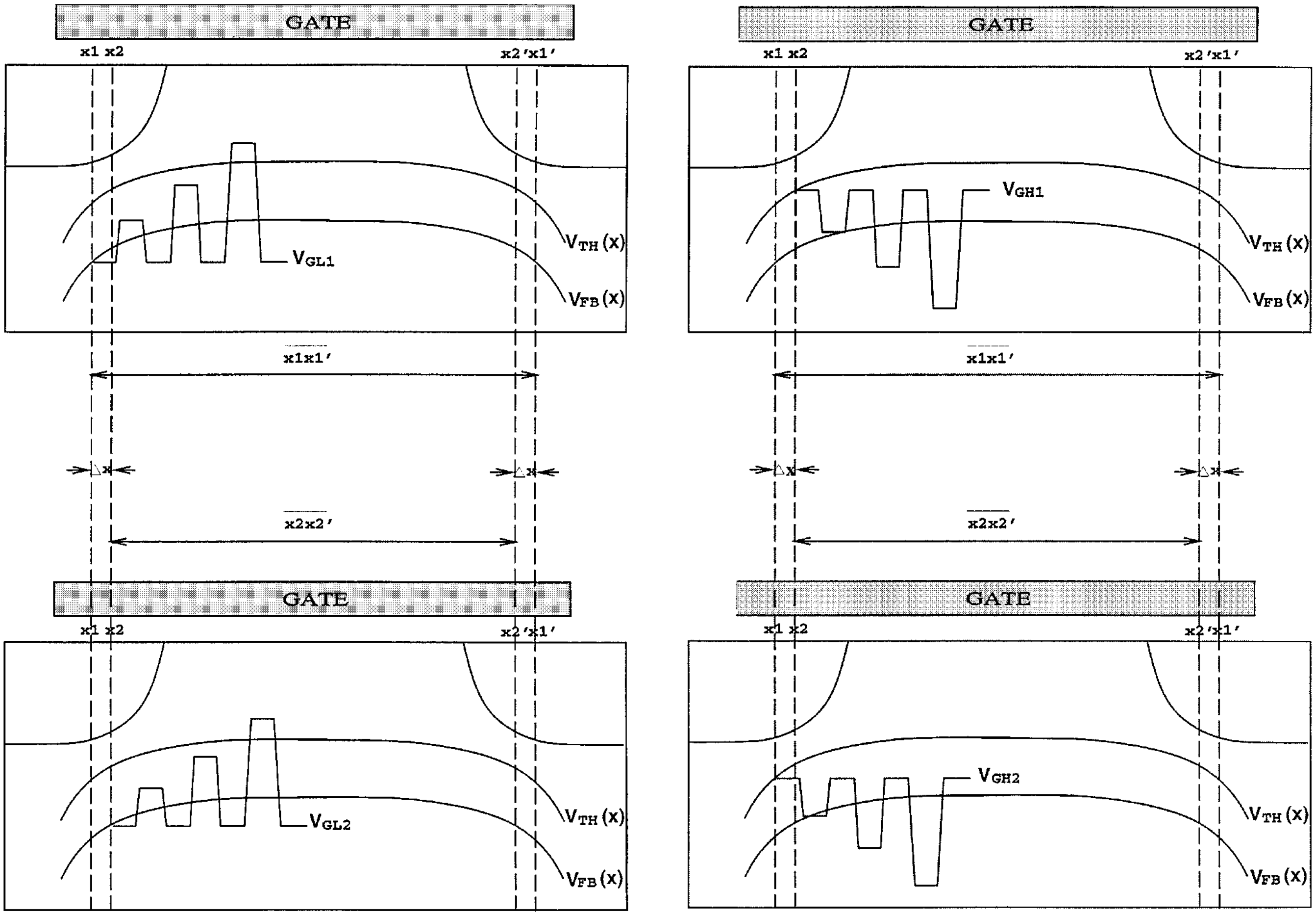

(a) (b)

Fig. 2. Illustration of the given gate-pulse voltage versus effective charge-pumping area for (a) base-level $(V_{\rm GL})$ and (b) high-level $(V_{\rm GH})$.

integration range from zero to L' gives the lateral length that can contribute to the charge-pumpint current. Note that only the region where the surface potential can fully swing from accumulation to inversion would provide the charge-pumping current. Based on this fact, the interface-states and the oxide-trapped charges on the Si–SiO2 interface can be profiled.

The basic principle is described as follows. As shown in Fig. 2(a), the pulse generator gives a series of pulses with the base-level fixed at $V_{\rm GL1}$ and high-level $V_{\rm GH}$ starting from a value slightly larger than $V_{\rm GL1}$ to a fixed high-level to ensure that the charge-pumping current can reach its saturated value. After this step, the charge-pumping current attributed by the region between x_1 and x_1' can be measured. The result of $I_{\rm cp}(V_{\rm GL1})/f$ is shown in Fig. 3. Again, a series of pulses with the base-level fixed at $V_{\rm GL2}$ which is slightly larger than $V_{\rm GL1}$ is generated, then the charge-pumping current attributed by the region between x_2 and x_2' can be measured. The result of $I_{\rm cp}(V_{\rm GL2})/f$ is also shown in Fig. 3. Note that the $V_{\rm GL}$ difference used to extract the interface-states and the oxide-trapped charges should not be too small, otherwise the noise induced by the measurement error will be serious. On the other hand, if the $V_{\rm GL}$ difference is large, the profiling resolution of interface-states and oxide-trapped charges will decrease. The difference between $I_{\rm cp}(V_{\rm GL1})/f$ and $I_{\rm cp}(V_{\rm GL2})/f$ is shown in Fig. 3, which is the charge-pumping current provided by the small region between $x_1 - x_2$ and $x_1' - x_2'$. $\Delta I_{\rm cp}/f$ behaves like a standard charge-pumping curve, which consists of a rising edge and a saturation region with the saturation value equal to $\Delta I_{\rm cp,sat}/f$. If the interface-states were generated after

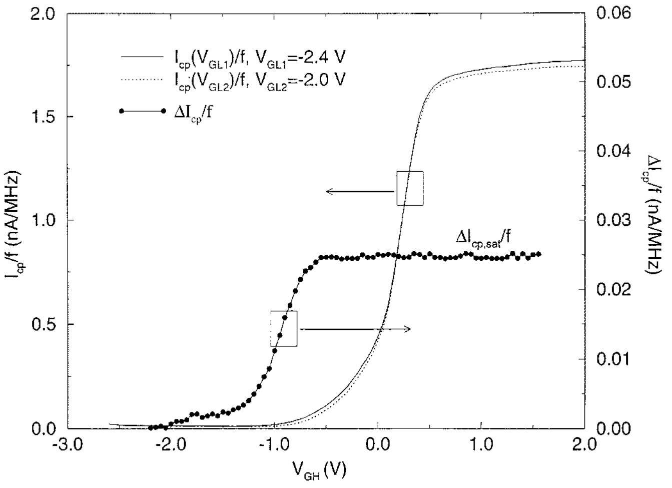

Fig. 3. Two charge-pumping currents with different base-levels and the difference between them.

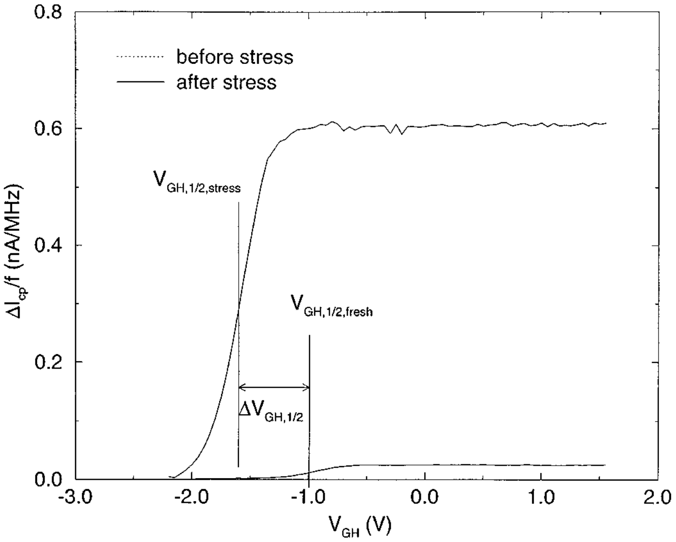

Fig. 4. Pre-stress and post-stress charge-pumping currents inside a small area defined by two different base-levels.

hot-carrier stress, the saturation level of $\Delta I_{\rm cp,sat}/f$ would increase because there are more interface-states to produce the charge-pumping current. If the oxide-trapped charges were generated by hot-carrier stress, the rising edge of $\Delta I_{\rm cp}/f$ would shift parallelly because the local threshold-voltage is changed by the oxide-trapped charges. If the polarity of the trapped charges is negative, the curve would shift to right because the local threshold-voltage increases. If the polarity of the oxide-trapped charges is positive, the curve would shift to left because the local threshold-voltage decreases. The half-maximum value of $\Delta I_{\rm cp}/f$ is chosen to be the reference point to measure the shift quantity $\Delta V_{\rm GH,1/2}$ [13], as shown in Fig. 4. Different base-levels of $V_{\rm GL}$ are related to different ranges where the potential can be biased into accumulation as the gate pulse stays low. This range is simulated by a two-dimensional (2–D) device simulator with a critical surface hole concentration p_c

$$\begin{cases} p_s(V_{\rm GL}, x) \geq p_c, & \text{if in } accumulation \\ p_s(V_{\rm GL}, x) < p_c, & \text{if not in } accumulation, \end{cases} \tag{2}$$

where $p_s(V_{\rm GL}, x)$ is the local hole concentration on the silicon surface. By comparing $\Delta I_{\rm cp}/f$ before and after stress, the total interface-states and the stress-induced oxide-trapped charges can be extracted by the following two equations:

$$N'_{\rm it}(x) = \frac{\Delta \frac{I_{\rm cp,sat}}{f}}{q \cdot W \cdot \Delta x} \tag{3}$$

and

$$Q'_{\rm ox} = C_{\rm ox} \Delta V_{\rm GH,1/2} \tag{4}$$

where

$$\Delta \frac{I_{\rm cp,sat}}{f} = \frac{I_{\rm cp}(V_{\rm GL1})}{f} - \frac{I_{\rm cp}(V_{\rm GL2})}{f}. \tag{5}$$

Similarly, the interface-states and the oxide-trapped charges can also be extracted by measuring the $I_{\rm cp}/f - V_{\rm GL}$ curves under different high-levels of $V_{\rm GH}$, as shown in Fig. 2(b). The typical $I_{\rm cp}/f - V_{\rm GL}$ and $\Delta I_{\rm cp}/f - V_{\rm GL}$ curves are shown in Fig. 5. It should be noted that during the measurement, the $V_{\rm GH}$ used should be smaller than the threshold-voltage so that the measured $I_{\rm cp}/f - V_{\rm GL}$ is mainly contributed by the region near or inside the gate and drain overlapped area. Furthermore, the $\Delta I_{\rm cp}/f - V_{\rm GL}$ curves and $\Delta V_{\rm GL,1/2}$ (the voltage shift related to half-maximum value of $\Delta I_{\rm cp}/f$ after stress) contributed by a local area near the drain junction from the difference of two $I_{\rm cp}/f - V_{\rm GL}$ curves measured at different $V_{\rm GH}$ levels can be obtained, as shown in Fig. 6. It should be noted that the $\Delta I_{\rm cp}/f$ after stress slightly falls in lower $V_{\rm GL}$, because the charge-pumping current difference $(\Delta I_{\rm cp}/f)$ contributed by a small area defined by two voltage levels of $V_{\rm GH}$ is very small (~ pA/MHz) even after stress and should be sensitive to the noise during measurement. Therefore, some measurement errors due to noise would result in a slight deviation from its saturated value. The rising edge of $\Delta I_{\rm cp}/f$ will shift to left for hole-traps and to right for electron-traps due to the change of

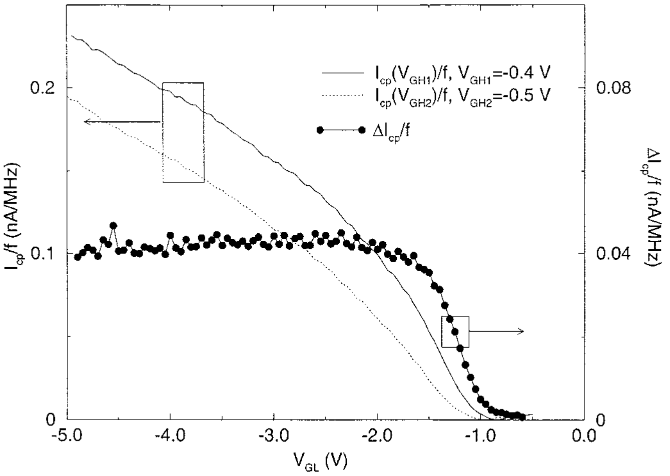

Fig. 5. Two charge-pumping currents with different high-levels and the difference between them.

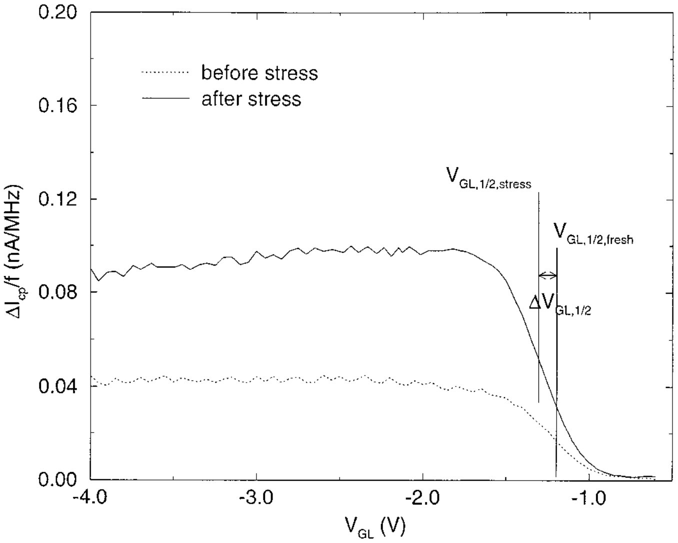

Fig. 6. Pre-stress and post-stress charge-pumping current inside a small area defined by two different high-levels.

local flat-band voltage. Note that different $V_{\rm GH}$ levels are related to different ranges where the potential can be biased into inversion as the gate pulse stays high. This range can also be simulated by a 2–D device simulator with a critical surface electron concentration n_c:

$$\begin{cases} n_s(V_{\rm GH}, x) \geq n_c, & \text{if in } inversion \\ n_s(V_{\rm GH}, x) < n_c, & \text{if not in } inversion \end{cases} \tag{6}$$

where $n_s(V_{\rm GH}, x)$ is the local electron concentration on the silicon surface. Also, the generated interface-states and the oxide-trapped charges should be written as

$$N''_{\rm it}(x) = \frac{\Delta \frac{I_{\rm cp,sat}}{f}}{q \cdot W \cdot \Delta x} \tag{7}$$

and

$$Q''_{\rm ox} = C_{\rm ox} \Delta V_{\rm GL,1/2} \tag{8}$$

where

$$\Delta \frac{I_{\rm cp,sat}}{f} = \frac{I_{\rm cp}(V_{\rm GH1})}{f} - \frac{I_{\rm cp}(V_{\rm GH2})}{f}. \tag{9}$$

In theory, both the magnitude and the position of $N'_{\rm it}(x)$ and $N''_{\rm it}(x)$ should be the same if n_c and p_c are correctly extracted while $Q'_{\rm ox}$ and $Q''_{\rm ox}$ would not be identical because the rising edge of both $I_{\rm cp}/f - V_{\rm GH}$ and $I_{\rm cp}/f - V_{\rm GL}$ curves would be perturbed by the generated interface-states after hot-carrier stress; that is, $Q'_{\rm ox}$ in (4) is underestimated for electron-traps and overestimated for hole-traps, and $Q''_{\rm ox}$ in (8) is overestimated for electron-traps and underestimated for hole-traps. Hence, the more reasonable method to extract the oxide-trapped charges should be modified and is described as follows.

$\Delta V_{\rm GH,1/2}$ and $\Delta V_{\rm GL,1/2}$ in (4) and (8) can be written as

$$\begin{aligned} \Delta V_{\rm GH,1/2} &= V_{\rm GH,1/2,stress} - V_{\rm GH,1/2,fresh} \\ &= \Delta V_{\rm ox} + \Delta V_{\rm in}, \end{aligned} \tag{10}$$

and

$$\begin{aligned} \Delta V_{\rm GL,1/2} &= V_{\rm GL,1/2,stress} - V_{\rm GL,1/2,fresh} \\ &= \Delta V_{\rm ox} - \Delta V_{\rm in} \end{aligned} \tag{11}$$

where $\Delta V_{\rm ox}$ is the shift value due to oxide-trapped charges, which is positive for hole-trap and is negative for electron-trap; $\Delta V_{\rm in}$ is the absolute shift value due to generated interface-states after stress; and the subscripts "fresh" and "stress" mean the conditions before and after stress. Combining (10) and (11) gives

$$\begin{aligned} \Delta V_{\rm ox} = \frac{1}{2}[&V_{\rm GH,1/2,stress} + V_{\rm GL,1/2,stress} \\ &- (V_{\rm GH,1/2,fresh} + V_{\rm GL,1/2,fresh})]. \end{aligned} \tag{12}$$

Therefore, the oxide-trapped charges excluding the interference caused by the generated interface-states should be written as

$$Q_{\rm ox} = C_{\rm ox} \Delta V_{\rm ox}. \tag{13}$$

During profiling the interface-states and the oxide-trapped charges, the critical surface electron and hole concentrations must be carefully defined, otherwise the position of extracted interface-states and oxide-trapped charges may be incorrect. The methods for extracting n_c and p_c are described in the next section.

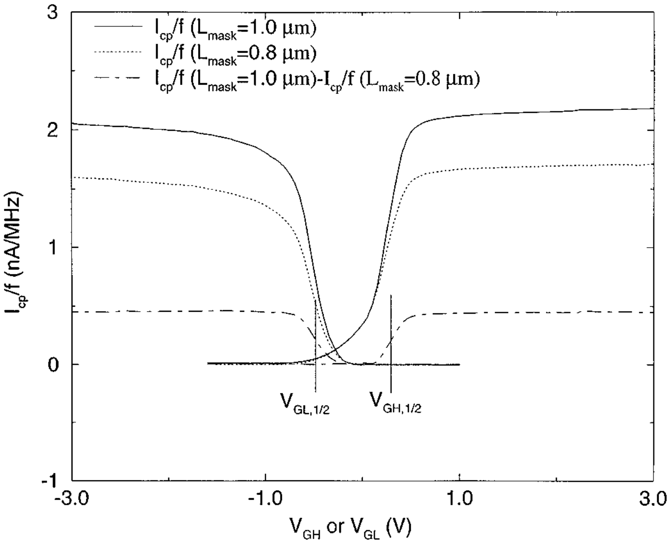

Fig. 7. $I_{\rm cp}/f - V_{\rm GL}$ and $I_{\rm cp}/f - V_{\rm GH}$ curves derived from the difference of two devices with different mask channel lengths.

III. Critical Surface Electron and Hole Concentration

In our experiment, two devices with different mask lengths are needed to extract critical surface electron and hole concentrations [13]. The mask lengths of the two devices are 1.0 μm and 0.8 μm, respectively. To extract the critical hole concentration p_c, the $I_{\rm cp}/f - V_{\rm GL}$ curve under a fixed high-level $V_{\rm GH}$, which can make the entire channel inverted, is applied to the two devices. These two devices are identical except the mask length so that the charge-pumping current difference $\Delta I_{\rm cp}/f - V_{\rm GL}$ of the two devices is mainly introduced by a small area inside the mid-channel region and the charge-pumping current contributed by the source/drain proximity effect can be ignored. The $\Delta I_{\rm cp}/f - V_{\rm GL}$ of the two devices is shown in Fig. 7, where $V_{\rm GL,1/2}$ corresponding to half-maximum of $\Delta I_{\rm cp}/f - V_{\rm GL}$ is set to be the flat-band voltage of the mid-channel region. $V_{\rm GL,1/2}$ is then put into a two-dimensional device simulator to simulate the surface hole concentraion. In our experiment, the simulated value is 1.5×10^{14}/cm^3 and hence we define $p_c = 1.5 \times 10^{14}$/cm^3. Similarly, a series of pulses with a fixed base-level $V_{\rm GL}$ are applied to the two devices to extract n_c with the same procedure, the $\Delta I_{\rm cp}/f - V_{\rm GH}$ is also shown in Fig. 7, where $V_{\rm GH,1/2}$ corresponding to half-maximum of $\Delta I_{\rm cp}/f - V_{\rm GH}$ is set to be the threshold-voltage of the mid-channel region. The simulated surface electron concentraion at $V_{\rm GH,1/2}$ is 7.8×10^{13}/cm^3 and n_c can be defined to be 7.8×10^{13}/cm^3.

IV. Experimental Results and Discussion

Based on the aforementioned charge-pumping technique, the interface-states and the oxide-trapped charges generated by hot-carrier stress are measured. The test devices are LDD n-MOSFET's with the mask channel length of 0.8 μm, the channel width of 120 μm and the oxide thickness of 110 Å, the device structure parameters used in 2-D device simulation

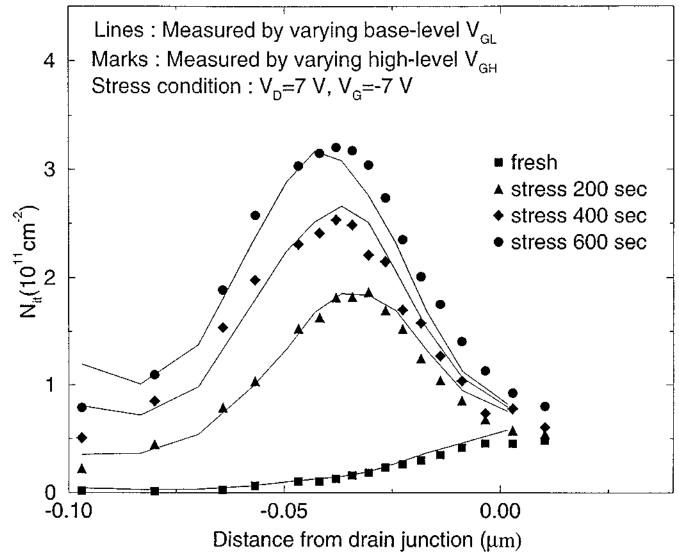

Fig. 8. Distribution of the cumulative interface-states with the stress condition: $V_D = 7$ V and $V_G = 7$ V.

are extracted by accurately simulating the curent-voltage (*I-V*) characteristics of the fresh device.

As described in Section II, the extraction procedures are summarized as follows.

1) Measure the $I_{\rm cp}/f - V_{\rm GL}$ and $I_{\rm cp}/f - V_{\rm GH}$ curves under various $V_{\rm GH}$ and $V_{\rm GL}$ conditions, respectively, then the $\Delta I_{\rm cp}/f - V_{\rm GL}$ and $\Delta I_{\rm cp}/f - V_{\rm GH}$ curves can be obtained.
2) Extract $V_{\rm GL,1/2}$ and $V_{\rm GH,1/2}$ from the $\Delta I_{\rm cp}/f - V_{\rm GL}$ and $\Delta I_{\rm cp}/f - V_{\rm GH}$ curves, respectively.
3) Extract n_c and p_c from the charge-pumping current difference $\Delta I_{\rm cp}/f - V_{\rm GH}$ and $\Delta I_{\rm cp}/f - V_{\rm GL}$ of the specified two short-channel devices, respectively.
4) Extract $N_{\rm it}(x)$ according to (3) and (7), and $Q_{\rm ox}(x)$ according to (12) and (13).

In our experiments, the $I_{\rm cp}/f - V_{\rm GH}$ curves are measured with $V_{\rm GL}$ varying from –2.4 V to –0.4 V and the $I_{\rm cp}/f - V_{\rm GL}$ curves are measured with $V_{\rm GH}$ varying from –0.1 V to –1.7 V, and both the rising slope (S_R) and the falling slope (S_F) of the gate pulse are fixed to ensure that the charge-pumping currents are contributed by the same band-gap region. In our case, both S_R and S_F of the gate pulse for measuring the $I_{\rm cp}/f - V_{\rm GH}$ and $I_{\rm cp}/f - V_{\rm GL}$ curves are set to be 2 V/µs.

In this work, the stress condition of $V_D = 7$ V and $V_G = -7$ V, which may generate band-to-band tunneling(BTBT)-induced hot hole [14], [15], is taken for example. As shown in Fig. 8, the magnitude and the position of interface-states are very close for the extraction method under different base-levels of $V_{\rm GL}$ and high-levels of $V_{\rm GH}$, this confirms the correctness of the extracted critical electron-surface concentration (n_c) and hole-surface concentration (p_c). It also shows that the distribution of the interface-states for a fresh device is not uniform, this result contradicts the basic assumption of some previous papers [4], [8], [9]. Furthermore, as shown in Fig. 9, $V_{\rm GL,1/2,stress}$ under different high-levels of $V_{\rm GH}$ and $V_{\rm GH,1/2,stress}$ under different base-levels of $V_{\rm GL}$ are extracted, where the values of $V_{\rm GH,1/2,stress}$ become smaller as the stress time incerases while the values of $V_{\rm GL,1/2,stress}$ are nearly invariant, this is contradictory if the hole-traps are generated after the BTBT-induced hot-hole stress. As a result, we can say that the extracted values of $V_{\rm GL,1/2,stress}$ were perturbed by the generated interface-states so that the values of $V_{\rm GL,1/2,stress}$ do not shift to a more negative value with cumulative stress time. Hence, (12) should be used to modify the contradictory results mentioned above and the extracted $Q_{\rm ox}(x)$ for different stress times are shown in Fig. 10. Note that as the surface potential under the gate/drain overlap region would be changed due to the generated interface-traps and oxide-trapped charges, the iteration process is necessary to obtain the accurate distribution, as mentioned in our previous work [5]. It should be noted that because the charge-pumping currents are very small for fresh devices, $V_{\rm GH,1/2,fresh}$ and $V_{\rm GL,1/2,fresh}$ in (12) are generated by 2-D numerical simulation instead of experimental results to prevent the measurement errors caused by noise. From Figs. 8 and 10, the maximum position of generated interface-traps is

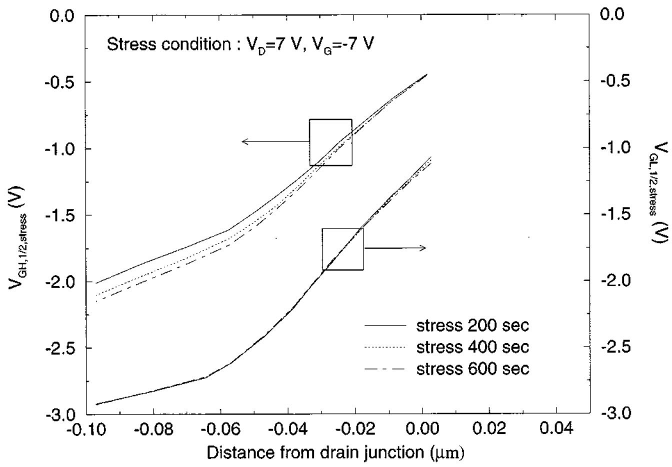

Fig. 9. $V_{\rm GH,1/2,stress}$ and $V_{\rm GL,1/2,stress}$ extracted from $\Delta I_{\rm cp}/f - V_{\rm GH}$ and $\Delta I_{\rm cp}/f - V_{\rm GL}$ curves, respectively.

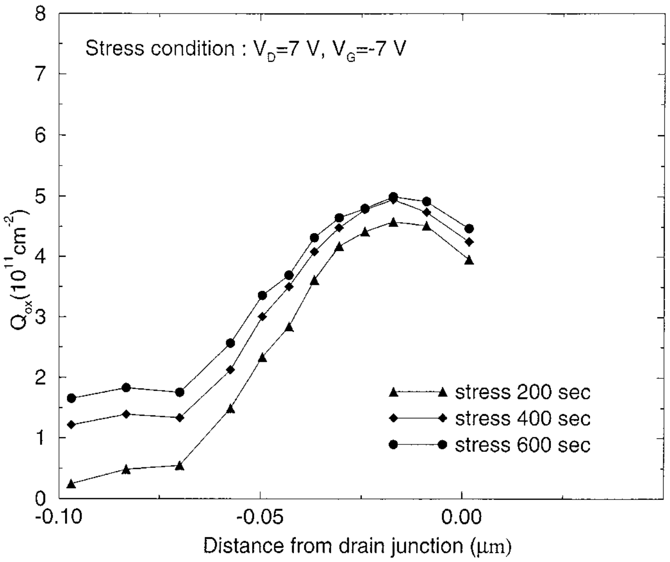

Fig. 10. distribution of the cumulative oxide-trapped charges with the stress condition: $V_D = 7$ V and $V_G = -7$ V.

inconsistent with that of oxide-trapped charges. The phenomenon is possible due to the fact that the generated electrons will travel toward the gate edge and the generated interface-traps are located near the gate edge; and the generated hole will travel away from the gate edge and the generated oxide-trapped charges are located away from the gate edge.

V. CONCLUSION

In this paper, the charge-pumping technique has been successfully applied to the characterization of stressd LDD n-MOSFET devices. In particular, a new method with modifying the existing extraction technique of oxide-trapped charges is presented. By holding the rising and failing slopes of the gate pulse constant and then varying the high-level and base-level of the gate pulse, the smooth $\Delta I_{\text{cp}}/f - V_{\text{GH}}$ and $\Delta I_{\text{cp}}/f - V_{\text{GL}}$ curves related to a localized area near or inside the drain and gate overlapped region can be easily obtained, and the interface-states and oxide-trapped charges related to this area can be calculated at the same time. The experimental results obtained from $\Delta I_{\text{cp}}/f - V_{\text{GH}}$ and $\Delta I_{\text{cp}}/f - V_{\text{GL}}$ curves during the extraction of $Q_{\text{ox}}(x)$ after hot-carrier stress contradict to each other, and some unreasonable assumptions are removed to eliminate the interference induced by the generated interface-states after hot-carrier stress for extracting $Q_{\text{ox}}(x)$.

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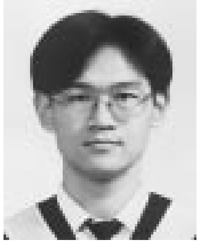
Yu-Lin Chu (S'91) was born in Taiwan, R.O.C., on September 10, 1968. He received the B.S. degree from the Department of Material Science and Engineering, National Tsing-Hua University, Taiwan, in 1991, and the M.S. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993. He is currently pursuing the Ph.D. degree at the same institute.

His present research areas focus on deep-submicrometer MOS device physics and reliability issues.



Da-Wen Lin was born in Taiwan, R.O.C., on February 10, 1974. He received the B.S. degree from the Department of Electronics Engineering, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 1996, and the M.S. degree from the Institute of Electronics, NCTU, in 1998.

He is currently in military service as a second Lieutenant. His research interest is in the modeling and physics of MOSFET reliability.

Mr. Lin is a member of Phi Tau Phi.

Ching-Yuan Wu (S'72-M'75) was born in Taiwan, R.O.C., on March 18, 1946. He received the B.S. degree in electrical engineering from the National Taiwan University, Taipei, in 1968, and the M.S. and Ph.D. degrees from the State University of New York (SUNY), Stony Brook, in 1970 and 1972, respectively.

During the 1972–1973 academic year, he was a Lecturer in the Department of Electronical Sciences, SUNY. During the 1973–1975 academic years, he was a Visiting Associate Professor at the National Chiao-Tung University (NCTU), Hsinchu, Taiwan. In 1976, he became Full Professor in the Department of Electronics and the Institute of Electronics at NCTU. While there, he was Director of the Engineering Laboratories and Semiconductor Research Center from 1974 to 1980, the Director of the Institute of Electronics from 1978 to 1984, and the Dean of the College of Engineering from 1984 to 1990. He was a Principal Investigator of the National Electronics Mass Plan-Semiconductor Devices and Integrated-Circuit Technologies from 1976 to 1979, and had been a Coordinator of the National Microelectronics Research and High-Level Man-Power Education Committee, National Science Council, Taiwan, from 1982 to 1988. He has been the Research Consultant of the Electronics Research and Service Organization (ERSO), ITRI, a member of the Academic Review Committee in the Ministry of Education, and the Chairman of the Technical Review Committee on Information and Microelectronics Technologies, Ministry of Economic Affairs. His research activities have been in semiconductor device physics and modeling, and integrated circuit designs and technologies. His current work focuses on the development of efficient 2-D and 3-D simulators for deep-submicrometer CMOS devices. He has published over 180 papers in the semiconductor field and has served as a reviewer for international journals such as IEEE ELECTRON DEVICE LETTERS, IEEE TRANSACTIONS ON ELECTRON DEVICES, and *Solid-State Electronics*.

Dr. Wu is a member of the Honorary Editorial Advisory Board of *Solid-State Electronics*, and is a board member of the Chinese Engineering Society. He received the Academic Research Award in Engineering from the Ministry of Education in 1979 and the Outstanding Scholar Award from the Chinese Educational and Cultural Foundation in 1985. He received the Outstanding Research Professor Fellowship from the Ministry of Education and National Science Council from 1982 to 1999. He received the Distinguished Engineering Professor Medal Award from the Chinese Engineering Society in 1992.