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Modeling of Interconnect Capacitance, Delay, and Crosstalk in VLSI

Shyh-Chyi Wong, Gwo-Yann Lee, and Dye-Jyun Ma

Abstract—**Increasing complexity in VLSI circuits makes metal interconnection a significant factor affecting circuit performance. In this paper, we first develop new closed-form capacitance formulas for two major structures in very large scale integration (VLSI), namely, 1) parallel lines on a plane and 2) wires between two planes, by considering the electrical flux to adjacent wires and to ground separately. We then further derive closed-form solutions for the delay and crosstalk noise. The capacitance models agree well with numerical solutions of three-dimensional (3-D) Poisson's equation as well as measurement data. The delay and crosstalk models agree well with SPICE simulations.**

Index Terms—**Closed-form models, delay and crosstalk, interconnect capacitance, simulations.**

I. Introduction

In modern very large scale integration (VLSI) technology, efforts have been devoted to reduce metal wiring pitch to increase chip density and to save silicon budget [3]–[5]. This makes metal wiring line resistance and line-to-line capacitance, thus the resistance-capacitance delay (*RC* delay) and interline crosstalk noise, increase. The huge amount of interconnection lines in VLSI makes the interconnect delay and crosstalk noise more dominant factors in the overall circuit speed [6]–[8].

Many works have been devoted to calculating line capacitance, e.g., [2]–[4]. Sakurai and Tamaru [2] derived formulas, both for parallel lines on a large plane. Choudhury *et al.* [3] gave models for several layout primitives but only for one set of technology parameters. Chern *et al.*[4] gave a general capacitance formula for three-dimensional crossing lines assuming same dielectric and wire thickness for all layers. In delay and crosstalk modeling, Sakurai [5] gave equations of distributed *RC* line, but solutions were not obtained in closed-form.

In this paper, we give a new model of metal interconnection, where closed-form formulas are derived for the wiring capacitance, delay and crosstalk noise, all as explicit functions of the wire thickness, dielectric thickness, interwire spacing and wire width. New capacitance formulas are first developed for two major structures in VLSI: 1) parallel lines on a plane and 2) wires between two planes; combinations of them can cover any given layout. The developed capacitance formulas then in turn lead to closed-form formulas for both the delay and crosstalk noise. Section II gives the capacitance model, and Section III gives the delay and crosstalk models, before the paper is concluded in Section IV.

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II. Interconnect Capacitance Model

We define two capacitance structures: 1) parallel lines on one plate as shown in Fig. 1(a), and 2) parallel lines between two plates as shown in Fig. 1(b). The first structure emulates lines without top wiring, and the second structure emulates lines with top wiring. In VLSI, that a line in a given layer is not (is) underneath a line can be covered by the first (second) structure. Developing formulas for the two fundamental structures is useful for simulating arbitrary integrated circuit layouts.

The interconnect capacitance is decomposed into two capacitance components: 1) $C_{\rm couple}$ is the flux to adjacent wire which affects both wiring delay and crosstalk noise and 2) $C_{\rm af}$ is the area and fringe flux to the underlying plane which determines wiring delay only.

Physical approach requires analytical solution of Poisson's equation, which often results in lengthy and complicated equations, often non-solvable. Thus, we adopt a semi-empirical approach here [2]–[5]. We use rational functions to give simple and explicit observations of field line variations with geometry parameters. The derived formulas model the field flux from different portions of an electrode separately, so that unique dimensional dependence of each electrical flux can be taken care of independently.

A. Parallel Lines on a Ground Plane

As shown in Fig. 1(a), wire thickness is denoted by T, dielectric thickness by H, interwire spacing by S and wire width by W. The range of dimension is chosen as $0.15 < T < 1.2, 0.16 < H < 2.71, 0.16 < S < 10$, and $0.16 < W < 2$, all in units of micrometers. The ranges of these parameters are selected based on applications in deep submicron VLSI. Although our models [(1)–(4) below] are tested and verified only over these selected ranges, they should prove to hold for parameter values outside the above ranges. It is simply because the solution to Poisson's equation is majorly affected by the relative values of the dimensional parameters, not their individual ones. This is exactly the rationale behind the derivation of our models in what follows.

First, $C_{\rm couple}$ is modeled as the summation of three rational functions which simulate three flux components, and is obtained explicitly via the least-square fitting as

$$\begin{aligned}\frac{C_{\rm couple}}{\epsilon_{\rm ox}} = {} & 1.144\frac{T}{S}\left(\frac{H}{H+2.059S}\right)^{0.0944} \\ & + 0.7428\left(\frac{W}{W+1.592S}\right)^{1.144} \\ & + 1.158\left(\frac{W}{W+1.874S}\right)^{0.1612} \\ & \cdot\left(\frac{H}{H+0.9801S}\right)^{1.179} \qquad (1)\end{aligned}$$

where $\epsilon_{\rm ox} = 3.9 \times 8.85 \times 10^{-14}$ F/cm. The first term on the right-hand side of (1) models side-wall flux, which is linearly proportional to T and decreases as H/S decreases (i.e., as ground flux increases), because more flux originated from side wall now gets attracted to ground. The second term gives the upper-surface flux contribution, which increases as W increases or as S decreases, and which is independent of the ground flux. The third term models the lower surface flux, which is heavily inversely proportional to the ground flux. The power-law de-

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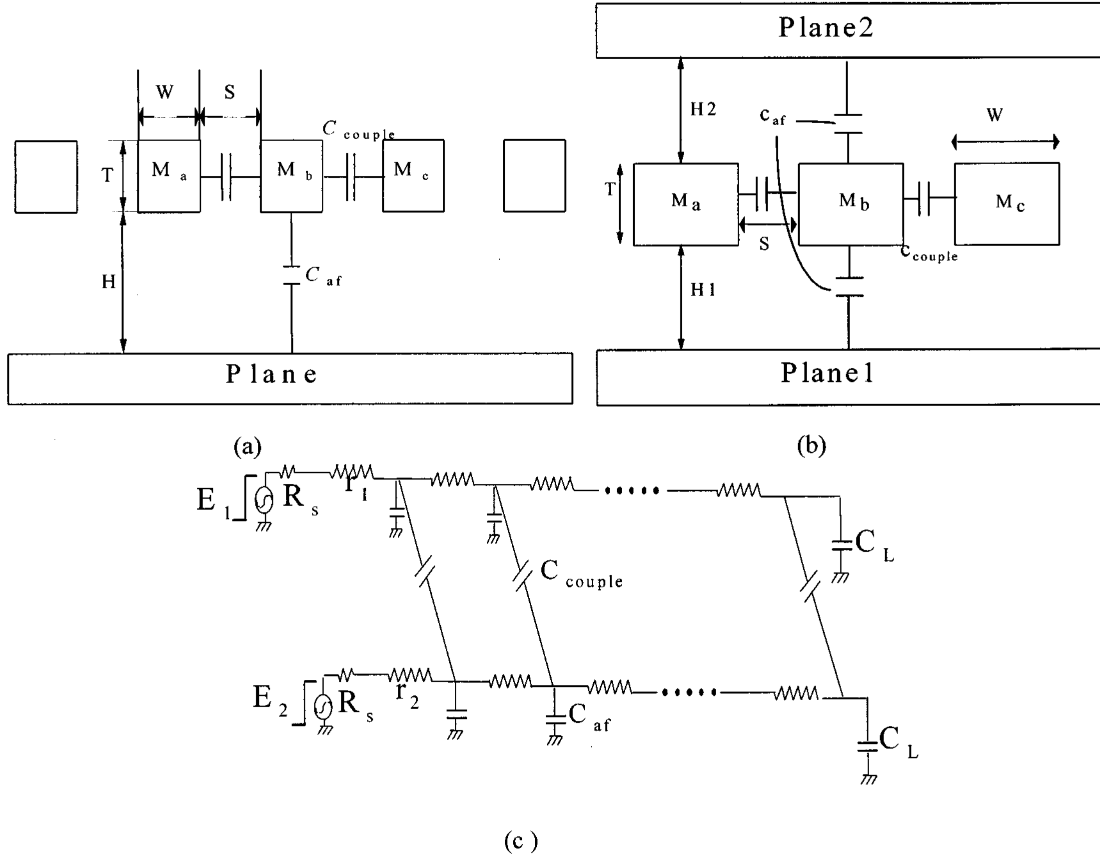

Fig. 1. (a) Cross-section diagram of parallel lines on one plane and corresponding layout. (b) Cross-section diagram of parallel lines between two planes. (c) Schematic diagram of distributed *RC* line.

pendence in these functions has been a good approximation to the field strength between adjacent nonoverlapping perpendicular surfaces [2], [5].

$C_{\rm af}$ is similarly modeled as the summation of three rational functions to simulate three flux components, and is obtained explicitly via the least-square fitting as

$$\frac{C_{\rm af}}{\epsilon_{\rm ox}} = \frac{W}{H} + 2.217\left(\frac{S}{S+0.702H}\right)^{3.193} + 1.171\left(\frac{S}{S+1.510H}\right)^{0.7642} \cdot \left(\frac{T}{T+4.532H}\right)^{0.1204}. \tag{2}$$

The total capacitance of the wire M_b is $C_{\rm total} = C_{\rm af} + 2C_{\rm couple}$. The first term on the righhand side of (2) models bottom plate-to-ground flux, which is simply the plate-to-plate capacitance. The second term and the third term model the upper surface and side-wall flux contributions, respectively; in both terms, that the flux reduces with reduced S is because more coupling flux is attracted to the adjacent electrode M_c and M_a.

B. Parallel Lines Between Two Planes

As shown in Fig. 1(b), the thicknesses of top dielectric layer and bottom dielectric layer are denoted by H_1 and H_2, respectively. The range of dimension is as in the previous case, except that $0.16 < H_1 < 2.71$ and $0.16 < H_2 < 2.71$. By similar rational function approach and similar reasoning as before, $C_{\rm couple}$ is modeled to simulate the side-wall flux and upper and lower planes' flux. $C_{\rm af}$ is modeled to simulate the upper and lower surface flux and the side-wall flux. Again, using least-square fitting, we have

$$\begin{aligned}\frac{C_{\rm couple}}{\epsilon_{\rm ox}} &= 1.4116\frac{T}{S}\exp\left(-\frac{2S}{S+8.014H_1} - \frac{2S}{S+8.014H_2}\right) \\ &\quad + 1.1852\left(\frac{W}{W+0.3078S}\right)^{0.25724} \\ &\quad \cdot \left\{\left(\frac{H_1}{H_1+8.961S}\right)^{0.7571} + \left(\frac{H_2}{H_2+8.961S}\right)^{0.7571}\right\} \\ &\quad \times \exp\left(-\frac{2S}{S+3(H_1+H_2)}\right)\end{aligned} \tag{3}$$

and

$$\begin{aligned}\frac{C_{\rm af}}{\epsilon_{\rm ox}} &= \left(\frac{W}{H_1} + \frac{W}{H_2}\right) \\ &\quad + 2.04\left(\frac{T}{T+4.5311H_1}\right)^{0.071}\left(\frac{S}{S+0.5355H_1}\right)^{1.773} \\ &\quad + 2.04\left(\frac{T}{T+4.5311H_2}\right)^{0.071}\left(\frac{S}{S+0.5355H_2}\right)^{1.773}.\end{aligned} \tag{4}$$

Again, $C_{\rm total} = C_{\rm af} + 2C_{\rm couple}$.

C. Model Validation

The accuracy of our capacitance model is verified by numerical solutions from Raphael [1] and measured data. We also include results from Sakurai's analytic model [2], [5] for comparison. Fig. 2(a)

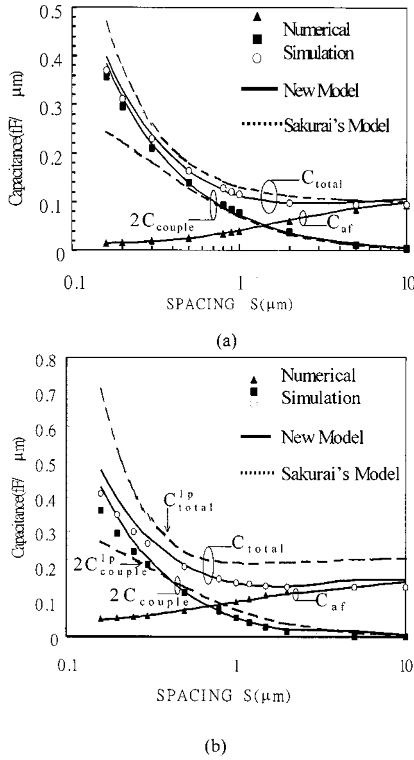

Fig. 2. (a) Verification of model accuracy of various capacitance components [(1)–(2)]; symbols: Raphael, solid line: our model, dashed line: model in [2]. $W = 0.2\,\mu$m, $T = 0.64\,\mu$m, $H = 0.89\,\mu$m. (b) Verification of model accuracy of various capacitance components [(3)–(4)]; symbols: Raphael, solid line: our model, dashed line: calculated by adding up the one-plane model based on formula in [2]. $W = 0.5\,\mu$m, $T = 0.64\,\mu$m, $H_1 = H_2 = 0.89\,\mu$m.

gives the comparison results for wires on one plane. The accuracy of $C_{\rm couple}, C_{\rm af}$ and the interaction between them are observed, and improvement of our model over Sakurai's model [2], [5] is demonstrated. The comparison of our model for wires between two planes with Raphael is shown in Fig. 2(b). The maximum errors here are 7.4% and 12.3% for Fig. 2(a) and (b), respectively. Note that in Fig. 2(b), $C^{1p}_{\rm couple}$ denotes the coupling capacitance obtained from Sakurai's model [2], and $C^{1p}_{\rm total}$ is the value by adding up the capacitances to top plate and to bottom-plate calculated using Sakurai's model [2]. The root-mean-square error (rmse) for $C_{\rm af}$ $(C_{\rm couple})$ is 3.68% (4.45%) and 1.05% (16.13%) for one- and two-plane cases, respectively. The number of data points used in calculating the root mean square error is 627.

Our model is further compared with measured data, and the results are shown in Table I. Five dies have been measured per wafer for sixwafers, and the typical die around the distribution mean was used for comparison. Test structures were fabricated in two technologies: 1) a 0.5-μm twin-well CMOS with SOG plannarized three-level metals and 2) a 0.35-μm twin-well CMOS with chemical mechanical polished (CMP) three-level metals. All dielectric thicknesses used in model calculation are measured from large-plane capacitors on the same die as measured structures for accurate reflection of dielectric constant and dielectric thickness H. This thickness H is used for calculating all capacitance structures. The large-plane capacitors have been placed close to other capacitance structures in test key to eliminate intradie dielectric thickness variations. Wire width W, interwire spacing S, and wire thickness T are determined from SEM bars of small interwire spacing on the same wafer. The small spacing between SEM bars

TABLE I
COMPARISON OF CAPACITANCE MODEL WITH MEASUREMENT DATA.

Structure/Process	Model (10^{-12} Farad)	Measured (10^{-12}Farad)	Dimension parameters(μm)
M2-M1-poly, structure-2/0.5μm	16.14	18.31	{W,S,T,H$_1$,H$_2$}= {0.79, 0.71, 0.63, 0.717}
M1-poly-field, structure-2/0.5μm	17.45	17.52	{W,S,T,H$_1$,H$_2$}= {0.805, 0.695, 0.63, 0.378, 0.717}
M1-field, structure-1/0.35μm	7.741	8.176	{W,S,T,H}= {1.032, 0.685, 0.969, 1.023}
M3-M2-M1, structure-2/0.35μm	19.77	19.55	{W,S,T,H$_1$,H$_2$}= {0.501, 0.776, 0.49, 0.737, 0.793}
M2-M1-Field, structure-2/0.35μm	10.72	11.27	{W,S,T,H$_1$,H$_2$}= {0.50, 0.99, 0.776, 1.02, 0.737}

guarantees that horizontal dimension in dense array is adopted for capacitance calculation. All measurements are executed using a HP4284 impedance meter at 100 kHz, with all parasitic effects canceled using an open-pad calibration structure. Good agreement is observed, and this further demonstrates the accuracy of our capacitance model.

III. DELAY AND CROSSTALK MODEL

Our delay model is based on the circuit schematic diagram shown in Fig. 1(c), where two lines of length L in the same layer run in parallel, with each line being modeled by a distributed *RC*-line. These two lines couple via the coupling capacitance $C_{\rm couple}$ per unit length. $C_{\rm af}$ is the unit-length line-to-ground capacitance of each line.

Let V_1 and V_2 denote the signals propagating on first and second line, and let r_1 and r_2 be the unit-length resistance of the first and second line. Applying step function input E_1 to the first line and with input of the second line being grounded, we analyze the signal at the end of the first line as the signal delay and at end of the second line as the crosstalk noise.

Let $C'_{\rm af} = C_{\rm af}L, C'_{\rm couple} = C_{\rm couple}L$, and $R = r_1 L = r_2 L$. From the maxwell equations of [5], we have at $x = L$

$$\frac{V_1(L,t)}{E_1} = 1 + \frac{K_{11}}{2}\exp\left(-\frac{\sigma_{11}t}{RC'_{\rm af}}\right) + \frac{K_{12}}{2}\exp\left(-\frac{\sigma_{12}t}{RC'_{\rm af} + 2RC'_{\rm couple}}\right) \tag{5}$$

$$\frac{V_2(L,t)}{E_1} = \frac{K_{11}}{2}\exp\left(-\frac{\sigma_{11}t}{RC'_{\rm af}}\right) - \frac{K_{12}}{2}\exp\left(-\frac{\sigma_{12}t}{RC'_{\rm af} + 2RC'_{\rm couple}}\right) \tag{6}$$

where $\sigma_{11} = 1.04/(R_T + C_{T11} + R_T C_{T11} + (2/\pi)^2)$, $\sigma_{12} = 1.04/(R_T + C_{T12} + R_T C_{T12} + (2/\pi)^2)$, $K_{11} = (-1.01(R_T + C_{T11} + 1))/(R_T + C_{T11} + (\pi/4))$, $K_{12} = (-1.01(R_T + C_{T12} + 1))/(R_T + C_{T12} + (\pi/4))$, $R_T = R_S/R, C_{T11} = C_L/C'_{\rm af}$ and $C_{T12} = C_L/(C'_{\rm af} + 2C'_{\rm couple})$ [5].

Note that in theory, one should have $V_1(L,0) = V_2(L,0) = 0$ at $t = 0$. The forms in (5)–(6) actually give a small deviation from zero, which is induced by the approximations in obtaining $\sigma_{11}, \sigma_{12}, K_{11}$ and K_{12}. This initial deviation does not affect the final results, as it matters only when the signals have been propagated to the end of line.

Here, the equations of (5)–(6) are based on a simplified two-line structure. This is intended to provide sufficient physical modeling in its simplest form. To consider three (or more) lines, one will end up with a set of three (or more) partial differential equations with three (or more) unknowns. To simplify such a set of differential equations to

make it solvable as in (5) –(6), one in general needs to make the assumption that the signals on two successive even (or odd) numbered lines are the same, which can essentially reduce to our two-line model. The general situation with more lines can only complicate the analysis matter, giving no explicit concrete information. Our two-line approximation is effective, as it will give simple closed-form solutions, and is directly applicable in at least two applications. 1) Assuming that the M_b is the active line and M_c is the victim line, our result is directly applicable when M_a has the same signal with M_b, hence the signal flow to M_a can be eliminated. 2) When both M_a and M_c are quiet victim lines, our model can be applied by simply modifying C_{couple} to $2C_{\text{couple}}$, which approximates the signl on the forth line next to M_c being similar to that on M_b.

To solve (5), set $x = \exp(-(\sigma_{11}t/RC'_{\text{af}})), \alpha = C_{\text{af}}/(C_{\text{af}} + 2C_{\text{couple}})(\sigma_{12}/\sigma_{11})$ and $a = 2((V_1/E_1) - 1)$, and we rewrite (5) as $K_{12}x^{\alpha} + K_{11}x = a$, whence $x = ((a - K_{11}x)/K_{12})^{1/\alpha} = (a/K_{12})^{1/\alpha}(1 - (K_{11}x/a))^{1/\alpha}$. Since $0 < x < 1$ and $0 < \alpha < 1$, it follows that $0.5^{1/\alpha} < x/a < 0.5$, and $(1 - (K_{11}x/a))^{1/\alpha}$ can be well approximated by a first order polynomial using Taylor's expansion, i.e. $x = (a/K_{12})^{1/\alpha}(1 - (K_{11}x/a))^{1/\alpha} \approx (a/K_{12})^{1/\alpha}(1 - (K_{11}/\alpha)(x/a))$, whence x is solved as $x = (a/K_{12})^{1/\alpha}(1 + ((a/K_{12})^{1/\alpha}K_{11})/\alpha a)^{-1}$. The delay time for $V_1(t)$, denoted by t_d, which is to rise to $0.9E_1$, is simply

$$t_d = -\frac{RC_{\text{af}}L}{\sigma_{11}} \ln\left(\frac{\frac{a}{K_{12}}^{\frac{1}{\alpha}}}{1 + \frac{\frac{a}{K_{12}}^{\frac{1}{\alpha}}K_{11}}{\alpha a}}\right). \tag{7}$$

The time for peak crosstalk noise on the adjacent wire, denoted by t_p, can be obtained by solving the equation $(dV_2(L,t))/dt = 0$ in (6), with

$$t_p = -\frac{RC_{\text{af}}L}{\sigma_{11}} \ln\left(\frac{\alpha K_{12}}{K_{11}}^{-\frac{1}{\alpha-1}}\right). \tag{8}$$

The peak crosstalk noise V_p on the adjacent wire is given by (6) with $t = t_p$, i.e.

$$V_p = \frac{E_1}{2}\left\{K_{11}\exp\left(-\frac{\sigma_{11}t_p}{RC'_{\text{af}}}\right) - K_{12}\exp\left(-\frac{\sigma_{12}t_p}{R(C'_{\text{af}} + 2C'_{\text{couple}})}\right)\right\}. \tag{9}$$

To examine the accuracy of the models developed above, we calculate interconnect lines as a distributed *RC* delay line. We divide the delay line into 20 sections. Coupling and area-fringe capacitances of the lines, C_{couple} and C_{af}, are obtained from our capacitance model of Section II, and resistance of each line section is proportional to the inverse of cross-section area and to the length of each section, with resistivity of 0.025 $\Omega\mu$m. The accuracy of our delay and crosstalk model is demonstrated in Fig. 3(a), (b), with comparison with SPICE simulations. Good agreement is shown.

Note that R_s in Fig. 1(c) in the active-line transistor and victim-line transistor should in general be diffenent. This may cause some tedius calculations in the derivations above. However, during the initial period of charging process, both transistors are dominated by the PMOS resistance in the saturation region. Thus, for that period, the use of the same resistance R_s in active and victim lines is a reasonable approximation.

Here, we use a step input model in deriving the delay and crosstalk. The work of [8] gave a different interconnect model with a ramp input.

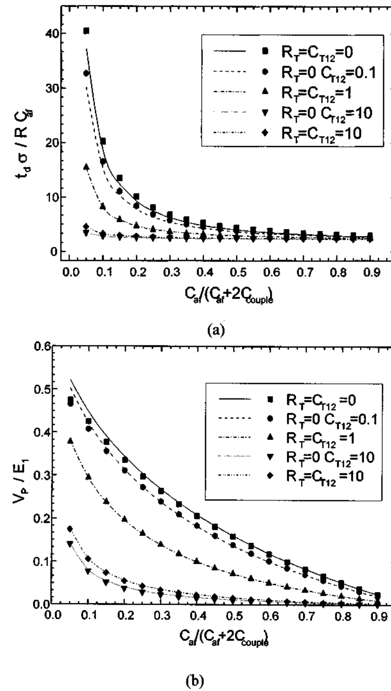

Fig. 3. (a) Model accuracy of *RC* line delay model. (b) Model accuracy of *RC* line crosstalk model.

The model developed here can also easily extend to cover the case with a ramp input via similar derivaitons.

IV. Conclusion

Accurate closed-form models have been developed for wire capacitance, wire delay and crosstalk noise. The capacitance model gives line-to-line and line-to-ground capacitances separately, and lead to precise delay and crosstalk estimations. The delay and crosstalk formulas allow for simple analytic prediction of interconnection performance for arbitrary interconnect dimensions. Our model is useful for VLSI design and process optimization.

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