A CMOS Delta–Sigma True RMS Converter

Wei-Shinn Wey and Yu-Chung Huang

***Abstract*—Conventionally, monolithic electronics true rms converters are constructed by bipolar circuitry. This paper describes a new architecture based on delta–sigma ($\Delta\Sigma$) modulation to realize a low-cost rms converter in CMOS technologies, especially intended for handheld digital multimeters. The signal-to-quantization noise ratio as well as transfer characteristics of this architecture have been deduced to obtain initial design parameters. The use of an indirect charge transfer technique makes the converter gain depend only on an on-chip capacitor ratio, reducing gain drift and offering good gain accuracy. Measured results show that this converter achieves a signal-to-noise ratio of 88 dB and a relative error of $\pm 0.2\%$ for arbitrary inputs with a signal crest factor up to three. The signal bandwidth exceeds 50 kHz, and the full-scale input range is greater than 0.4 V_{rms}. Without trimming and calibration, this converter has an absolute gain error less than $\pm 0.4\%$. This chip is fabricated in a 0.8-μm double-poly, double-metal CMOS process and occupies active area of 1 mm^2.**

***Index Terms*—CMOS analog integrated circuits, delta–sigma modulation, indirect charge transfer filter, multiplier-divider, rms-to-dc converter, switched-capacitor circuits, true rms converter.**

I. Introduction

THE root-mean-square (rms) value of arbitrary signals is one of the important parameters in electronics measurements, especially for digital multimeters (DMM's). With the great progress of VLSI technologies, most circuitry of a handheld DMM has been integrated into a single CMOS chip except an rms converter. Therefore, to integrate a CMOS rms converter into a DMM chip tends to be urgent.

A few DMM's use a simple rectifier and an averaging circuit for ac measurements. These meters have to be calibrated to read the rms value, but this is correct only for a specified waveform. In contrast to the averaging circuit, true rms converters compute the rms value of a signal regardless of waveform. To realize this rms converter, we have two alternative methods: comparing and computing. The comparing method, based on a thermal principle [1] or an electrostatic principle [2], has offered a wide bandwidth and good accuracy, but this method requires extra processing steps and complex packages, resulting in high-cost converters. The computing method is based on analog signal processing or digital signal processing. Although the analog processing method using translinear property of bipolar circuitry has led to elegant solutions [3]–[5], these converters are difficult to implement in standard CMOS processes. In addition, because an averaging capacitor appears across a based-emitter junction whose resistance varies with signal level, the response time increases linearly as the input signal is reduced [6]. Therefore, the response time especially for a decreasing input is also an important issue in the bipolar converters. Furthermore, in the digital processing method [7], the rms value of an input signal is calculated by a digital computation unit after high-speed analog-to-digital (A/D) conversion. This converter, providing a fast response, is realized in a CMOS process. However, the digital computation unit occupies a large chip area and thus does not lead to a low-cost solution.

The use of delta–sigma $(\Delta\Sigma)$ modulators in both low-pass and band-pass A/D converters has shown promise for coping with the analog component limitations inherent in VLSI technologies. Actually, if we take account of the reference input of a $\Delta\Sigma$ modulator, the output of this modulator can be interpreted as a ratiometric function plus quantization noise. From this point of view, the $\Delta\Sigma$ modulator acts like a divider, and is thus referred to as a $\Delta\Sigma$ divider in this paper. In addition, applying the 1-bit digital output of a $\Delta\Sigma$ divider to control a polarity switch, an analog input signal can be converted to its positive or negative value by this switch so that the polarity switch acts like a multiplier. Furthermore, combining a $\Delta\Sigma$ divider and a polarity switch, a $\Delta\Sigma$ multiplier-divider can be built. Consequently, $\Delta\Sigma$ true rms converter-based nonlinear analog signal processing can be constructed from the $\Delta\Sigma$ multiplier-divider [8].

In this paper, we describe a CMOS $\Delta\Sigma$ true rms converter for a low-cost integration in a handheld DMM chip. A new architecture using $\Delta\Sigma$ modulation for realizing a CMOS rms converter is presented in Section II. Transfer characteristics and signal-to-quantization noise ratio (SQNR) of the architecture have been deduced to obtain initial design parameters. In Section III, performance limitations in measurements, including crest factor, noise, linearity, and response time, are investigated to get design criteria. In Section IV, an indirect-charge-transfer (IDCT) filter for realizing an ultralarge time-constant (ULT) is designed to make the converter gain depend only on an on-chip capacitor ratio. Due to the excellent stability and good matching properties of poly-poly capacitors in double-poly, double-metal (DPDM) CMOS processes, the converter gain drift is limited and gain calibration is not required. A test chip based on the new idea was successfully realized in a 0.8-μm DPDM CMOS process. Details of the circuit implementation are described in Section V and measured results are shown in Section VI, which demonstrates that the performance of this converter meets the requirement of handheld DMM's.

II. Architecture of True rms Converter

A. $\Delta\Sigma$ Dividers

Fig. 1(a) illustrates a second-order $\Delta\Sigma$ divider, which features a numerator input $x(t)$, a denominator input $w(t)$, a

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quantized output $d(t)$, two summers, two integrators, a 1-bit analog-to-digital converter (ADC), and a digital-to-analog converter (DAC). The denominator input must always be positive. Compared to a conventional $\Delta\Sigma$ modulator [9], the $\Delta\Sigma$ divider has a variable denominator input instead of a constant reference input. The two possible output states of $d(t)$ are, respectively, treated as 1 and -1. The operation of the $\Delta\Sigma$ divider can be analyzed quantitatively by the sampled-data equivalent circuit shown in Fig. 1(b). The 1-bit DAC and the ADC are modeled, respectively, by a multiplier and by an additive quantization noise source $q[n]$ [10]. Since the 1-bit ADC is sensitive only to the sign (not to the magnitude) of its input and is in the negative feedback loop including a multiplier, its additive noise model should be led by a factor of $4/w[n]$. Thus, the divider output can be found by

$$d[n] = \frac{x[n-2]}{w[n]} + \left(q[n] - 2\,\frac{w[n-1]}{w[n]}\,q[n-1] + \frac{w[n-2]}{w[n]}\,q[n-2]\right) \tag{1}$$

which shows a ratiometric function of the delayed numerator input to the denominator input and a difference equation of the quantization noise. It can be observed that the varying denominator makes the zeros of the noise transfer function be no longer at dc, and thus the SQNR of the divider is degraded by the quantization noise leakage in the interested frequency. The more rapidly the denominator varies, the more crucial the SQNR degradation becomes. To cope with this degradation, the denominator input should be restricted to vary slowly or its swing should be sufficiently small. Furthermore, if the denominator input is limited to be a quasi-static signal, which may vary in time but keeps static in steady state, the divider output can be simplified to

$$d[n] = \frac{x[n-2]}{W} + (q[n] - 2q[n-1] + q[n-2]) \tag{2}$$

where in steady state we have $w[n] = w[n-k] = W$. The modulation noise now becomes the well-known second difference of $q[n]$ [11]. In the rms converter application, the denominator will be fed by a quasi-static signal so that the SQNR degradation as (1) can be ignored and (2) can be used.

It is useful to construct a phase-compensated $\Delta\Sigma$ divider as shown in Fig. 1(c). A loop, referred to as a phase-compensation loop, feeding the numerator directly forward to the second integrator is added to compensate the phase delay resulting from the first integrator. The divider output can consequently be found by

$$d[n] = \frac{x[n-1]}{W} + (q[n] - 2q[n-1] + q[n-2]) \tag{3}$$

and thus the system function of this divider is given by

$$D(z) = \frac{X(z)\cdot z^{-1}}{W} + Q(z)\cdot(1-z^{-1})^2. \tag{4}$$

Compared to a conventional second-order $\Delta\Sigma$ modulator [9], the quantization step size (referred to as Δ) of two should be

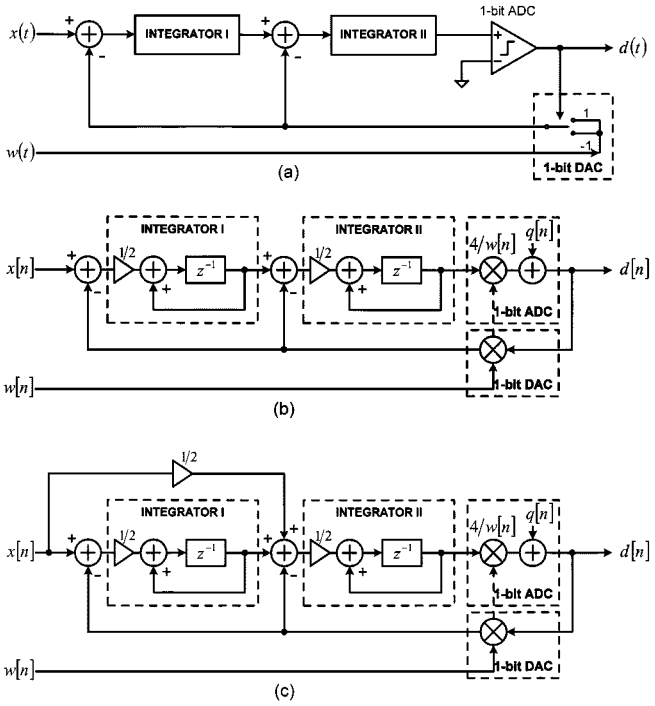


Fig. 1. Second-order $\Delta\Sigma$ divider. (a) Block diagram, (b) sampled-data equivalent circuit, and (c) phase-compensated sampled-data circuit.

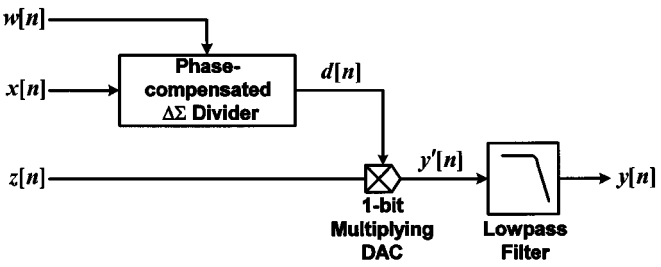


Fig. 2. Block diagram of $\Delta\Sigma$ multiplier-divider.

taken since the 1-bit output of the divider is treated as ± 1. Therefore, the spectral density of the modulation noise in (3) can be given by

$$N(f) = Q(f)|1 - e^{-j2\pi f\tau}|^2 = 2\sqrt{\frac{\tau}{3}}\,\sin^2(\pi f\tau) \tag{5}$$

where τ is the sampling period.

B. $\Delta\Sigma$ Multiplier-Divider

A $\Delta\Sigma$ multiplier-divider is shown in Fig. 2. Depending on the divider's output $d[n]$ as 1 or -1, the multiplicand input $z[n]$ is converted to $z[n]$ or $-z[n]$ by the 1-bit multiplying DAC. In steady state, the DAC output $y'[n]$ can be given by

$$y'[n] = \frac{x[n-1]\cdot z[n]}{W} + (q[n] - 2q[n-1] + q[n-2])\cdot z[n]. \tag{6}$$

It appears to be a multiplication-division function of the inputs $x[n]$, $z[n]$, and W and an intermodulation function of $z[n]$ and the shaped quantization noise. If the input $z[n]$ contains any high-frequency component, the intermodulation yields important in-band noise components that will degrade the SQNR.

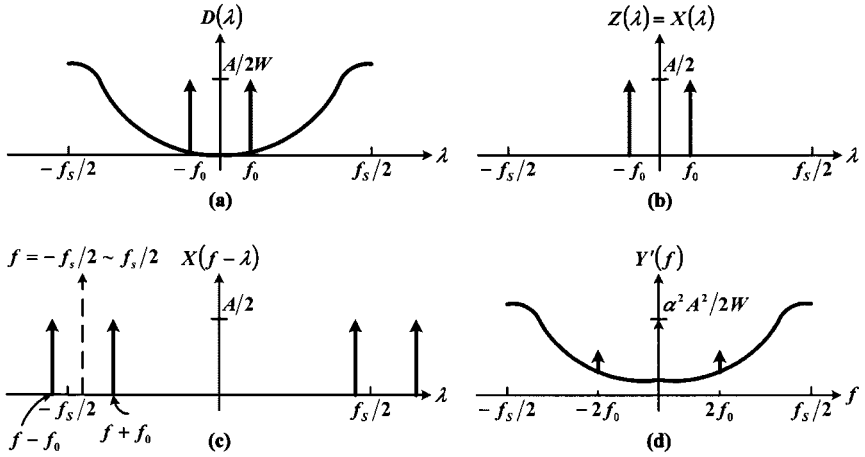


Fig. 3. Amplitude spectrum of the periodic convolution for the $\Delta\Sigma$ multiplier-divider. (a) Divider output. (b) Numerator and multiplicand inputs. (c) Mirrored and shifted spectrum of input $x[n]$. (d) Multiplier-divider output.

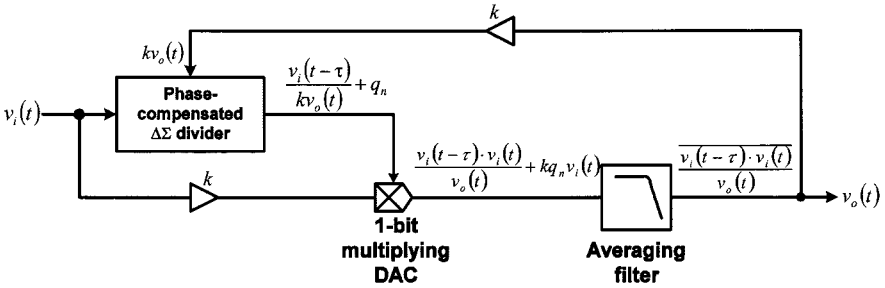


Fig. 4. Block diagram of the $\Delta\Sigma$ true rms converter.

Therefore, $z[n]$ should be restricted to be a band-limited signal to prevent this degradation.

In the rms converter application, the inputs $x[n]$ and $z[n]$ both are connected to a signal input so that $z[n] = x[n]$. Thus, the spectral density of $y'[n]$ can be found by

$$Y'(f) = \frac{1}{f_s} \int_{-f_s/2}^{f_s/2} D(\lambda)X(f-\lambda) \cdot d\lambda \tag{7}$$

which corresponds to a periodic convolution. Assuming that $x[n]$ is a sinusoidal input with frequency f_0 and amplitude A, the periodic convolution can be interpreted by Fig. 3(a)–(d). Plugging (4) and (5) into (7), the amplitude spectrum of $y'[n]$ can be found by

$$\begin{aligned} |Y'(f)| \approx & \frac{A^2}{2W} \cdot \cos(2\pi f_0 \tau) \\ & \cdot \left[\delta(f) + \frac{\delta(f+2f_0)}{2} + \frac{\delta(f-2f_0)}{2}\right] \\ & + 4A\pi^2\tau^2 \sqrt{\frac{\tau}{3}} \cdot (f^2 + f_0^2). \end{aligned} \tag{8}$$

If the 3-dB frequency of the low-pass filter is far less than the signal frequency so that $f_{3\,\mathrm{db}} \ll f_0$, the amplitude spectrum of $y[n]$ then can be given by

$$|Y(f)| \approx \frac{A^2}{2W} \cos(2\pi f_0 \tau) + 4A\pi^2\tau^2 f_0^2 \sqrt{\frac{\tau}{3}}. \tag{9}$$

This equation will be used to obtain the SQNR of the $\Delta\Sigma$ rms converter.

C. $\Delta\Sigma$ trms Converter

As shown in Fig. 4, the proposed true rms (trms) converter is constructed from a $\Delta\Sigma$ multiplier-divider. The averaging filter has a very low 3-dB frequency to filter out all of the ac terms so that the filter's output is an average response of its input. In ac measurements, a crest factor (CF) can be used to distinguish different waveforms having the same rms value. A crest factor is defined as the ratio of the peak signal amplitude to the rms amplitude (so that $\mathrm{CF} = \mathrm{V_{PEAK}}/\mathrm{V_{rms}}$),, and it is always equal to or larger than one. Thus, to prevent the divider from overload, a gain factor k ($k > 1$) is placed on the feedback loop to keep the denominator of the divider always larger than the numerator. In addition, the multiplicand input is also scaled by the same factor k to compensate the attenuated converter gain due to the feedback scaling. Therefore, the conversion accuracy is still maintained while measuring an input signal with a crest factor up to k. The converter output $v_o(t)$ can be found by

$$v_o(t) = \sqrt{\overline{v_i(t-\tau)v_i(t)}} \approx \alpha\sqrt{\overline{v_i^2(t)}}. \tag{10}$$

A true rms conversion is achieved where α results from the signal delay of the divider and slightly depends on input waveforms. For a sinusoidal input with signal frequency f_0, α is given by

$$\alpha = \sqrt{\cos(2\pi f_0 \tau)} \tag{11}$$

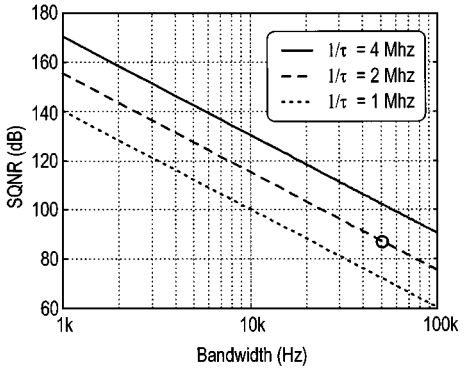


Fig. 5. SQNR plot of a second-order $\Delta\Sigma$ rms converter with a gain factor of three.

and the SQNR of this rms converter can be deduced from (9) and by

$$\mathrm{SQNR}_{\mathrm{trms}} = \frac{\alpha\sqrt{2}}{8k\pi^2\tau^2 f_0^2\sqrt{\tau/3}} \tag{12}$$

which depends only on the signal frequency regardless of the signal level, in contrast to $\Delta\Sigma$ modulators [9], [10], whose maximum SQNR is achieved only while the modulator accommodates its largest input level. A plot of SQNR versus signal bandwidth of this converter is illustrated in Fig. 5.

III. Limitations of Measurement Performance

A. Crest Factor

A true rms converter computes the rms value of a signal with arbitrary waveforms. Waveforms differ in their crest factors. In this converter, a gain factor of k can be designed to make the converter have the ability to accommodate an input signal having a crest factor of k. However, taking a high gain factor enlarges the signal range of the operational amplifiers (op-amps) in the divider and degrades the SQNR of the converter from (12), resulting in sacrificing of the dynamic range. Consequently, to measure a greater crest factor signal or to obtain a larger converter dynamic range becomes a tradeoff. In this design, a gain factor k of three is taken to maintain superior conversion accuracy for an input signal with crest factor up to three.

B. Noise

Output noise of the rms converter restricts the smallest measurable input change of an ac measurement, which refers to the least-significant digit (LSD) of a meter's display. A typical display resolution of a handheld DMM is 4000 counts, resulting in a required rms converter that should have 100 $\mu\mathrm{V}_{\mathrm{rms}}$ LSD and 400 $\mathrm{mV}_{\mathrm{rms}}$ full-scale input range. This corresponds to an output noise of 16 $\mu\mathrm{V}_{\mathrm{rms}}$ to provide a noise-free indication. The sources of noise in the rms converter are twofold: 1) device noise generated in all MOS transistors and resistors and 2) quantization noise produced by the $\Delta\Sigma$ divider.

The two most important sources of device noise are flicker noise and thermal noise. Flicker noise generated by the MOS transistors can be removed to out of the signal band by using chopper op-amps [12]. Thermal noise, of the MOS transistors in op-amps and of the on-resistance of the sampling switches, can be made insignificant in the rms converter due to a very high oversampling ratio [13]. For example, assume that a 3-dB frequency of an averaging filter at $f_{3\,\mathrm{dB}} = 5$ Hz and a sampling frequency at $f_s = 2$ MHz has an oversampling ratio of 200 000. Such a high oversampling ratio makes the in-band thermal noise far less than 16 $\mu\mathrm{V}_{\mathrm{rms}}$, even for a sampling capacitor of 0.1 pF.

Therefore, the output noise is dominated by quantization noise. Since the rms converter has the same SQNR for different input levels, a larger input signal will induce a greater quantization noise. From (12) and Fig. 5, if a sampling frequency at 2 MHz and a signal bandwidth of 50 kHz are taken, an SQNR of 88 dB can be obtained. Assuming a full-scale input level of 400 $\mathrm{mV}_{\mathrm{rms}}$, the converter will have an output quantization noise of 16 $\mu\mathrm{V}_{\mathrm{rms}}$.

C. Linearity

Since the robustness of $\Delta\Sigma$ modulators against circuit imperfections has been proved in many other applications, linearity of the rms converter will be limited by component offsets and the 1-bit DAC with averaging filter. Component offsets usually do not introduce nonlinear distortion in most other applications, but they do in the rms converter due to the nonlinear feedback to the divider's denominator input. Referring to Fig. 4, the input-referred offsets of the numerator and the denominator of the divider are assumed to be V_{OS1} and V_{OS2}, respectively, and that of the averaging filter is V_{OS3}. The input signal is expressed as a combined signal of V_{dc} and $V_{\mathrm{ac}}(t)$ so that

$$v_i(t) = V_{\mathrm{dc}} + v_{\mathrm{ac}}(t). \tag{13}$$

Then the output $v_o(t)$ can be found by (14), shown at the bottom of the page. In pure ac measurements $(V_{\mathrm{dc}} = 0)$,, the offset voltage V_{OS1} is modulated into the ac band and hence is filtered out by the averaging filter. In contrast to V_{OS1}, the offset voltages V_{OS2} and V_{OS3} induce nonlinear distortion in all measurements. It can be found that the nonlinear distortion becomes crucial for low-level input signals. Offset sources in switched-capacitor (SC) circuits are op-amps and charge injections from MOS switches. These offsets can be reduced by using chopper op-amps and fully differential configuration, respectively. However, residual offset [14] still remains and thus limits the linearity of this converter.

Furthermore, the linearity performance of the 1-bit multiplying DAC with averaging filter also plays an important role to

$$v_o^2(t) = \frac{V_{\mathrm{OS2}} - V_{\mathrm{OS3}} + \sqrt{(V_{\mathrm{OS2}} + V_{\mathrm{OS3}})^2 + 4V_{\mathrm{OS1}}V_{\mathrm{dc}} + 4\overline{v_i^2(t)}}}{2}. \tag{14}$$

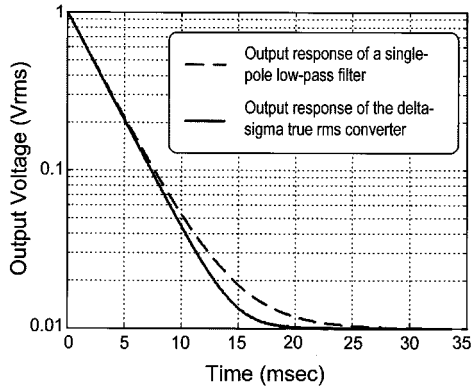


Fig. 6. Simulated output response versus predicted single-pole, low-pass filter's output response.

make this converter have good linearity. Several circuits to implement $\Delta\Sigma$ audio DAC's have been revealed and explored by [15]. Due to lower sensitivity for clock jitter, it has been proved that circuitry based on charge packet transformation has superior performance over others [16]. However, comparing with a postfilter for audio DAC's, the averaging filter for rms converters has two more severe requirements: much lower 3-dB frequency and good gain stability. This will be discussed in the next section.

D. Response Time

The response time of the rms converter is limited by the averaging filter with ultralarge time constant. While a step signal is applied to the input of a single-pole filter with a 3-dB frequency $f_{3\,\mathrm{dB}}$, the time needed for the output to reach a final value to within a specified tolerance E can be given by

$$T_{RS} = \frac{\ln(E)}{2\pi f_{3\,\mathrm{db}}}. \tag{15}$$

Fig. 6 shows a simulated output response of the proposed rms converter with a 50-Hz filter applied by a step-decreasing signal from 1 V_{rms} to 10 mV_{rms}, which is faster than that of a 50-Hz single-pole, low-pass filter. It can be found that the response time of this converter can be roughly estimated by (15). In a digital rms converter, the response time is restricted by a mean-squared filter with a low 3-dB frequency. For example, if the specified tolerance and 3-dB frequency are 0.005% and 3.5 Hz, respectively, from (15), the response time can be estimated to be 0.45 s, which is close to the time (0.42 s) depicted in [7]. Therefore, the response time of a delta–sigma rms converter is comparable to that of a digital one.

IV. Ultralarge Time Constant SC Filters

To filter out all of the ac terms including the harmonics due to multiplication as well as the quantization noise, the 3-dB frequency of the averaging filter should be low enough (e.g., 5 Hz) in the rms converter. In addition, to obtain a sufficient high oversampling ratio, the sampling frequency has to be much higher (e.g., 2 MHz) than the signal bandwidth. The two demands lead the averaging filter to have an ultralarge time-constant and the required capacitor spread to run into hundreds of thousands

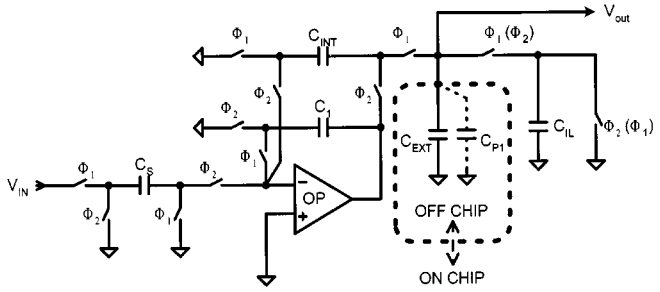


Fig. 7. Indirect charge transfer averaging filter.

(e.g. 400 000), resulting in a prohibitively large area requirement. Some very large time-constant (VLT) SC filters have been proposed [17], [18]. The required capacitor spread has been reduced to its square-root value, but these VLT filters still cannot serve for this spread requirement of hundreds of thousands. A previous design [19] aimed at the same goal uses external resistors and capacitors to realize a ULT filter [20]. However, the converter gain in this work depends not only on a capacitor ratio but also on a sampling frequency, resistance value, and capacitance value. Due to the different temperature coefficients between the capacitors and the resistors, the gain drift becomes a crucial issue. Moreover, the tolerance of the absolute value of capacitance in VLSI technologies is usually above $\pm 10\%$; thus, gain calibration is indispensable to the previous work.

In CMOS technologies, the accuracy of capacitor ratio better than 0.1% can be performed by unit and common-centroid capacitor layouts [21]. Besides, the temperature stability of a capacitor ratio achieving 2 ppm/°C has been shown by a transducer ADC [13]. Thus, it is preferred to construct an averaging filter whose dc gain depends only on a capacitor ratio in this application.

The approach taken here is to use an indirect charge transfer technique, demonstrated by Fig. 7. During the Φ_2 phase, a charge packet of the magnitude of $+V_{\mathrm{in}}C_S$ is delivered to an integrating capacitor C_{INT}. In Φ_1 phase, capacitors C_{INT} and C_{EXT} are connected in parallel with each other, and hence the charge on C_{INT} and C_{EXT} redistributes across the parallel combination. Since the capacitance of the external capacitor C_{EXT} is usually far greater than that of C_{INT}, most of the charge on C_{INT} flows into C_{EXT}. That is, the charge packet sampled on C_S is indirectly transferred to C_{EXT} via C_{INT}. A capacitor C_1 serves as a voltage source, so the op-amp output does not have to move much during this phase. Besides, an internal load capacitor C_{IL} is charged to the voltage V_{out} during Φ_1 (or Φ_2) phase and is discharged to ground voltage Φ_2 (or Φ_1) phase, respectively. Thus, the transfer function of the IDCT filter can be derived by

$$H(z) = \frac{V_{\mathrm{OUT}}(z)}{V_{\mathrm{IN}}(z)} = \frac{C_S}{C_{\mathrm{IL}}} \times \frac{z^{-1}}{1 + \dfrac{C_{\mathrm{EXT}} + C_{P1}}{C_{\mathrm{IL}}} \cdot (1 - z^{-1})} \tag{16}$$

whose dc gain and 3-dB frequency are, respectively, given by

$$H(1) = \frac{C_S}{C_{\mathrm{IL}}} \tag{17}$$

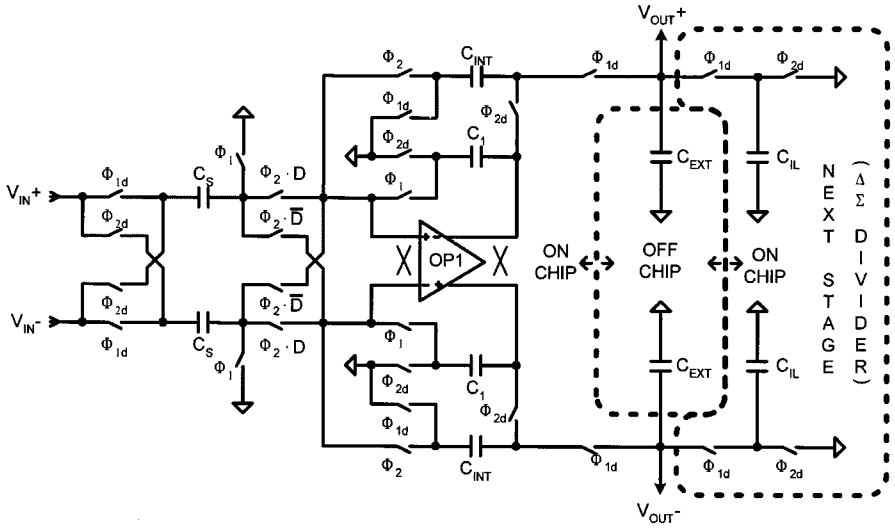


Fig. 8. Fully differential 1-bit multiplying DAC with an IDCT filter.

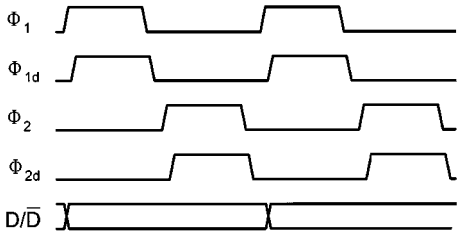


Fig. 9. Clock timing diagram.

and

$$f_{3\,\mathrm{dB}} \approx \frac{f_S C_{\mathrm{IL}}}{2\pi C_{\mathrm{EXT}}} \tag{18}$$

where $C_{\mathrm{EXT}} \gg C_{P1}$. A dc gain depending only on an on-chip capacitor ratio is performed.

V. Circuit Implementation

A fully differential configuration is used in the implementation to not only maximize dynamic range but also suppress common-mode noise such as digital noise coupling through the common substrate and power lines. This also leads to a first-order cancellation of the charge injection offsets from switches, having another benefit of reducing the low-level signal distortion as seen in (14). The common-mode feedback (CMFB) for each fully differential op-amp is provided by a SC dynamic CMFB circuit, which has an advantage of consuming minimum power [22].

A 1-bit multiplying DAC with the averaging filter can be built by combining the IDCT filter with 1-bit multiplying switches controlled by the digital input signal D, as shown in Fig. 8. The control clock is a nonoverlap two-phase clock, as illustrated in Fig. 9. Both delayed clock phase $\Phi_{1\mathrm{d}}$ and $\Phi_{2\mathrm{d}}$ are taken to make charge injection errors from CMOS switches become signal-independent [23]. During the Φ_1 phase, the input voltage is sampled onto the capacitors C_S. During the Φ_2 phase, depending on the 1-bit digital input D's being 1 or -1, the charge packet of the magnitude of either $+2V_{\mathrm{in}}C_S$ or $-2V_{\mathrm{in}}C_S$ is delivered to an integrating capacitor C_{INT}. Since the input V_{in} is sampled two times in each clock cycle, this filter has a dc gain of $2\,C_S/C_{\mathrm{INT}}$. The internal-load capacitors C_{IL} here are the denominator sampling capacitors of the $\Delta\Sigma$ divider stage, and the large capacitors C_{EXT} are off-chip to make the 3-dB frequency low enough. In addition, the op-amp offset is reduced by the chopper-stabilized technique in [12], [14].

Fig. 10 illustrates a schematic of the phase-compensated $\Delta\Sigma$ divider as in Fig. 1(c). Each integrator has a gain coefficient of 0.5, and the op-amp of the first integrator is chopper-stabilized. The numerator input is sampled in both Φ_1 and Φ_2 phases to obtain an additional phase lead of a half of a sampling period. The SC network associated with C_{FW} feeding the input V_{IN} directly forward to the second integrator is designed to compensate the delay resulting from the first integrator. To perform this compensation, the capacitance value of C_{FW} should be half the value of C_D. A complete schematic of the rms converter is shown in Fig. 11, which features the $\Delta\Sigma$ divider as in Fig. 10, the 1-bit multiplying DAC with an IDCT filter as in Fig. 9, a clock generator, and two input buffers. The internal load capacitor C_{IL} of the IDCT filter now is realized by the denominator sampling capacitors C_{IL1} and C_{IL2}. The two chopper-stabilized input buffers are used to offer high input impedance. The output voltage can be found by

$$v_o(t) \approx \alpha \cdot \sqrt{\frac{4C_S C_D}{C_{\mathrm{IL1}}(C_{\mathrm{IL1}} + C_{\mathrm{IL2}})}} \cdot \sqrt{\overline{v_i^2(t)}}. \tag{19}$$

The converter gain depends on a capacitor ratio of C_S, C_D, C_{IL1}, and C_{IL2}, where α slightly depends on input waveforms. For a sinusoidal input, α is identical to (11). Furthermore, it can be found that the response time is signal-level independent, in contrast to bipolar rms converters, which become slower at low input levels.

Since the crest factor is aimed at three, the gain factor k of this converter is given by

$$k = \frac{2C_S}{C_{\mathrm{IL}}} = \frac{C_{\mathrm{IL1}}}{2C_D} = 3. \tag{20}$$

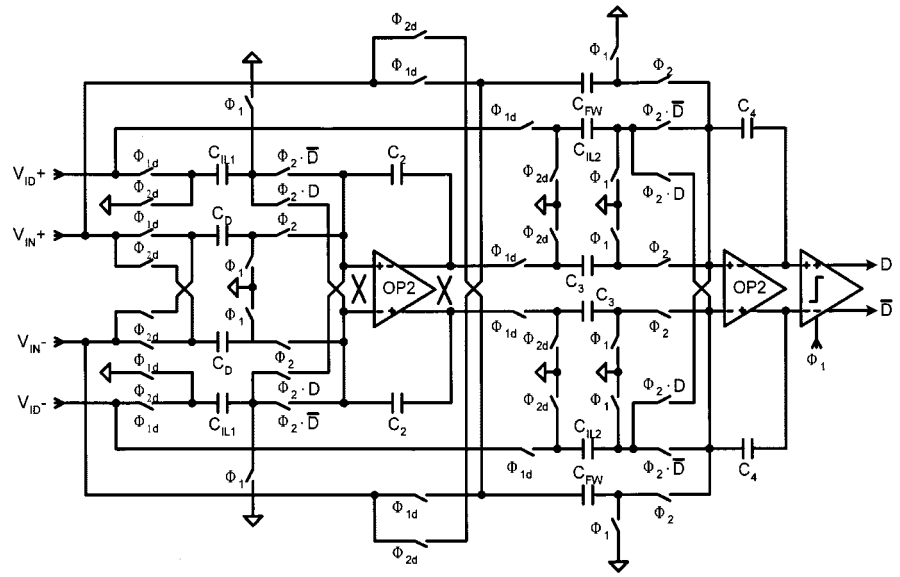


Fig. 10. Fully-differential phase-compensated SC $\Delta\Sigma$ divider.

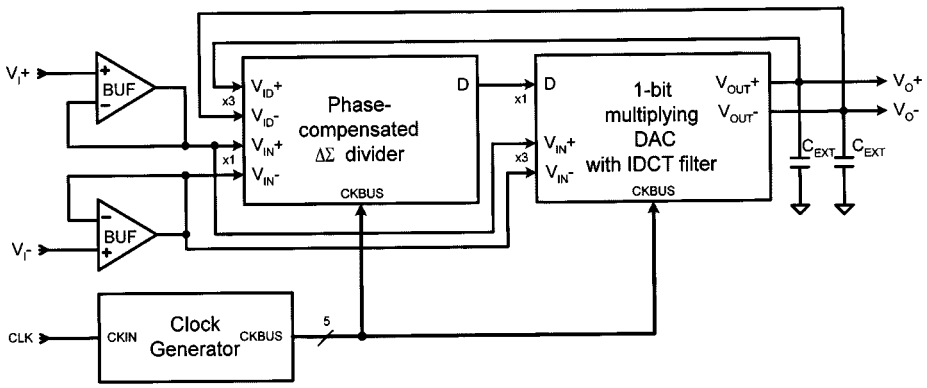


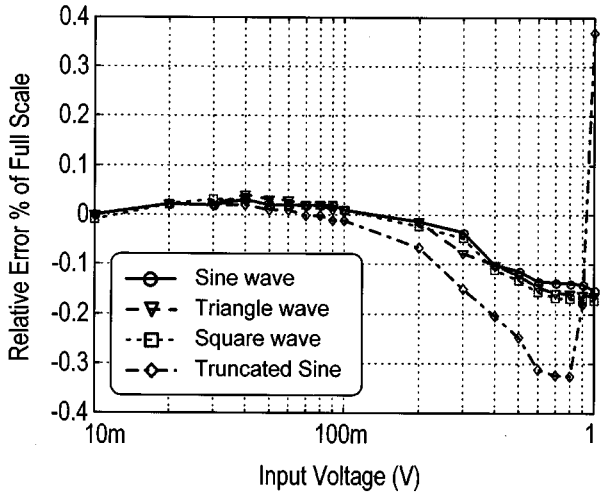
Fig. 11. Complete circuit description of the rms converter.

In a phase-compensated $\Delta\Sigma$ divider, we have $C_D/C_{\rm FW} = 2$, and thus the minimum capacitor is $C_{\rm FW}$. It has been investigated that kT/C noise can be neglected in this converter even for capacitance less than 0.1 pF. Therefore, the capacitor value of $C_{\rm FW}$ is chosen as 0.25 pF, and the other capacitor values can be found by $C_D = 0.5$ pF, $C_{\rm IL1} = C_{\rm IL2} = 3$ pF, and $C_S = 9$ pF. In addition, if the external capacitor is given by $C_{\rm EXT} = 340$ nF, the averaging filter has a 3-dB frequency of 5 Hz, from (18). All of the op-amps are Miller-compensated two-stage class A type [24]. Table I illustrates some important specifications of these op-amps. Because the op-amps BUF and OP1 are directly adopted from another design, the load capacitance (15 and 8 pF) they can drive are greater than the actual capacitance (9.5 and 5 pF, respectively) they should drive in this converter. Therefore, if the two op-amps are redesigned especially for this converter, the current consumption can be reduced.

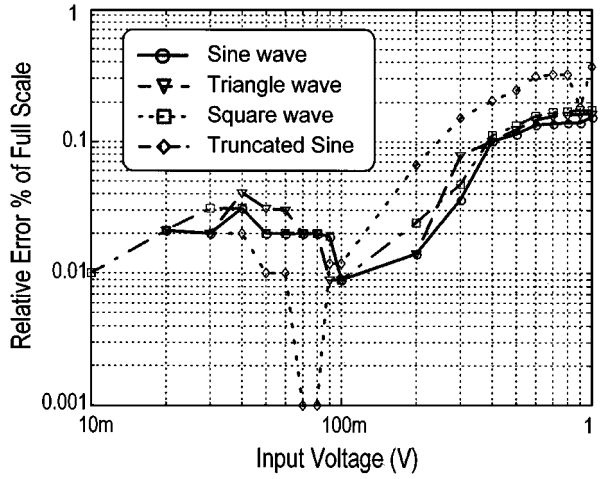
The power consumed in a switched-capacitor circuit is generally proportional to its integrators' loading, and the minimum capacitance that could be used is restricted by kT/C noise. In addition, to measure input signals with crest factor of k leads the required (internal) capacitor spread to be 2 k^2. Consequently, the performance of power consumption is limited by the specified crest factor and dynamic range. Compared to the traditional bipolar or digital converters [4], [7], this converter consumes more power. However, if power consumption becomes a major issue, it can be significantly improved by using a class AB amplifier and dynamic biasing technique [22].

TABLE I
SOME IMPORTANT CHARACTERISTICS OF THE OP-AMPS

Operational Amplifier	BUF	OP1	OP2	
Load capacitance (required)	15 (9.5)	8 (5)	2 (2)	pF
Open-loop gain	75	74	74	dB
Unit-gain frequency	14	30	41	MHz
Unity-gain phase-margin	63	60	65	degree
Slew rate	50	70	50	V/μs
Quiescent Current	1.2	1.8	0.75	mA
Required quantity	2	1	2	na
Load capacitors	C_S+C_D	C_S//C_1	(C_{IL1}+C_D)//C_2	na



(a)



(b)

Fig. 12. Relative error percentage of full scale for 1-kHz various input waveforms. (a) Linear y-axis. (b) Logarithmic y-axis.

VI. Experimental Results

A test chip is fabricated in a 0.8-μm DPDM CMOS process. The converter operates on $\pm$3-V supplies. A plot of relative error versus input levels of 1-kHz signals including sinusoidal wave, triangle wave, square wave, and truncated sine waves is shown in Fig. 12(a). The truncated sine waves have a signal crest factor of 2.41. For the specified full-scale range of 0.4 $V_{\rm rms}$, this converter has a relative error of full scale less than $\pm$0.2%. Besides, to visualize the error at smaller input signals in a better way, another plot is illustrated in Fig. 12(b) whose y-axis is plotted on a logarithmic scale.

In this chip, to observe the performance of the phase compensation, a pair of controllable switches is inserted into the phase-compensation loop of the $\Delta\Sigma$ divider to enable or disable the compensation. Measured frequency responses of this chip are shown in Fig. 13. While the compensation is disabled, the converter gain degrades rapidly for signal frequency greater than 20 kHz, which is very close to the theoretical prediction. In contrast to disabling the compensation, enabling it makes the converter have a flatter response whose gain error is less than $\pm$0.6% with 50-kHz bandwidth. Fig. 14 shows a frequency

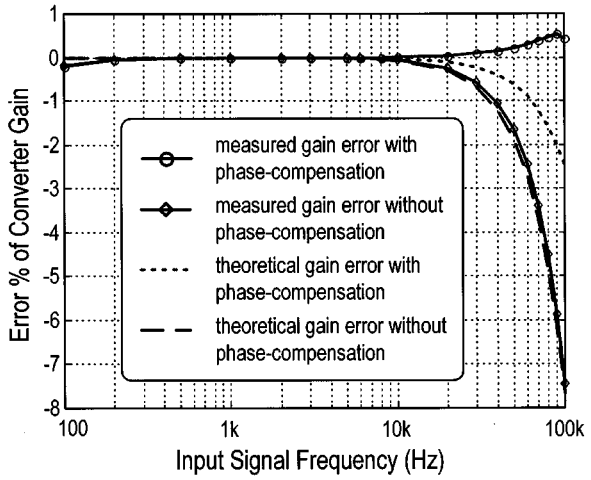


Fig. 13. Frequency response of the converter with and without phase compensation.

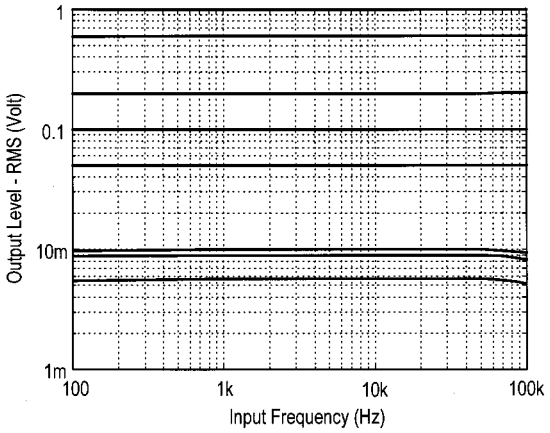


Fig. 14. Frequency response of different signal levels.

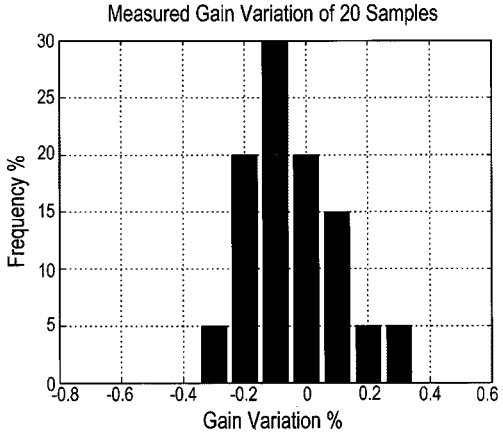


Fig. 15. Measured converter gain variation in 20 samples.

response of the converter for different output levels. Signal degradation becomes noticeable while input level and signal frequency are less than 10 $mV_{\rm rms}$ and greater than 50 kHz, respectively.

The converter gain is insensitive to process fluctuation since it depends only on an on-chip capacitor ratio. A histogram of measured gain variation in 20 samples is shown in Fig. 15. As shown in the histogram, no gain calibration is required; this

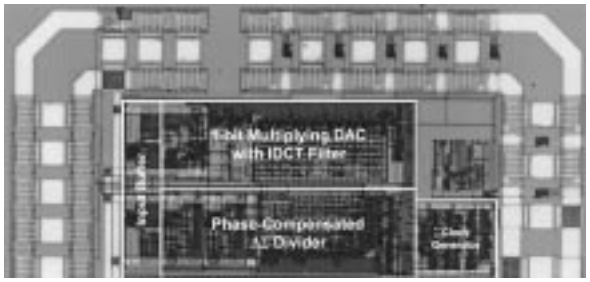


Fig. 16. Die microphotograph.

TABLE II
MEASURED PERFORMANCE SUMMARY

Full scale range (with SNR of 88 dB)	0.4	V_{rms}
Relative error of FS for arbitrary input waveforms	±0.2	%
Crest factor of input signals for accurate conversion	3	(na)
Signal bandwidth	50k	Hz
Gain variation	±0.4	%
Output noise voltage	<16	μV_{rms}
Supply voltage	±3	V
Power dissipation	40	mW

converter has an absolute gain error distributed in the range of ±0.4%. Measured performance of this test chip is summarized in Table II. A die photograph is shown in Fig. 16 where the rms converter occupies an active area of 660 × 1480 μm^2.

VII. CONCLUSION

One approach to realize a CMOS rms converter, a $\Delta\Sigma$ true rms converter, has been described and successfully integrated in a 0.8-μm CMOS process. In a $\Delta\Sigma$ divider, a varying denominator degrades the SQNR of the divider. The maximum SQNR can be obtained by restricting the denominator to be a quasi-static signal. In addition, transfer characteristics of a $\Delta\Sigma$ rms converter has been investigated, showing that the SQNR of this converter depends only on the input signal frequency without regard to the input levels. The crest factor of this converter can be designed by changing a capacitor ratio. However, obtaining a higher crest factor is a tradeoff with the SQNR of this converter. Furthermore, the linearity of this converter is limited by residue offset, especially for low-level signals.

An IDCT filter has been developed to make the converter gain depend only on an on-chip capacitor ratio, so this converter has good gain accuracy and temperature stability. Experimental results show that no trimming and calibration is required. This converter has an absolute gain error in the range of ±0.4%. In addition, using the phase-compensation scheme has effectively enhanced the converter's bandwidth. This converter has a bandwidth exceeding 50 kHz and a full-scale range greater than 0.4 V_{rms}. Furthermore, the relative error is ±0.2% for arbitrary inputs with a crest factor up to three. The response time of this converter is comparable to that of a digital converter, and the consumed power could be reduced in the future design. Therefore, the presented converter is a good choice for further integration of DMM chips.

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