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Thin-Film Transistors with Polycrystalline Silicon Films Prepared by Two-Step Rapid Thermal Annealing

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A novel two-step rapid thermal annealing (RTA) process has been developed to significantly reduce the crystallization time for the solid-phase crystallization (SPC) of amorphous silicon films. In comparison with the conventional SPC processes, it not only keeps a low thermal budget but also achieves a larger poly-Si film grain size than that obtained by one-step RTA, and even as large as that obtained by conventional furnace annealing (CFA). Furthermore, poly-Si thin-film transistors fabricated by such a novel annealing scheme possess electrical characteristics superior to those obtained by one-step RTA and comparable to those obtained by long-time CFA.

KEYWORDS: SPC, RTA, CFA, poly-Si TFTs, two-Step RTA

1. Introduction

In the last decade, polycrystalline silicon thin-film transistors (poly-Si TFTs) have received much attention, in particular, for active-matrix liquid crystal displays (AMLCDs) with on-glass peripheral circuits and 3-D integrated circuits.[1–3] Unlike the transistors fabricated on bulk silicon substrates, the performance of poly-Si TFTs is strongly influenced by the grain boundaries and intragranular defects. In order to improve the performance of poly-Si TFTs, the recrystallization of silicon films[4–8] has been widely investigated to enlarge the grain size and reduce the defect-state density in poly-Si films. In addition, AMLCDs, fabricated on glass substrates, require a low-thermal-budget process to avoid any degradation of glass substrates. However, the conventional low-temperature (600°C) furnace annealing in solid phase crystallization (SPC),consisting of incubation and crystallization steps, usually requires more than 10 h for full crystallization. The use of rapid thermal annealing (RTA)[9–12] enables efficient reduction of the thermal budget and cycle time of the processes, which results in a substantially higher throughput than with conventional furnance annealing (CFA). Nevertheless, the grain size of a poly-Si film annealed by RTA is much smaller than that obtained by CFA. Recently, new annealing methods which combine CFA and RTA[13,14] have been proposed to obtain high-quality poly-Si films and to reduce the annealing time for crystallization of a-Si films. On the other hand, it still takes a few hours to achieve full recrystalliztion. In this work, a novel two-step RTA method is proposed for the recrystallization of a-Si films. By this way, it not only reduces the annealing time from several hours to a few minutes but also enables the realization of high-quality poly-Si films of grain size as large as that in the case of long-time CFA. The electrical characteristics of poly-Si TFTs fabricated by various annealing methods are also compared and discussed.

2. Experimental Procedures

The poly-Si films were fabricated on thermally oxidized silicon wafers. A 100-nm-thick a-Si film was initially deposited at 475°C by low-pressure chemical vapor deposition (LPCVD) using Si_2H_6 gas. The crystallization was performed by the two-step RTA technique, in which the a-Si films were first annealed at 550°C for 60 s and then at 750°C for 60 s. In addition, comparison for films were also annealed by either CFA at 600°C for 20 h or one-step RTA at 750°C for 120 s. The structure and the grain size of the crystallized poly-Si films were determined by transmission electron microscopy (TEM). In order to evaluate the electrical characteristics of the poly-Si films, two sets of TFTs were separately fabricated using high- and low-temperature processes, denoted as HT and LT. After defining the active islands, 60-nm-thick gate oxide was thermally grown by dry oxidation at 900°C for the HT process and SiN_x was deposited as gate dielectrics by plasma-enhanced CVD (PECVD) at 300°C for the LT process. Therefore, another 250-nm-thick a-Si film was deposited at 560°C in a LPCVD system using SiH_4 and patterned as the gate electrodes. Self-aligned phosphorus ion implantation with energy of 50 keV and dose of 5E15 cm^{-2} was used to dope the drain, source, and the gate areas. Prior to the dopant activation, a 500-nm-thick encapsulation oxide was deposited in a PECVD system. The implanted dopants were activated by 40-min annealing at 850°C for the HT samples and by 12-h annealing at 600°C for the LT case. After opening the contact holes, the Al films were evaporated and then patterned. For evaluation of the simple effects of the different annealing processes on the TFT characteristics, no further hydrogenation was perfoemed. The final TFT had a conventional coplanar structure and the W/L ratio was 50 μm/10 μm.

3. Results and Discussion

Figure 1 shows the plan-view bright-field TEM micrograph of the 100-nm-thick silicon film annealed by (a) one-step RTA (750°C/120 s), (b) two-step RTA (550°C/60 s + 750°C/60 s), and (c) CFA (600°C/20 h). As can be seen in Fig. 1(a), the grains in the case of the one-step RTA process exhibit a dendritic structure and the grain size, as estimated by dark-field TEM, is around 0.8 μm. The structure of the silicon films annealed by two-step RTA, as shown in Fig. 1(b), is similarly dendritic and the grain size is about 1.5 μm. The result is almost similar to that for an a-Si film annealed by long-time CFA, as shown in Fig. 1(c). It is noteworthy that the CFA takes 20 h to crystallize the a-Si film, while the two-step RTA takes only 2 min. Therefore, the crystallization time of SPC can be significantly reduced with no associated reduction in grain size by applying the new annealing scheme.

To verify the electrical properties of the poly-Si films

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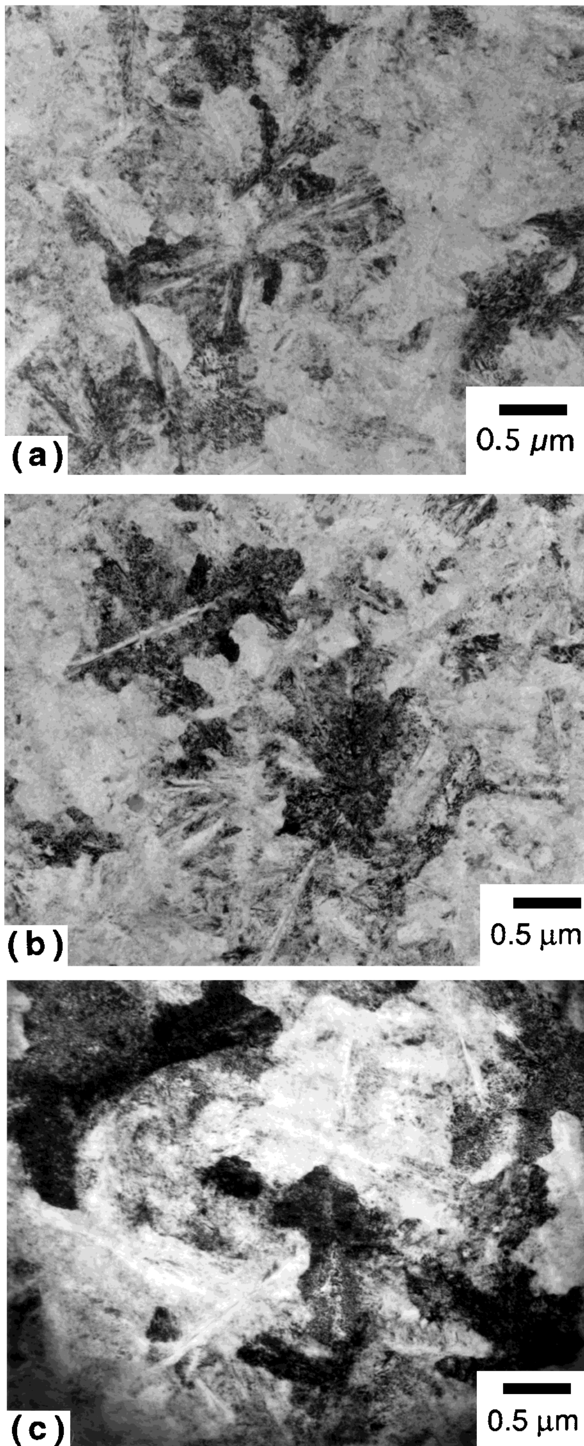

Fig. 1. Plan-view bright-field TEM micrographs of 100-nm-thick silicon films crystallized by (a) one-step RTA (750°C/120 s), (b) two-step RTA (550°C/60 s + 750°C/60 s), and (c) CFA (600°C/20 h).

formed by the new annealing technique, n-channel poly-Si TFTs were fabricated and the current–voltage (I–V) characteristics of the TFTs were measured by an HP 4156A precise semiconductor parameter analyzer. Figure 2 gives the typical I_d–V_g transfer characteristics for the differently processed TFTs at $V_{DS} = 5$ V. The extracted electrical parameters from the plot, including the threshold voltage, the on/off current ratio, the field effect mobility, the subthreshold swing, and the trap-state density, are all listed in Table I. The trap-state density N_t is obtained by using the theory es-

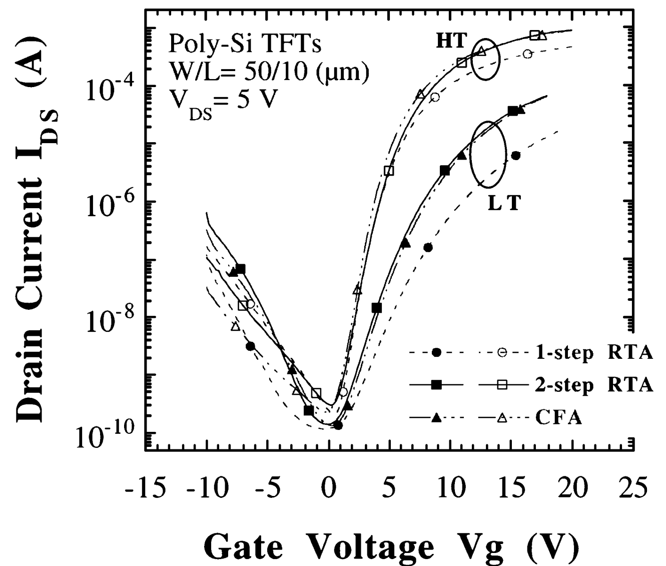

Fig. 2. The I_d–V_g transfer characteristics of n-channel poly-Si TFTs at $V_{DS} = 5$ V, fabricated using HT and LT processes with various crystallization methods. The W/L is 50 μm/10 μm.

tablished by Levison *et al.*[15] and Proano *et al.*[16] Whether the HT or LT process is used, it is evident that the two-step RTA specimens exhibit superior electrical performance such as higher field-effect mobility, on/off current ratio, lower threshold voltage, and trap-state density. The enhancement of the TFT characteristics is attributed to the larger grain size and lower trap-state density achieved by the two-step RTA method. As to the enlarged grain size obtained by two-step RTA, the first low-temperature RTA (550°C/60 s) is thought to play an important role during crystallization. It is presumed that the first low-temperature RTA induces the formation of a few nucleation sites which then enlarge during the second high-temperature RTA (750°C/60 s). In contrast, one-step RTA at 750°C induces the rapid formation of a mass of nucleation sites everywhere, which results in a small grain size. Further compared with CFA-TFTs, the devices fabricated by the two-step RTA possess similar electrical characteristics to those of the TFTs fabricated by CFA. The similar electrical performances of the TFTs fabricated by these two methods are believed to be due to their similar microstructures and grain size. The lower field effect mobility, as compared with that of films fabricated by Excimer laser annealing (ELA), can be attributed to the crystallinity of the poly-Si films. The poly-Si film subjected to solid-phase crystallization of RTA and CFA has more defects than that in case of liquid-phase crystallization by ELA. These defects include intra-grain defects and high-angle grain-boundaries within the active channel portion of the TFTs. Hence, the field effect mobility of the poly-Si TFTs fabricated by CFA or two-step RTA is relatively lower than that of the TFTs fabricated by ELA.

4. Summary and Conclusions

In conclusion, a new annealing method, two-step RTA, was developed to obtain high-quality poly-Si films. The grain size of poly-Si films obtained by this two-step RTA is twofold that in the case of one-step RTA and as large as that obtained by CFA. Poly-Si TFTs with an active layer prepared by this novel method have superior electrical characteristics to those

Table I. The values of the threshold voltage, the on/off current ratio, the field effect mobility, the subthreshold swing and the trap-state density of poly-Si TFTs fabricated using HT and LT processes with various SPC techniques. The threshold voltage is defined at a fixed drain current $I_d = I_{dn} \times W/L$, where I_{dn} is the normalized drain current, 10 nA. The subthreshold swing and field effect mobility were measured at $V_{DS} = 0.1$ V for $W/L = 50\,\mu$m/10 μm. The on/off current ratio is the drain current measured at $V_{DS} = 5$ V and $V_G = 15$ V over the minimum value of the drain current measured at $V_{DS} = 5$ V.

		Threshold voltage (V)	On/Off current ratio	Field effect mobility μfe (cm^2/V·s)	Subthreshold swing (V/dec)	Trap-state density (cm^{-2})
HT	RTA	2.85	1.44×10^6	26.4	0.872	3.48×10^{12}
	2-step RTA	2.78	1.90×10^6	52.5	0.806	2.67×10^{12}
	CFA	2.58	2.46×10^6	50.4	0.791	2.64×10^{12}
LT	RTA	6.77	4.58×10^4	1.95	1.83	8.92×10^{12}
	2-step RTA	4.91	2.43×10^5	6.82	1.40	8.08×10^{12}
	CFA	5.20	2.33×10^5	5.77	1.39	8.21×10^{12}

fabricated by one-step RTA, comparable to those obtained by CFA. Since the two-step RTA can significantly improve the characteristics of the poly-Si TFTs at a lower thermal budget and manufacturing cost, its use is recommended for application to poly-Si TFT/LCDs.

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