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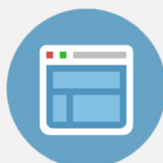

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Defects in Ge^+-preamorphized silicon

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This work studied the morphology and annealing behaviors of extended defects in Si subjected to various Ge^+ preamorphization and BF_2^+ implantation conditions. The extended defects formed were near the specimen surface when Ge^+ implantation energy and dose amount were low. During subsequent annealing, the end-of-range (EOR) loops were enlarged and then moved out of the specimen. High energy/low dose Ge^+ implantation generated a damaged layer which initially transformed into a wide zone containing dislocation loops and rodlike defects in the annealed specimen. As the annealing proceeded, the width of defective zone gradually shrunk so that most of the extended defects could be annihilated by defect rejection/recombination process. In addition to the category II defects found in previous investigations, hairpin dislocations emerged in high energy/high dose Ge^+-implanted specimens. In this specimen, rodlike defects and hairpin dislocations could be removed by annealing, while the EOR loops became relatively inert so that their removal would require high temperatures and/or long annealing times. Microwave plasma surface treatment was also carried out to form a nitride layer on specimen surface. Experimental results indicate that in addition to effectively reducing the size of EOR loops, surface nitridation might serve as a vacancy source injecting vacancies into Si to annihilate the interstitials bounded by dislocation loops. Reduction in the defect size was pronounced when bias voltage was added to the plasma process. However, radiation damage might occur with too high of a bias voltage. © *1999 American Institute of Physics.* [S0021-8979(99)06322-7]

I. INTRODUCTION

With the decreasing lateral dimensions of electronic devices, the formation of shallow p/n junctions becomes a vital issue in integrated circuit (IC) processing. The p/n junctions can be divided into two major types, the p^+/n junction and the n^+/p junction. The fabrication of shallow p^+/n junction with desired physical properties has been extensively studied.[1] Ion implantation is one of popular techniques to prepare the p^+/n junction. It is often carried out by amorphizing the n-type Si substrate with a Si^+ or Ge^+ implantation, followed by implanting p^+ impurities such as B^+.[2] The purpose of preamorphization is to inhibit dopant channeling during subsequent implantation.

Following ion implantation, annealing treatment is carried out to activate the dopant and annihilate the primary crystalline defects resulting from ion bombardment. However, various extended defects appear after annealing. According to the classification scheme of Jones *et al.*, category I damages arise when ion implantation can not produce a continuous amorphous layer.[3] In the presence of a continuous amorphous layer, the category II damages, also called the EOR dislocation loops, emerge in the vicinity of amorphous/crystalline (a/c) interface. An adverse phenomenon related to the EOR defects is that the excess Si interstitials in the dislocation loops may combine with the dopant atoms to induce the transient enhanced diffusion (TED).[4,5] Previous investigations conjectured that the TED is attributed to the emission of Si interstitials from the rodlike defects.[6–8] Thus, in terms of understanding the occurrence of TED, the study of the nucleation, growth, and dissolution of rodlike defects in ion implanted Si is another important issue. The category III damages, also referred to as the hairpin dislocations, are associated with the occurrence of an imperfect solid phase epitaxy of an amorphous structure during annealing. The sharper the a/c interface implies less hairpin dislocations.[9] Concentrations of the extended defects mentioned above vary according to the ion implantation and subsequent annealing conditions.

As well known, the extended defects deteriorate the electrical properties of p^+/n junction and, therefore, must be eliminated to secure a defect-free junction device. Ajmera *et al.* employed rapid thermal annealing (RTA) at 1050 °C for 10 s in argon (Ar) atmosphere to remove implantation defects in shallow, low dose Ge^+-preamorphized B^+-implanted Si.[10,11] Myers *et al.* demonstrated that balancing the Ge^+ preamorphization and subsequent BF_2^+ implantation conditions in Si allows one to annihilate the EOR defects by RTA at a temperature as low as 950 °C for 10 s.[12] The role of free surface on defect elimination during thermal process has received considerable attention.[13–18] For instance, Agarwal *et al.* revealed that free surface was a strong interstitial sink to extract point defects from the EOR loops, thereby reducing the TED.[14] Another possible defect annihilation mechanism in BF_2^+-implanted Si proposed by Myers *et al.* is that the free surface can promote the climb motion of

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TABLE I. Ion implantation conditions.

Implantation condition	Specimen S	L	D	H
Ge^+, 5 keV, $5\times10^{14}/cm^2$	○			
Ge^+, 30 keV, $5\times10^{14}/cm^2$		○	○	○
Ge^+, 400 keV, $1\times10^{14}/cm^2$			○	
Ge^+, 400 keV, $5\times10^{14}/cm^2$				○
BF_2^+, 5 keV, $5\times10^{14}/cm^2$	○	○	○	○
Thickness of amorphous layer (nm)	17	43.4	43.4	440

TABLE II. Conditions of plasma treatment with applied bias.

Conditions of treatment and applied bias	Specimen
250 W, −400 V, N_2 ambient, 20 cc/min, 1 h	D4, H4
100 W, −800 V, N_2 ambient, 20 cc/min, 1 h	D5, H5

dislocations by exerting a pull force on EOR loops.[18]

Gettering is another favored technique to eliminate the EOR defects.[19,20] According to a previous work, a certain type of silicide on Si surface might serve as a source of point defects.[21] The vacancies generated then diffused into Si to combine with the excess interstitials bounded by EOR loops. Wen *et al.* presented an example of this, demonstrating that the density of EOR defects would decrease when titanium (Ti) silicide was grown on implanted Si.[22] By using a NH_3 annealing process, Herner *et al.* grew a nitride layer on Si which might also serve as a point defect source to remove EOR defects.[23] In a related work, Ahn *et al.* demonstrated that the nitride layer acts as the source of vacancies which diffuse into Si to eliminate the EOR defects.[24]

In this work, we prepare Si wafers subjected to various Ge^+ preamorphization conditions followed by a BF_2^+ ion implantation. Using transmission electron microscopy (TEM), this work also investigates the extended defects formed during subsequent annealing treatments. Experimental results indicate that ion implantation conditions and subsequent annealing process affect the defect removal behaviors of Si. In addition, microwave plasma process is employed to grow a SiON layer that serves as a point defect source on implanted Si. Also investigated herein are the effects of ambient and applied bias of plasma treatment on the distribution and size variation of EOR loops. According to those results, plasma surface modification is a viable alternative to reduce the size of EOR defects. Moreover, the ion implantation conditions affect its defect reduction capability. Further size shrinkage of EOR loops is observed when bias voltages are added to the plasma modification process. Nevertheless, such an addition induces radiation damages beneath the specimen surface when the bias voltage is too high.

II. EXPERIMENT

The (100), 3–5 Ω cm, *n*-type single-crystalline Cz–Si wafers (oxygen concentration less than $10^{18}\,cm^{-3}$) were first cleaned by the standard RCA cleaning process. The wafers were then Ge^+ preamorphized by using a Varian E200 ion implanter according to the conditions listed in Table I followed by a BF_2^+ implantation within the dose amount of $5\times10^{14}\,cm^{-2}$ and accelerating voltage of 5 keV. Part of the implanted specimens was further treated by microwave plasma by using a TePla 100E plasma system either in nitrogen or forming gas ambient (N_2:H_2=10:1). The power of plasma process was 250 W, the flow rate of gas was 100 ml/min, the chamber pressure was 0.2 Torr, and the dwell time was 3, 6, and 12 h, respectively. Bias voltage was also applied to *D*- and *H*-series specimens during plasma surface modification according to the conditions listed in Table II. Following plasma treatment, a silicon oxide layer of 500 nm thick was immediately sputtered onto the specimens. Subsequent annealing was carried out in either vacuum or nitrogen furnace at the temperatures ranging from 700 to 1000 °C for various time intervals.

The depth profile of chemical composition was carried out on a VG Microlab 310F Auger electron spectrometry (AES). The specimens were also thinned properly and sent to a Hitachi H-600 electron microscope to investigate the defect morphology. Both plan-view and cross-sectional TEM (PTEM and XTEM) specimens were prepared. In addition to microstructural registration, TEM micrographs were also used to quantify the interstitial concentration bounded by EOR dislocations. This method is described as follows. First, a $3\times3\ cm^2$ area was selected on a weak beam dark field picture imaged at the diffraction condition $\mathbf{g}$=[220]. The PTEM micrograph magnified at 30 000× was then sent to a personal computer equipped with image processing software (Ultimage from Graftek) to calculate the number and mean diameter of the dislocation loops. The interstitial concentration bounded by EOR dislocations was equal to the product of the density of EOR loops (i.e., number of loops per unit area of TEM pictures), area of EOR loops, and $1.6\times10^{15}\,cm^{-2}$ (i.e., average atom density in {111} planes of Si). The concentration of interstitials bounded by the rodlike defects was calculated by a similar method. The average line length of rodlike defects was determined from TEM micrograph. Assume that the width of rodlike defects is approximately equal to 6 nm. The concentration of interstitials bounded by the rodlike defects was equal to the mean line length multiplied by 26 interstitials per nm and the density of rodlike defect per unit area.[25]

III. RESULTS AND DISCUSSION

A. Effects of annealing on defect morphology

1. Specimen S

Figure 1 shows the XTEM micrograph for specimen S annealed at 700 °C for 1 min. The Ge^+ preamorphization generated a very thin amorphous layer of 17 nm thick in specimen S. According to Fig. 1, a very narrow band of extended defects formed in the vicinity of original *a/c* inter-

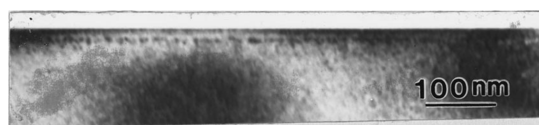

FIG. 1. Cross-sectional view of specimen S annealed at 700 °C for 1 min.

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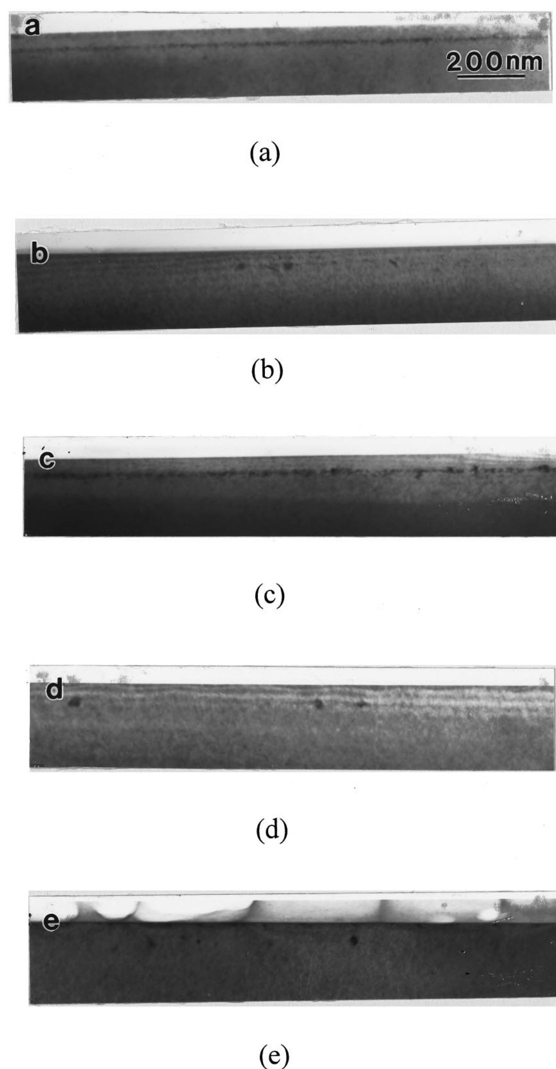

FIG. 2. Cross-sectional view of specimen L annealed at (a) 700 °C for 1 min, (b) 700 °C for 40 h, (c) 800 °C for 1 min, (d) 800 °C for 6 h, and (e) 900 °C for 10 s.

face when specimen S was annealed for relatively short times, e.g., at 700 or 800 °C for 1 min. These extended defects could be completely eliminated from the specimen by extending the time and/or raising the temperature of annealing treatment.

2. Specimen L

In specimen L, the Ge^+ implantation produced an amorphous layer of 43.4 nm thick. Annealing at 700 °C for 1 min generated a band of extended defects near the a/c interface, as shown in Fig. 2(a). At this temperature, formation and coalescence of EOR dislocation loops were observed. However, the EOR loops persisted after 40 h of annealing [Fig. 2(b)]. Coalescence of EOR loops and their removal became more obvious in specimen L annealed at temperatures beyond 800 °C. The dense EOR loops formed in specimen L annealed at 800 °C for 1 min gradually diminished with the increase of annealing time [Figs. 2(c) and 2(d)]. The XTEM observation and the calibration of concentration of interstitials bounded by EOR loops shown in Fig. 3 indicated that

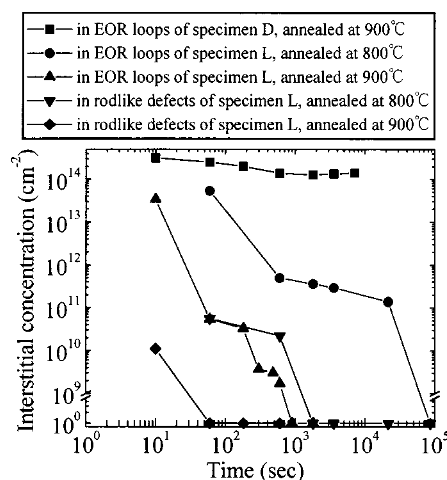

FIG. 3. Interstitial concentration bounded by rodlike defects and EOR loops as a function of annealing time in specimens D and L annealed at 800 and 900 °C.

no EOR defect remains in specimen L annealed at 800 °C for 24 h. Annealing at 900 °C for 10 s led to only a few coarse EOR loops in specimen L [Fig. 2(e)]. Notably, 900 °C annealing for 15 min or a 1000 °C annealing for 1 min could eliminate EOR defects in specimen L. Instead of increasing the annealing times, increasing the annealing temperature seems to be a more effective means of eliminating extended defects in specimen L. This is attributed to the enhancement of both vacancy and interstitial diffusivities at elevated temperatures, which accelerates the rate of defect annihilation.

Due to their intimacy, interactions between extended defects and sample surface should play an important role in defect annihilation for specimen L. During early annealing, the extended defects might reject a portion of excess interstitials, accounting for our observation of a steady decline of interstitial concentration in Fig. 3. In the middle of annealing treatment, a plateau region appears in the plot of Fig. 3. This should correspond to the enlargement of EOR loops by the coalescence process. According to the analysis of Narayan and Jagannadham, the total image force exerted on the loop increases with an increasing size of dislocation loops.[26] When annealing went beyond a certain time interval, the EOR loops became so large that they would experience a large enough image force which then pulled them out of the specimen. Hence, an abrupt drop of interstitial concentration bounded by EOR loops was observed as depicted in Fig. 3. The PTEM observation revealed that the maximum diameter of EOR loops in specimen L was about 26 nm for the specimen annealed at 900 °C for 8 min. By applying the formula of Narayan and Jagannadham,[26] the EOR loops of such a size could be removed through the interaction of image force if they were located at the average distance 52 nm from free surface. The XTEM observation revealed that in specimen L, most of the EOR loops lie in the depth ranging from 43.4 to 54 nm from free surface. The defect elimination in specimen L was hence attributed to the interactions of image force, particularly in the later stage of annealing treatment.

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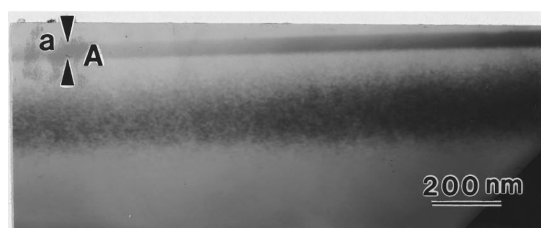

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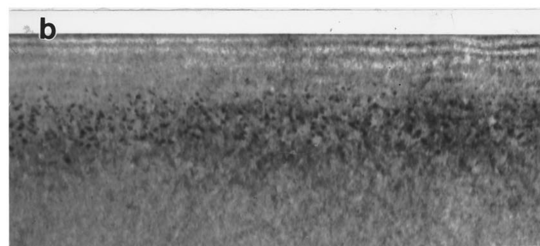

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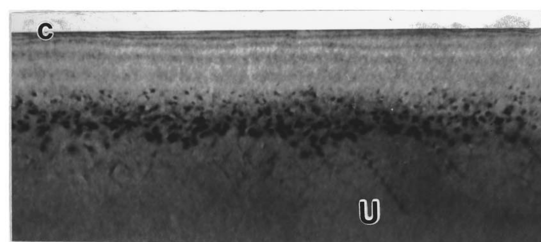
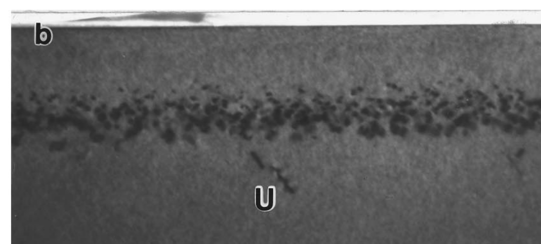


(c)

FIG. 4. Cross-sectional view of specimen D (a) as-implanted and annealed at 700 °C for (b) 2 h and for (c) 5 h (A: amorphous band; U: unfaulting dislocations).

(a)



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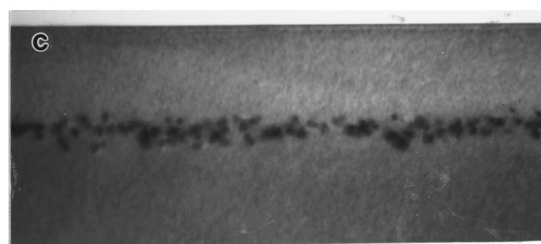

(c)

FIG. 5. Cross-sectional view of specimen D annealed at 800 °C for (a) 1 min, (b) 30 min, and (c) 24 h (U: unfaulting dislocations).

3. Specimen D

Figure 4(a) depicts the cross-sectional view of as-implanted specimen D. In addition to an amorphous layer of 43.4 nm thick, ion implantation also produced a damaged layer about 300 nm thick beneath the amorphous layer, as denoted by the dark contrast region in Fig. 4(a). During the 700 °C annealing, the category I defects accumulating in the damaged layer first transformed into cluster-like defects. As the time of heat treatment increased, the width of defective zone gradually shrunk, as shown in Figs. 4(b) and 4(c). In specimen D annealed at 700 °C, rodlike defects lying on {311} and {100} appeared after a 2 h treatment, as illustrated in Fig. 4(b). ''Unfaulting'' reaction of rodlike defects into perfect dislocations[27] was observed when the specimen was annealed for 5 h, as depicted in Fig. 4(c). Further annealing promoted the decomposition of rodlike defects so that they were barely observed in specimens annealed for 40 h.

The defect morphologies of specimen D annealed at 800 °C for various times are shown in Figs. 5(a)–5(c). At this temperature, both EOR loops and rodlike defects appeared in early annealing [Fig. 5(a)]. However, decomposition of the rodlike defects was relatively fast, which was completed in about 30 min. This phenomenon is illustrated in Fig. 5(b) in which most of the rodlike defects diminished and only few ''Unfaulting'' perfect dislocations remain in the specimen. While occurring with further annealing, coalescence of dislocation loops proceeded in a relatively slow rate so that no significant change of density and sizes of EOR loops was observed [Fig. 5(c)].

Figures 6(a) and 6(b) present the XTEM micrographs for specimen D annealed at 900 °C for 10 s and 2 h, respectively. At this temperature, EOR loops were the only type of defect visibly observed. Figure 3 plots the concentration of interstitials bounded by EOR loops as a function of annealing time. Since the 900 °C annealing temperature was relatively high, we can infer that the dramatic decrease of interstitials bounded by EOR loops at short annealing times is attributed to the rejection of interstitials which could then be annihilated by recombining with the vacancies provided by free surface and/or diffusing towards the specimen surface.[14,28] Since the dislocation loops were embedded at a depth of about 300 nm beneath the surface of specimen D, image force was unlikely the mechanism which would eliminate the defects. For the EOR loops of size shown in Fig. 6(b), the

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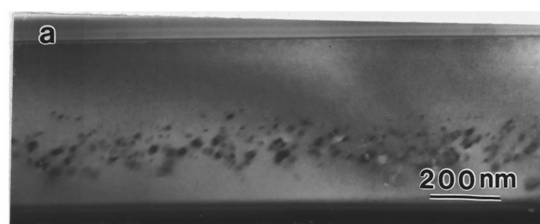
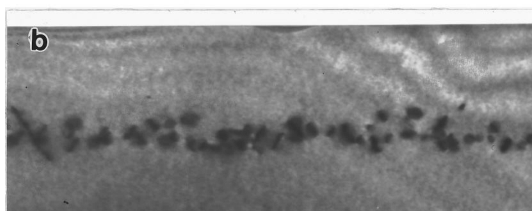


(a)



(b)

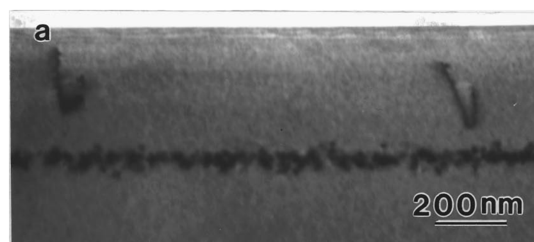
FIG. 6. Cross-sectional view of specimen D annealed at 900 °C for (a) 10 s and (b) 2 h.

calculated image force was too small to pull them out of the specimen.[27] In addition to the enlargement of EOR loops, the number of EOR loops apparently decreased when annealing time exceeded 10 min [Fig. 6(b)]. Beyond this time interval to 2 h, the EOR loops appeared to undergo conservative Ostwald ripening, as indicated by Figs. 3 and 6.

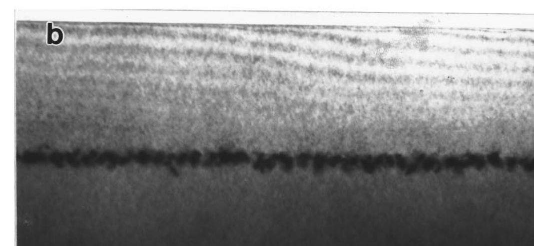
4. Specimen H

The ion implantation generated a continuous amorphous layer nearly 440 nm thick in specimen H. Figures 7(a)–7(d) depict the defect morphologies of specimen H annealed at 800 and 900 °C for various time intervals, respectively. The emergence of hairpin dislocations is a notable feature of these XTEM pictures. Such line defects were attributed to the not-so-sharp a/c interface generated by high energy/high dose Ge^+ implantation in specimen H. During annealing, the tiny misoriented crystallites embedded in the vicinity of rough a/c interface served as the nucleation sites of hairpin dislocations. The Ge^+ implantation employed in specimen H also generated a large amount of rodlike defects. Our calibration revealed that the interstitials bounded by rodlike defects in specimen H annealed at 800 °C for 10 min was $4.34\times 10^{12}/cm^2$. Meanwhile, in specimen L annealed under the same condition, the number of interstitials was $2.2\times 10^{10}/cm^2$.

Figure 8 quantitatively depicts the concentration of interstitials bounded by rodlike defects and EOR loops as a function of annealing times at 800 and 900 °C. At 800 °C, removing the rodlike defects took 24 h; meanwhile, at 900 °C, these defects could be annealed out in a 30 min treatment. Figure 8 also reveals that there is no significant drop of concentration of interstitials bounded by EOR loops in the specimens annealed at 800 °C up to 24 h. Accompanied by the TEM observation in Figs. 7(c) and 7(d), in specimen H, the EOR loops apparently undergo only the conser-



(a)



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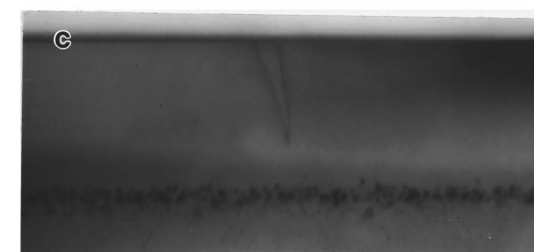
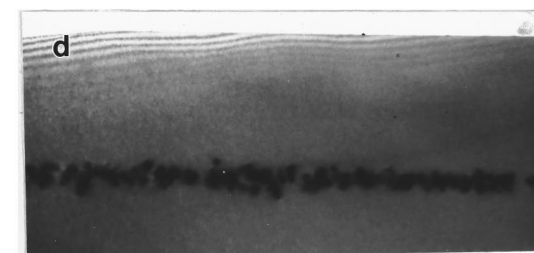


(c)



(d)

FIG. 7. Cross-sectional view of specimen H annealed at (a) 800 °C for 30 min, (b) 800 °C for 24 h, (c) 900 °C for 10 s, and (d) 900 °C for 30 min.

vative coarsening process during such a annealing treatment. The persistence of EOR loops might be attributed to that the extended defects were buried deep in specimen H. These loops interacted to a lesser extent with external defect sinks such as specimen surface so that the rate of defect annihilation became relatively slow. Annealing treatment at higher temperatures and/or longer time intervals was required to remove EOR defects from specimen H.

Figure 9 plots the variation of hairpin dislocation density in specimen H annealed at 700, 800, and 900 °C for various time intervals. In a time span of 24 h, eliminating hairpin dislocations by annealing at 800 °C or below was extremely difficult. However, at 900 °C, these line defects were elimi-

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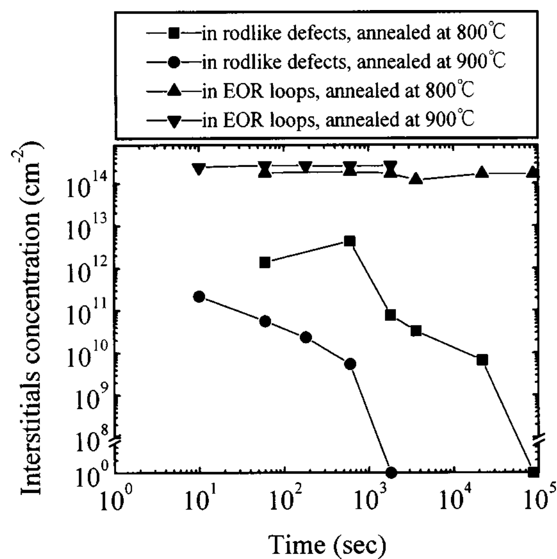


FIG. 8. Interstitial concentration bounded by rodlike defects and EOR loops as a function of annealing time in specimen H annealed at 800 and 900 °C.

nated in a relatively fast manner that they were no longer observed in specimens when annealing time intervals went beyond 30 min.

B. Effect of plasma surface nitridation on EOR defect removal

AES analysis indicated that the composition of plasma surface nitridation layer was in the form of SiON. AES analysis also revealed that the thickness of SiON layer increased with the time of plasma treatment. The thickness of SiON for the specimens treated by N_2 ambient for 3, 6, and 12 h was 2.5, 3.2, and 3.5 nm, respectively. The thickness of SiON layer for the specimen treated by N_2–H_2 ambient for 3, 6, and 12 h was 2.1, 2.9, and 3.2 nm, respectively. The defect size change of specimens D and H subjected to plasma treatment for various times is presented. The TEM observations revealed that the surface nitridation significantly reduce the size of EOR loops but not the number of EOR defects. Figures 10(a) and 10(b) illustrate the variation of diameter of

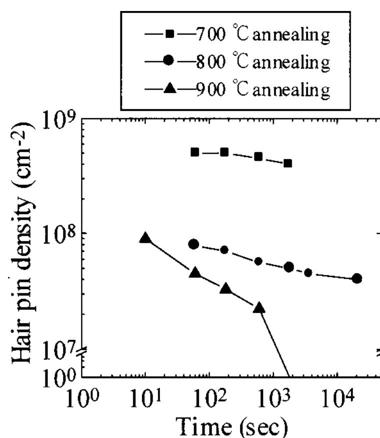
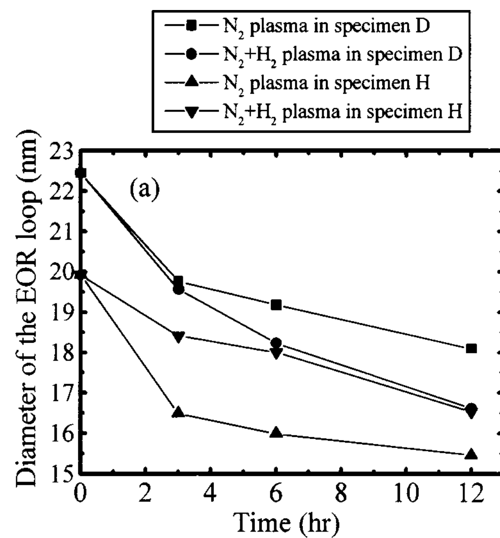


FIG. 9. Density of hairpin dislocations in specimen H as a function of annealing time at various temperatures.



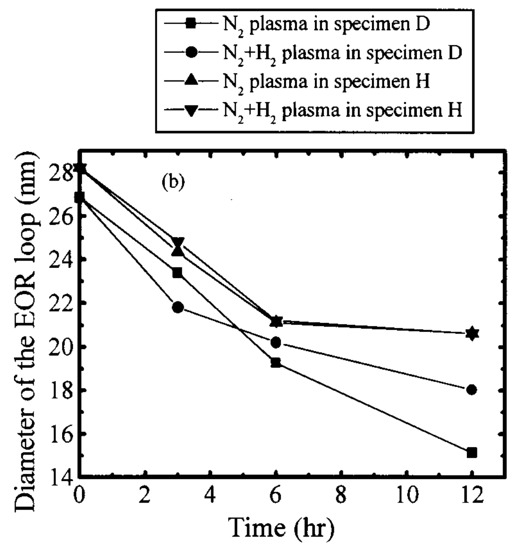


FIG. 10. Variation of diameter of EOR loops as a function of plasma treatment time in specimens D and H annealed at 900 °C for (a) 1 h and (b) 2 h.

EOR loops as a function of times of plasma treatment in N_2 or N_2+H_2 ambient for specimens D and H annealed at 900 °C for 1 and 2 h, respectively. According to these figures, the size of EOR loops decreases with an increase of the time intervals of plasma treatment. The thicker the SiON layer implies its enhanced ability to eliminate the interstitials bounded by EOR loops. This result suggests that microwave plasma surface nitridation is viable alternative for reducing defects.

Herein, a certain amount of hydrogen was added into plasma nitridation ambient to enhance the mobility of vacancies during subsequent annealing, thereby allowing us to obtain smaller EOR loops. However, according to experimental results, it benefited only the plasma-treated specimen D annealed at 900 °C for 1 h, as indicated in Fig. 10(a). In other specimens, either the opposite situation or no beneficiary was observed. This is possibly due to the relatively high annealing temperature. At 900 °C, the fast atomic diffusion rate would reduce the recombination time of vacancy and interstitial. This smears out the enhancement of vacancy mobility

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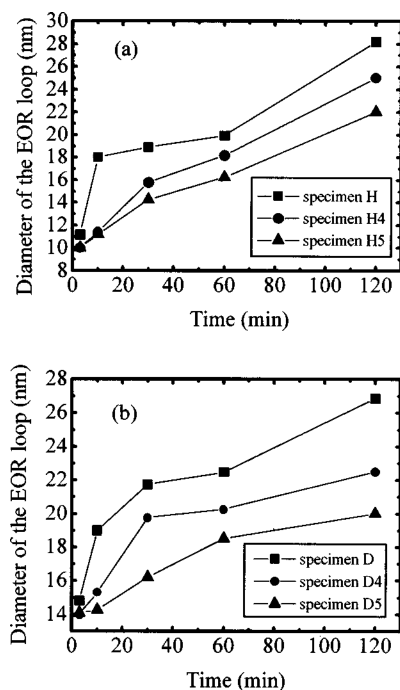

FIG. 11. Variation of diameter of EOR loops as a function of annealing time in (a) specimen H and (b) specimen D annealed at 900 °C.

by hydrogen and its effects to reduce the size of EOR loops.

Figure 11 shows the variation of EOR loop diameter as a function of subsequent annealing times in a series of specimens D and H subjected to plasma treatment with applied bias. For the specimens treated with −400 V, the thickness of SiON was about 5.6 nm and with −800 V, the thickness of SiON was 7 nm. According to this figure, the EOR loop size reduction increases with the increase of applied bias. This observation implies that the applied bias voltage can reinforce the surface nitridation of plasma treatment, thereby promoting the annihilation of interstitials bounded by EOR loops. However, as revealed by TEM, applying bias voltage during plasma process had a slight effect on reducing the number of EOR defects. The TEM observation also revealed that a high bias voltage induced cluster-like damages beneath the specimen surface. Therefore, bias voltage condition must be adjusted to optimize the plasma modification process for defect reduction.

IV. CONCLUSIONS

This work investigated the extended defects which formed in Si preamorphized specimen by various Ge^+ implantation conditions followed by BF_2^+ implantation. Experimental results indicate that ion implantation conditions affected the morphology and spatial distribution of defects. During subsequent annealing, the behaviors of defect removal were related to the depth of defects beneath the free surface, defect density and their size.

When a relatively low energy/dose ion implantation was carried out, extended defects generated were near the specimen surface and could be eliminated with relative ease by appropriate annealing treatment. For the EOR loops, they first enlarged themselves by Ostwald ripening. When annealing went beyond a certain time span, the dislocation loops became large enough, possibly allowing the resulting image force to overcome the lattice frictional force and pull those loops out of the specimen.

For those specimens bombarded by high energy Ge^+ ions, the morphology of extended defects changed according to the dose amount of implantation. During early annealing, widely distributed cluster-like defects initially formed in low ion dose specimens. Those defects then transformed into rodlike defects of {311} and {100} types as well as dislocation loops by coalescence process and the defective band gradually shrunk as the annealing proceeded. During subsequent annealing, the rodlike defects degenerated into perfect dislocations and then annealed out of the specimen. As for the EOR loops, they were buried at such a large depth that the image force resulting from free surface was negligible. We believe that rejecting the interstitials and recombining with the vacancies are the most plausible mechanisms for defect annihilation during annealing. The number of EOR loops was relatively low in this specimen and they underwent conservative coarsening during extended annealing.

In the high energy/high dose Ge^+-implanted specimen, very dense EOR loops and rodlike defects formed in the vicinity of a/c interface. The rodlike defects could be annihilated by appropriate annealing treatment whereas the EOR loops persisted at 800 °C for 24 h. In this specimen, the EOR loops underwent only the conservative coarsening process, as revealed by TEM observations and the calibration of interstitial concentration bounded by the EOR loops. Thermal treatment at a higher temperature and/or longer time may be necessary to eliminate the EOR loops. Notably, formation of hairpin dislocations in the high energy/high dose Ge^+-implanted specimen was a distinguishing feature. An 800 °C, 24 h annealing was found to be insufficient to remove these line defects. However, they could be eliminated by annealing at 900 °C for 30 min.

This work also examined the effect of microwave plasma surface nitridation on the removal of extended defects. According to those results, the diameter of EOR loops decreased when increasing the time of surface modification. The surface nitride layer might be treated as a defect source that provided vacancies to combine with the interstitials and reduced the size of EOR loops. In addition, hydrogen was added to the plasma ambient to enhance the mobility of vacancies during defect recombination. However, the accelerating effect of hydrogen only became apparent in part of the specimens; its role in reducing defects demands further clarification. Moreover, bias voltage was incorporated with plasma process to reinforce the surface nitridation, indicating that applying the bias voltage offers a better size reduction of EOR loops. Nevertheless, such an application generated surface damages so that the bias condition must be adjusted to achieve process optimization.

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