# Improvement of Junction Leakage of Nickel Silicided Junction by a Ti-Capping Layer

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Abstract—A novel NiSi process with a thin Ti-cap layer is proposed, for the first time, to improve the leakage problem of Ni-silicided junction. The Ti-cap samples exhibit a very low leakage current density about  $1\times 10^{-9}$  A/cm² after 600 °C annealing, which is one order of magnitude reduction comparing with uncapped samples. From Auger analyzes, it is found that this significant improvement results from suppression of the oxidation of the Ni-silicide during the thermal annealing process.

Index Terms—Junction leakage, nickel silicide, titanium.

#### I. Introduction

THE SILICIDE-RELATED technology has become an integral part of submicron devices for reducing the parasitic resistance in order to improve the devices and circuit performance. TiSi2 has been widely used in industry. However, the sheet resistance of the TiSi2 lines increases with decreasing line width that limits the future of TiSi<sub>2</sub> salicide in  $0.1-\mu m$ CMOS applications [1], [2]. A NiSi salicide technique has been developed as an alternative to TiSi2 due to no such narrow line effect [2], [3]. However, the problems encountered in the NiSi silicidation process are anomalously large junction leakage current and sheet resistance degradation. Recently, using TiN cap [4] and nitrogen-doped [5] techniques have been reported to reduce junction leakage current. The improvement was found due to the formation of nitride layer, which prevents oxidation of silicide/silicon interface and suppresses interface roughness to a certain degree. In this paper, we propose a novel NiSi process with a thin Ti-cap layer without any nitride layer. The titanium layer serves as an excellent oxygen scavenger. The junction with a very low leakage current density about 1 nA/cm<sup>2</sup> can be achieved.

### II. EXPERIMENT

Samples were fabricated on n-type (100) oriented Si wafers with resistivity of 1–5  $\Omega$ -cm. The field oxide with thickness of about 5500 Å was thermally grown by wet oxidation. Then, active regions were defined and followed by a 50-keV BF $_2^+$  implantation to a dosage of  $2\times10^{15}$  cm $^{-2}$ . After implantation, thermal annealing was carried out at 900 °C for 20 min in nitrogen. Nickel and titanium films were deposited at a base

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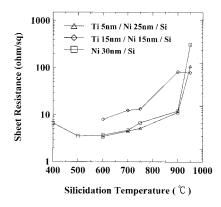


Fig. 1. Sheet resistance of Ni silicide as a function of silicidation temperature

pressure of less  $1 \times 10^{-6}$  torr with a deposition rate of 1 Å/s. All the samples were then annealed in the N<sub>2</sub> ambient for 30-s at different annealing temperatures in a RTA system. After RTA treatments, unreacted metal was removed by wet etching. Sheet resistance was measured using four-point-probe (FPP). X-ray diffraction (XRD) was used to identify the composition and the phase of silicide films. The current–voltage (I-V) characteristics of the junctions were measured by Hp-4145. Auger electron spectroscopy (AES) was used to determine the profiles of metal species and Si.

# III. RESULTS AND DISCUSSION

Fig. 1 shows sheet resistance of Ni silicide as a function of silicidation temperature. Three kinds of structures were compared, Ni (30-nm)/Si, Ti(5nm)/Ni(25nm)/Si, Ti(15nm)/Ni(15nm)/Si. It is seen that the Ti(5nm)/Ni(25nm)/Si sample exhibits a little improvement of the sheet resistance degradation compared with the uncapped sample. The degradation at high annealing temperature results from the phase transformation of NiSi to NiSi2 and agglomeration. The Ti-cap layers somewhat retard the presence of agglomeration due to restriction of surface diffusion. Another reason is the Ti-cap layers suppress the oxidation of silicide films. In the Ti(15nm)/Ni(15nm)/Si sample, the sheet resistance was obviously larger than the uncapped sample at lower annealing temperature. From the results of XRD investigation, not any peaks of titanium silicide or titanium nitride in the Ti-cap samples were detected as annealing temperature below 750 °C and unreacted titanium was removed by wet etching. Hence, this thin NiSi film results in a high sheet resistance. The leakage current density (Jr) of Ni-silicided p<sup>+</sup>/n junction

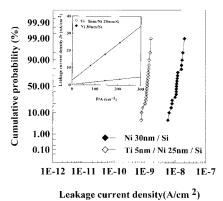
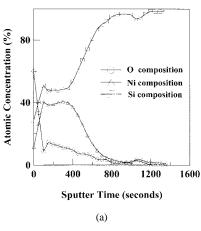


Fig. 2. Leakage current density (Jr) of Ni silicided  $p^+/n$  junction at -5 V reverse bias. Inset shows the fitting of the leakage current density (Jr) against the ratio of perimeter to area (P/A).



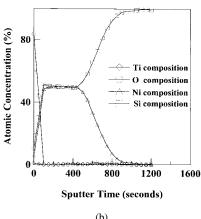


Fig. 3. Auger electron spectroscopy of Ni silicide formed by: (a) 30-nm Ni and (b) 5-nm Ti/25 nm Ni after 600  $^{\circ}$ C 30 s silicidation and removal of unreacted metal.

formed with and without the Ti-cap is shown in Fig. 2. The Ti-cap samples can achieve a very low leakage current density about  $1\times 10^{-9}~\text{A/cm}^2$  at 600 °C annealing, about one order of magnitude of reduction compared with uncapped samples. From the fitting of the leakage current density (Jr) against the ratio of perimeter to area (P/A) (shown in the inert of Fig. 2), it is found that the reduction is primarily due to the reduction of leakage from the perimeter. Fig. 3(a) shows

the auger electron spectroscopy (AES) of Ni-silicide without the Ti-cap after 600 °C silicidation. The signal of oxygen extended into entire nickel silicide film. The ratio of Ni to Si was not just equal to 1 due to the presence of Ni oxidant. On the other hand, for the samples with the Ti-cap shown in Fig. 3(b), the signal of oxygen reduces to a noise lowlimit level of the measurement in the entire nickel silicide film. Hence, it is clear that Ti-cap layer serves as an oxygen scavenger. According to the report of T. Ohguro et al. [4], [5], anomalously large Ni silicide junction leakage current is due to a very rough interface between the silicide layer and the silicon substrate caused by oxidation of the NiSi film during the thermal process. The oxygen plays the role as one kind of contaminant in the silicidation process and degrades the quality of Ni-silicide films. Ti-cap layer suppresses the oxidation at the interface between the silicide layer and the silicon substrate, which was believed to induce interface roughness. Although the result by using the TiN- and Ti-cap in somehow is in common, the mechanisms are different for TiN and Ti-cap. TiN is naturally a good barrier for a lot of oxidants. On the other hand, Ti-capping layer serves as an oxygen sacrificial layer in this case. Thus, the leakage current of Ni silicided junction with the Ti-cap can be significantly improved.

## IV. CONCLUSIONS

In summary, we have developed a new NiSi process with a thin Ti-cap layer and demonstrated the performance of sheet resistance and shallow junction. Our results reveal that the junction leakage current can be significantly reduced by using this technique. Ti-cap-layer suppresses the oxidation between Ni-silicide/silicon interface and can effectively reduce leakage current in the perimeter. Moreover, Ni-silicide with the Ti-cap has a little improvement for the degradation of sheet resistance at the same time.

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