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Electrical Reliability Issues of Integrating Thin Ta and TaN Barriers with Cu and Low-K Dielectric

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This work investigates the integration of very thin sputtered Ta and reactively sputtered TaN barriers with Cu and a low-dielectric-constant (low-K) layer of poly(arylene ether) (PAE-2). It is found that Cu readily penetrates into PAE-2 and degrades its dielectric strength in metal-insulator semiconductor capacitors of Cu/PAE-2/Si structure at temperatures as low as 200°C. Very thin Ta and TaN films of 25 nm thickness sandwiched between Cu and the low-K dielectric served as effective barriers during a 30 min thermal annealing at temperatures up to 400 and 450°C, respectively. We propose a failure mechanism of outgassing induced gaseous stress of PAE-2 under the Ta film to explain its premature barrier degradation. The TaN barrier did not suffer from this gaseous stress problem because of its stronger adhesion to PAE-2 than that of Ta to PAE-2, leading to a better long-term reliability.

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As device dimensions in ultralarge-scale integrated (ULSI) circuits are scaled down to deep submicron, the interconnect delay becomes the major performance-limiting factor.[1] Interconnect wire parasitics (wire resistance R and capacitance, C) have come to play a dominant role in determining not only the total signal delay but also the packing density, reliability, and manufacturing cost of integrated circuits (ICs). Because of increasingly smaller metal cross sections and reduced wire spacing, it is necessary to reduce RC through the use of new materials to limit the number of metal levels and keep the metal pitch tight. In addition, it has been reported that Cu/low-K (low-dielectric-constant) designs in 0.13 μm technology require only six metal levels to maintain a constant RC, compared to 12 levels in the Al/SiO_2 system.[2] More interconnect levels need more process steps, and each additional step reduces final production yield. Therefore, integration of Cu metallization and low-K dielectrics has been regarded as a promising antidote to alleviate the issues of driving speed, noise tolerance, and power dissipation in view of their respective inherent benefits such as low electrical resistivity, superior electromigration resistance, and low dielectric constant.

Before successful integration of the Cu/low-K system, however, a number of issues have to be addressed. First, with foreseeing damascene structures for Cu, a thin barrier layer is needed to encapsulate the Cu line in three sides so as to foster adhesion and avoid Cu outdiffusion through the interlevel dielectric.[1] As device dimensions move to 0.25 μm and below, it becomes inappropriate to use a barrier layer thicker than 30 nm because a thick barrier liner may lead to a high line resistance, and thus negate the advantage of low Cu resistivity. Refractory metals and their compounds have been regarded as attractive candidates for barrier layers because of their high thermal stability and good electrical conductivity.[3-5] Specifically, tantalum (Ta) and tantalum nitride (TaN) films have recently attracted much interest in serving as future mainstream barrier layers.[2,6,7] It is well known that Ta forms no compound with Cu and that TaN possesses a dense microstructure as well as a high melting point of 3087°C. There are many studies concerning the barrier capability of Ta-based barrier layers between Cu and Si substrate[8-10] as well as Cu and SiO_2 dielectric.[11,12] However, no work has been reported on the study of integrating the barrier layers with Cu and low-K dielectrics.

Second, organic polymers that have K values between 2.0 and 3.0 entail attractive alternatives to SiO_2. However, there are still many reliability issues concerning material properties, such as low thermal stability, high thermal expansion coefficient, and low glass transition temperature that may raise concern about the film's mechanical strength during continuous high-temperature thermal cycles.[13,14] All these properties induce great challenges in process integration; nonetheless, their impacts on the device's electrical properties have seldom been explored.

In this work, we investigate the barrier effectiveness of very thin Ta and TaN films (25 nm) in Cu/barrier/low-K-dielectric/Si metal-insulator semiconductor (MIS) capacitors and propose a novel dielectric outgassing mechanism to clarify the premature degradation of Ta barriers.

Experimental

The samples used in this study were Cu/low-K-dielectric/Si MIS capacitors with and without a 25 nm thick Ta or TaN barrier layer sandwiched between the Cu and the low-K dielectric layers. Figure 1 shows the schematic cross section of the MIS samples. The low-K dielectric layers are Schumacher poly(arylene ether) (PAE-2, K = 2.8) films,[15] which were spin-on coated on a (100)-oriented p-type Si wafer to a thickness of 495 nm. A curing step was performed at 425°C in a 20% O_2/80% N_2 ambient to cross-link the PAE-2 that increased the glass transition temperature (T_g) and the structural rigidity above T_g. A Ta or TaN barrier layer of 25 nm thickness was sputter deposited on the PAE-2 dielectric layer using a dc magnetron sputtering system with a base pressure of 1-2 × 10^{-6} Torr and no intentional substrate heating. The Ta barrier was sputtered from a Ta target (purity 99.95%) in Ar ambient at a pressure of 7.6 mTorr, while the TaN barrier was reactively sputtered using the same Ta target in a gas mixture of Ar and N_2 with Ar/N_2 flow rates of 24/6 sccm at the same pressure of 7.6 mTorr.[16] Prior to each sputter deposition, the target was cleaned by presputtering with the shutter closed for 10 min. The Ta and TaN films were deposited at a sputtering power of 150 W, and the deposition rates of Ta and TaN were determined to be 21 and 16 Å/min,

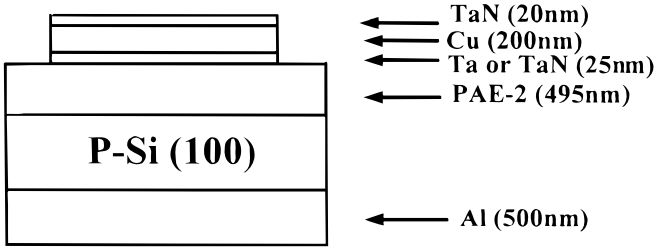

Figure 1. Schematic cross section of MIS samples studied in this work.

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respectively. After the barrier-layer deposition, Cu film of 200 nm thickness was deposited on the barrier metal without breaking the vacuum. Finally, the Cu surface was covered with a 20 nm thick TaN overlayer for the prevention of Cu oxidation in the subsequent high-temperature process. A lift-off process was used to define the metal gate in a circular area of 0.8 mm diam. For comparison, control samples with a dielectric layer of thermal SiO_2 (500 nm) in place of PAE-2 (TaN/Cu/(Ta, TaN)/SiO_2/Si) as well as control samples of Al-gated Al/PAE-2/Si structure were also prepared. Moreover, a 500 nm thick Al layer was deposited on the back side of Si substrates for all samples for a better contact in electrical measurements.

For the thermal stability study, the MIS capacitors were thermally annealed at various temperatures for 30 min in N_2 ambient. The time-zero dielectric breakdown of the low-K PAE-2 films was measured by applying a voltage ramp stress using an HP4145B semiconductor parameter analyzer with the MIS capacitors biased at accumulation polarity. The breakdown voltage (V_{bd}) is defined as the voltage at which the capacitor's leakage current density exceeds 1 nA/cm^2, and at least 25 capacitors were measured in each category to construct the breakdown statistics.

For material analysis, unpatterned samples of (Ta, TaN)/PAE-2/Si and TaN/Cu/(Ta, TaN)/PAE-2/Si structures were prepared. These samples were processed in the same process run with the MIS samples used for electrical measurements. Both film thickness and refractive index (RI) of the PAE-2 film were measured using a well-calibrated N&K analyzer at 6328 Å wavelength. X-ray diffraction (XRD) analysis using a 30 keV Cu Kα radiation was employed for phase identification. Field emission scanning electron microscopy (FESEM) was employed to observe the surface morphology and microstructure. Secondary ion mass spectroscopy (SIMS) was used to measure the elemental depth profiles. Fourier transform infrared spectroscopy (FTIR) as well as thermal desorption mass spectroscopy (TDS) was used to monitor the outgassing behavior of PAE-2 films during the thermal annealing process. The adhesion strength between barrier layer and PAE-2 was measured by a stud pull test using nail-shaped studs epoxy bonded to the Ta or TaN surface.

Results and Discussion

Physical property of PAE-2, Ta, and TaN.—Figure 2 shows the variation of thickness and refractive index of PAE-2 films thermally annealed at various temperatures. The film thickness remained nearly constant after thermal annealing at temperatures up to 450°C; however, it shrank fiercely after annealing at and above 500°C, implying the changes of film composition and bonding structure in the PAE-2 films. As for the refractive index, it remained nearly constant up to 500°C but increased drastically to a value of 1.80 after annealing at 600°C. We conclude that the intrinsic PAE-2 film is thermally stable at temperatures up to 450°C, which is the ultimate thermal annealing temperature at which the devices' electrical assessments were conducted.

The crystallographic structures of the as-deposited Ta and TaN barrier layers were identified to be β-Ta and cubic TaN, respectively, while the sheet resistances of the 25 nm thick Ta and TaN films were determined to be 72.3 and 1100 Ω/□, respectively. The atomic nitrogen concentration in the TaN film is about 20% as determined by Auger electron spectroscopy (AES) analysis. It was reported that β-Ta and cubic TaN phases exhibited superb barrier properties in the structures of Cu/(Ta, TaN)/p^+-n junction diodes[10] and Cu/(Ta, TaN)/SiO_2/Si MOS capacitors.[11]

TaN/Cu/PAE-2/Si capacitors.—Figure 3 illustrates the distributions of breakdown field for the Cu- and Al-gate MIS capacitors thermally annealed at various temperatures. The sample was considered a failure with a breakdown field less than 1 MV/cm. Compared with the Al-gate capacitors, severe degradation occurred for the Cu-gate capacitors annealed at 200°C, implying massive penetration of Cu into the PAE-2 layer, as confirmed by the results of SIMS depth profile measurements shown in Fig. 4. A substantial amount of Cu was found deep within the PAE-2 layer after 200°C annealing (Fig. 4b), leading to the failure of dielectric strength; the small amount of Cu presented in the as-deposited sample was presumably due to the knock-on effect of ion bombardment during the SIMS profiling.[17] The degradation of the breakdown field is generally believed to be correlated with Cu contamination in the dielectric layers, which may induce dielectric thinning[18-20] or result in increase of injection electron currents,[21-26] thus leading to poor breakdown strength. Figure 5 illustrates the SEM micrographs showing the surface morphology of TaN/Cu/PAE-2/Si samples annealed at 200 and 400°C. A large number of voids nonuniformly appeared on the topmost TaN surface (Fig. 5a), and the size of some voids enlarged as the annealing temperature was increased to 400°C (Fig. 5b). The results of electrical analyses indicated that the device failure was closely related to the formation of these voids.

TaN/Cu/(Ta, TaN)/PAE-2/Si capacitors.—Figure 6 illustrates the distribution of breakdown field for the Cu-gate capacitors having a

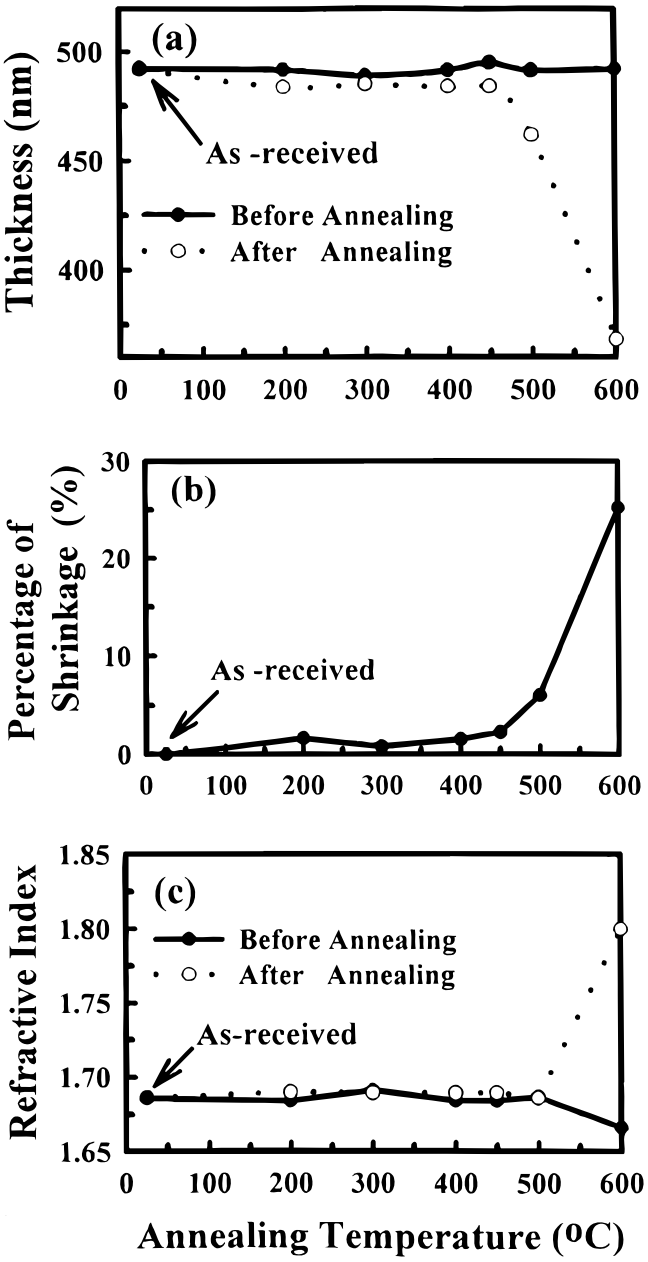

Figure 2. Variations of (a) thickness, (b) percentage shrinkage of thickness, and (c) refractive index of PAE-2 films annealed at various temperatures for 30 min in N_2 ambient.

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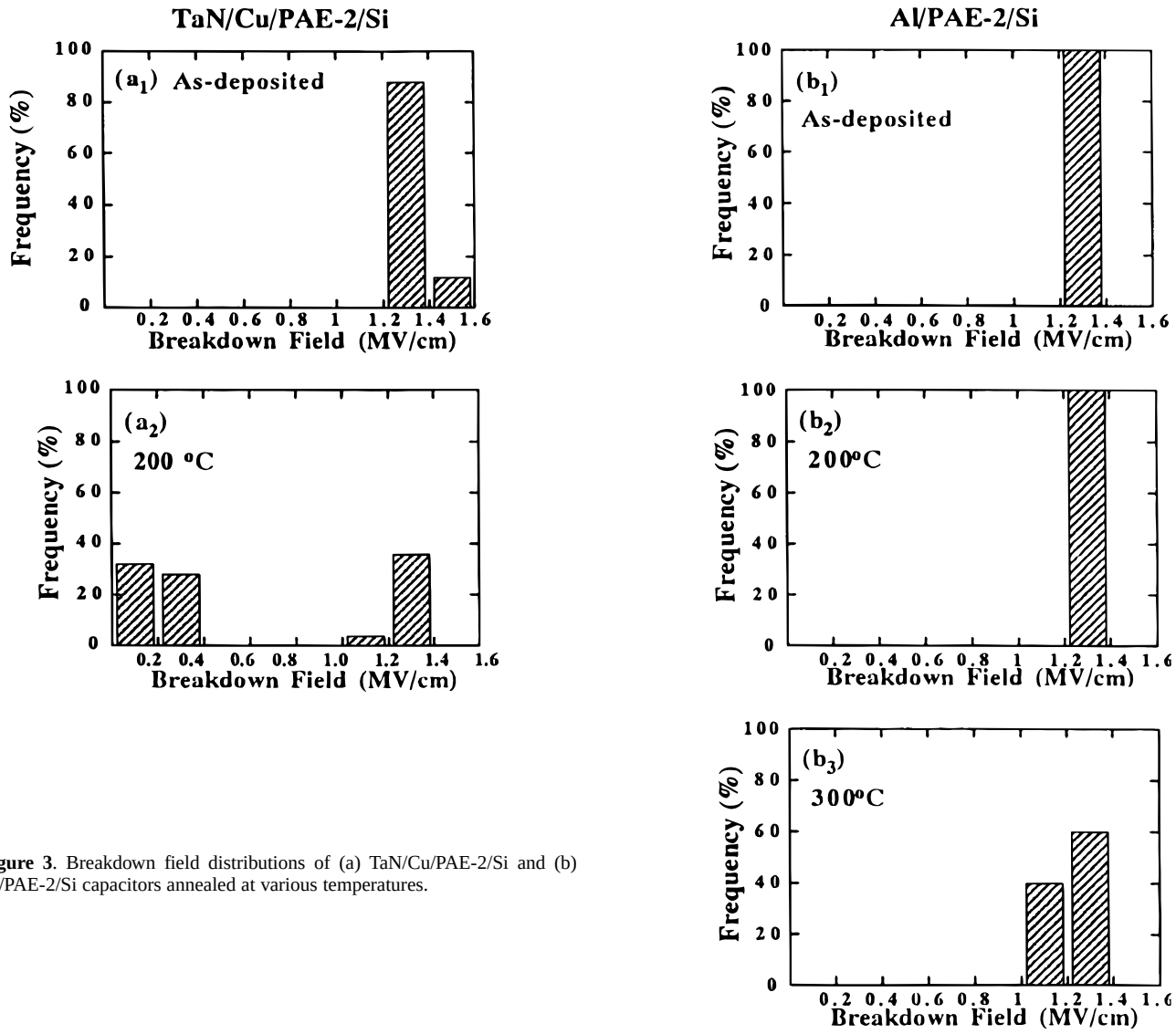

Figure 3. Breakdown field distributions of (a) TaN/Cu/PAE-2/Si and (b) Al/PAE-2/Si capacitors annealed at various temperatures.

25 nm thick Ta as well as TaN diffusion barrier. Compared with the samples without diffusion barrier, significant improvement in thermal stability was obtained, apparently due to the barrier effectiveness of Ta and TaN layers. In fact, it was reported that 25 nm thick Ta and TaN barriers in the structure of Cu/barrier/p^+n junction diodes can sustain a 30 min thermal annealing up to 550 and 750°C,

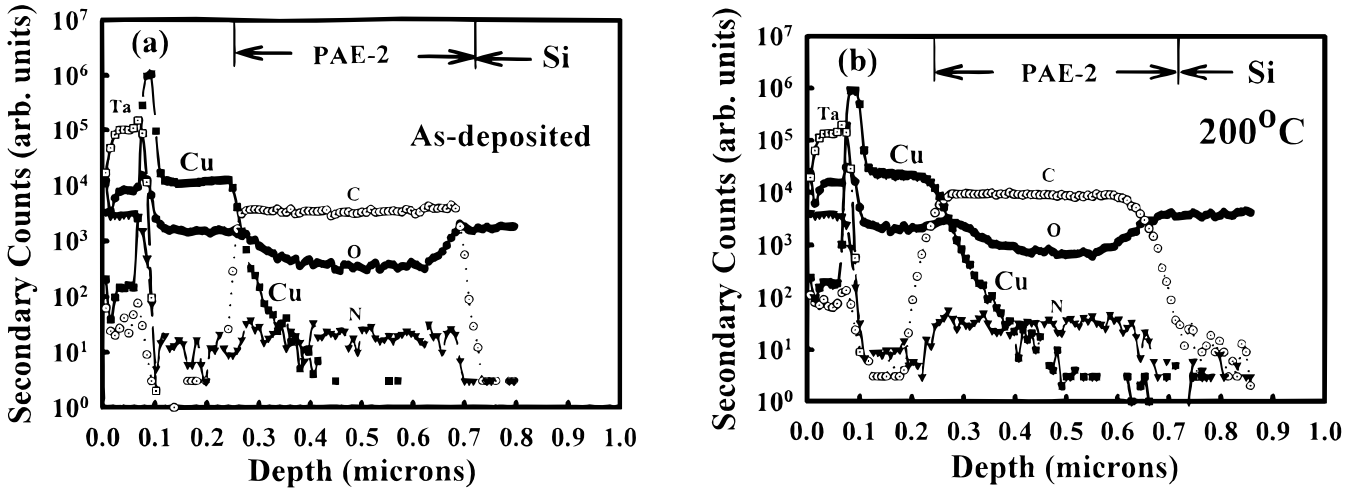

Figure 4. SIMS depth profiles of TaN/Cu/PAE-2/Si capacitor (a) as-deposited and (b) 200°C annealed.

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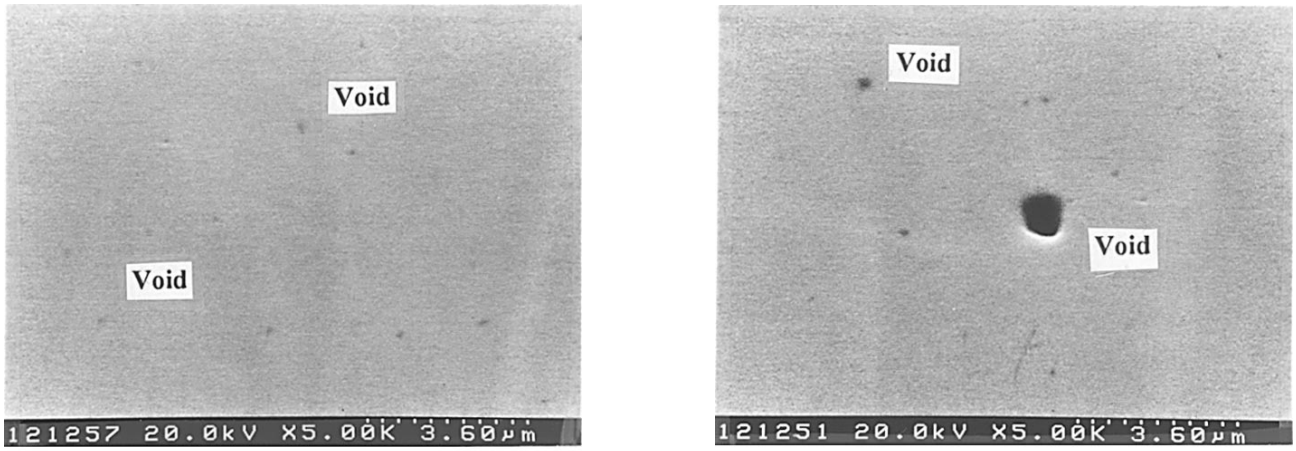

Figure 5. Top-view SEM micrographs showing the surface morphology of TaN/Cu/PAE-2/Si samples annealed at (a) 200 and (b) 400°C.

respectively, without causing degradation to the devices' electrical characteristics.[10] Thus, the premature degradation at 450°C for the TaN/Cu/Ta/PAE-2/Si MIS capacitor is believed to be associated with the thermal instability of the complex Ta/PAE-2 system. Figure 7 shows the SIMS depth profiles for the as-deposited as well as 450°C annealed TaN/Cu/Ta/PAE-2/Si capacitors. It can be seen that a substantial amount of Cu had permeated into PAE-2 (Fig. 7b). On the other hand, the SIMS depth profiles for the TaN/Cu/TaN/PAE-2/Si

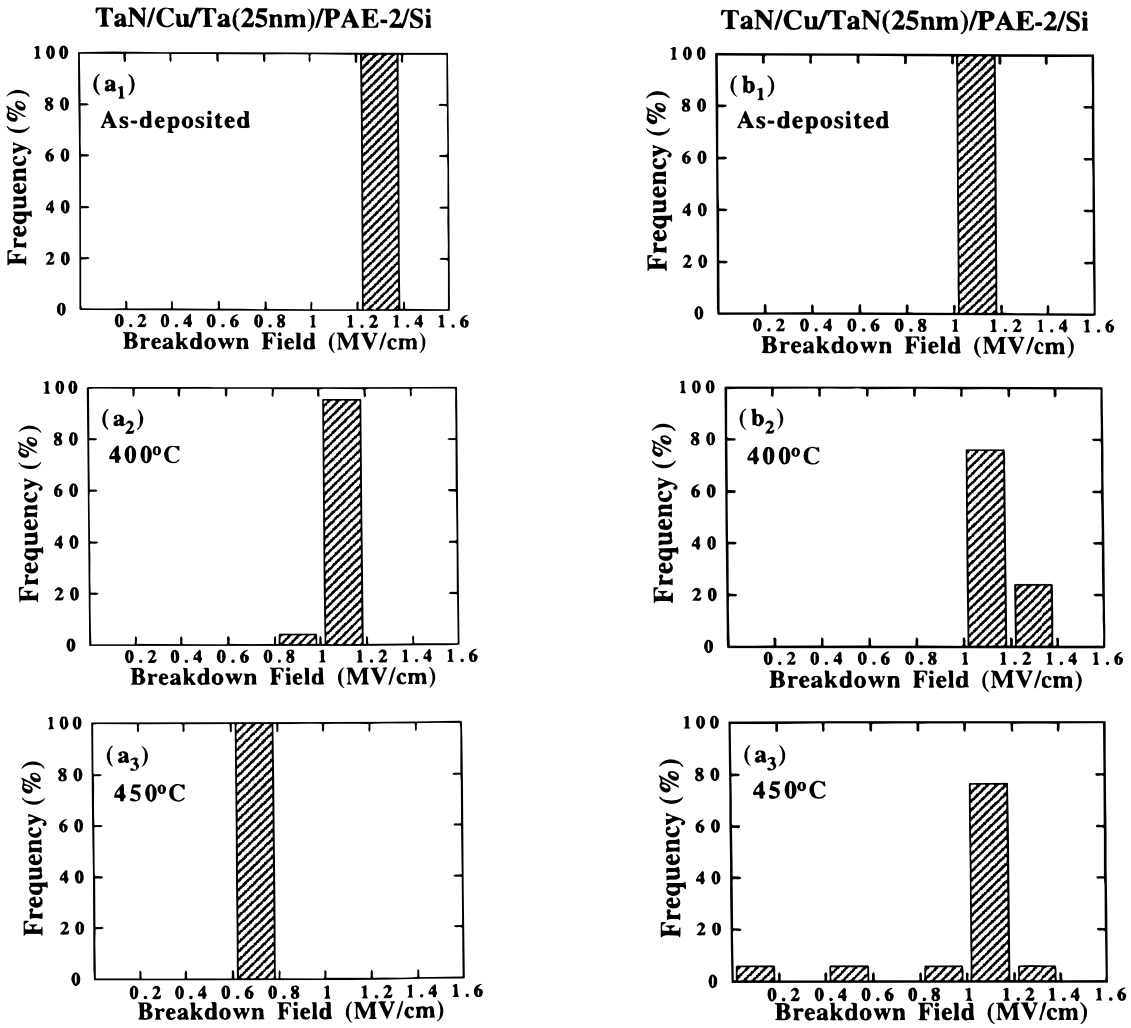

Figure 6. Breakdown field distributions of (a) TaN/Cu/Ta/PAE-2/Si and (b) TaN/Cu/TaN/PAE-2/Si capacitors annealed at various temperatures.

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samples annealed at the same temperature show much less permeation of Cu into PAE-2 (not shown). Figure 8 illustrates the scanning electron microscopy (SEM) micrographs showing the surface morphology of TaN/Cu/(Ta, TaN)/PAE-2/Si samples annealed at 450°C. Many voids were found on the surface of the TaN/Cu/Ta/PAE-2/Si sample, while few were found on the sample of TaN/Cu/TaN/PAE-2/Si. The temperatures at which these voids appeared coincided with the temperature of electrical degradations; similar coincidence was also observed for the samples without barrier layers, as shown in Fig. 5. Since device failure is closely related to the formation of the voids, one can infer that electrical degradation occurred in the TaN/Cu/Ta/PAE-2/Si sample annealed at 450°C. Figure 9 illustrates the SEM micrographs showing the surface morphology of TaN/PAE-2/Si and Ta/PAE-2/Si samples annealed at 450°C. The surface morphology of the TaN/PAE-2/Si sample remained stable after annealing at 450°C (Fig. 9a). However, blister- and/or knob-like artifacts were observed on the Ta surface for the 450°C annealed Ta/PAE-2/Si sample (Fig. 9b and c). We have found that the structure of Cu/(Ta, TaN)/SiO_2/Si was able to remain intact at temperatures up to at least 450°C, as confirmed by the results of breakdown field measurements shown in Fig. 10, indicating the superior stability of the (Ta, TaN)/SiO_2 system. There were reports that the blistering effect resulted in enhanced void formation in Al metal lines;[27-29] to the contrary, however, these local defects provided shortcuts for Cu permeation, leading to dielectric degradation.

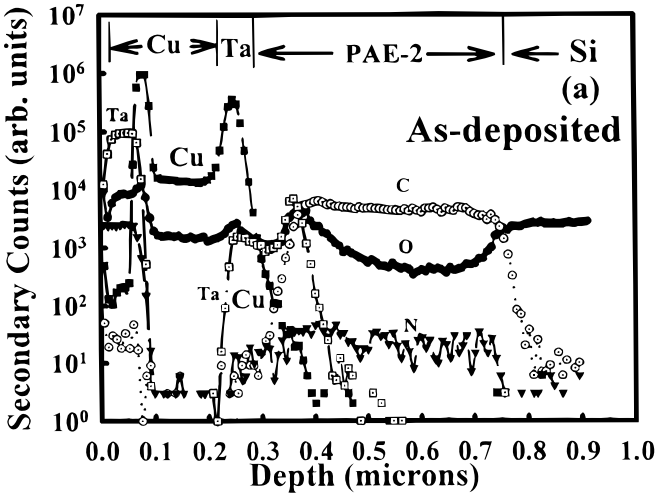

Figure 7. SIMS depth profiles of TaN/Cu/Ta/PAE-2/Si capacitor (a) as-deposited and (b) 450°C annealed.

TDS analysis.—To clarify this observed phenomenon, we propose a failure mechanism regarding the outgassing behavior of PAE-2 with respect to the strength of the adhesive force between the barrier and PAE-2. An interfacial pressure-cooking state under the Ta layer may be produced by a gaseous pressure originating from the massive outgassing of PAE-2 at 450°C, as confirmed from the measured TDS spectra shown in Fig. 11, wherein the primary peaks observed are H_2O with a major mass peak at 18 and H_2 with a major mass peak at 2. Small mass peaks were also observed at 28, 44, and 76. It can be seen from Fig. 11 that the desorption occurred at a temperature as low as 150°C and increased drastically at temperatures above 450°C. It should be noted that the desorption of water (H_2O) predominated among the outgassing species during the entire measurement period. The TDS measurement was conducted dynamically with a heating rate of 10°C/min except that the temperature of 420 as well as 500°C was held constant for 10 min each. Thus, the extent of outgassing should be more serious for the samples of PAE-2 MIS capacitor thermally annealed at 450°C for 30 min. The early deterioration of the barrier layer would occur provided the outgassing-induced gaseous pressure exceeded the yielding strength of the barrier layer. Because

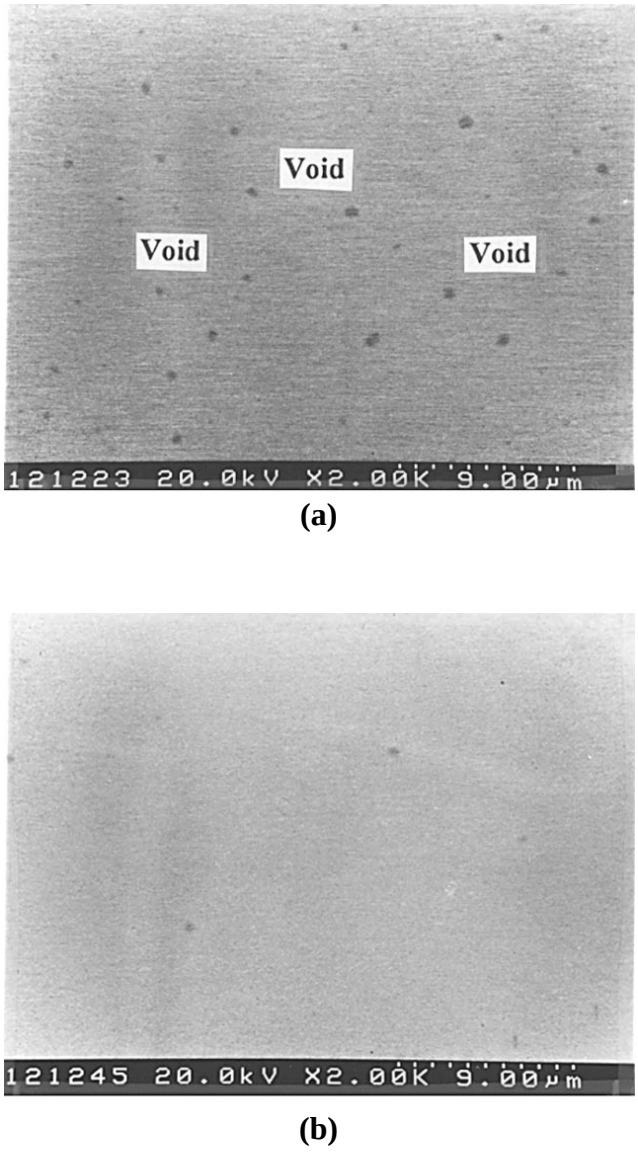

Figure 8. Top-view SEM micrographs showing the surface morphology of (a) TaN/Cu/Ta/PAE-2/Si and (b) TaN/Cu/TaN/PAE-2/Si samples annealed at 450°C.

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the upward gaseous stress forced the Ta film to deform downward and finally ruptured the surface, as shown in Fig. 9d, the impact that the gaseous pressure might have on the MIS sample studied may be governed by the adhesive force between the overlying barrier layer (Ta or TaN) and the underlying dielectric (*i.e.*, PAE-2). This inference was supported by the result of a pull test, which indicated that the adhesion between the TaN film and PAE-2 layer is much better than that between the Ta film and PAE-2 layer (average strength: 19.7 *vs.* 1.2 MPa). Thus, the result of electrical measurements that show the barrier capability of TaN films superior to that of Ta films is in complete accord with a stronger adhesive force between TaN and PAE-2 than that between Ta and PAE-2.

It was reported that the thermal stress induced from the mismatch of the thermal expansion coefficient caused voiding in metal lines and cracking in dielectric films.[13,14,27,28] The thermal stress cannot be ruled out from the possible cause of enhanced blister formation; however, further evidence is needed to confirm this point. This work investigates, in particular, a new mechanism of gaseous stress-induced voiding enhanced by massive outgassing of PAE-2 layer due to its low glass transition temperature (~290°C).[30]

Conclusion

Copper penetrates readily into PAE-2 dielectric and degrades its dielectric strength in the MIS capacitor of Cu/PAE-2/Si structure at temperatures as low as 200°C. We found that thin Ta and TaN films of 25 nm thickness are qualified to be effective barriers against Cu penetration at temperatures up to 400 and 450°C, respectively. Specifically, the TaN barrier is superior to the Ta barrier because of its resistance to outgassing-induced gaseous stress of PAE-2, which is believed to arise from stronger adhesion of TaN to PAE-2 than that of Ta to PAE-2, thus leading to better long-term reliability.

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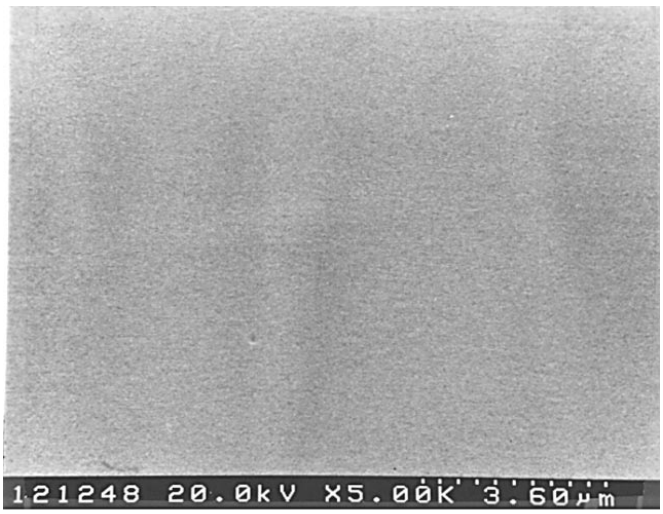
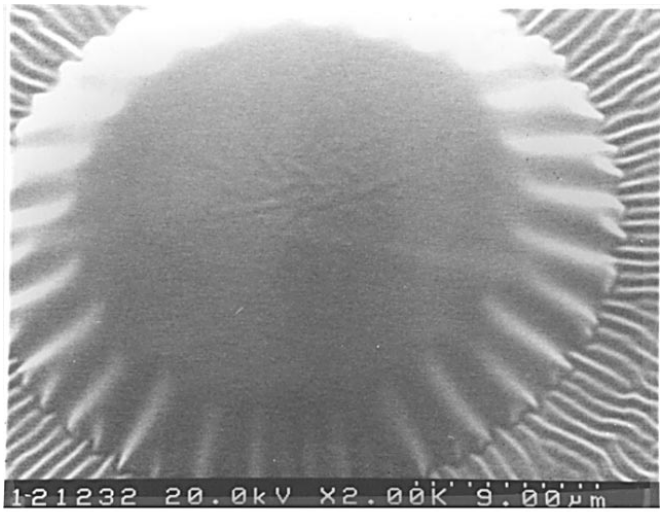
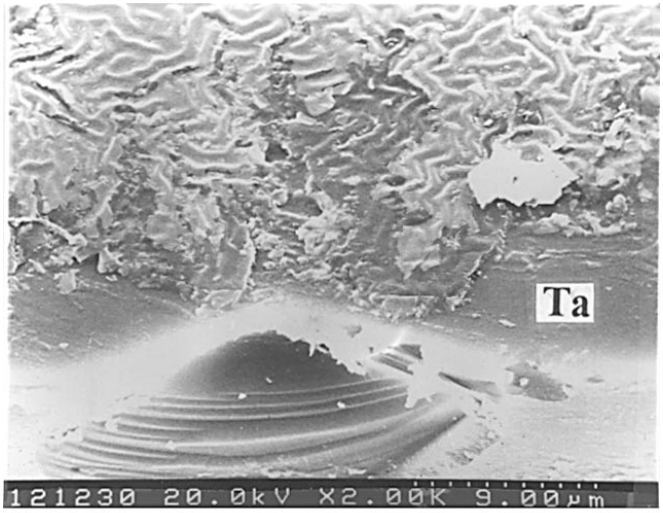


(a)

(b)



(c)



(d)

Figure 9. SEM micrographs of 450°C annealed (a) TaN/PAE-2/Si (top view), (b) and (c) Ta/PAE-2/Si (top view), and (d) Ta/PAE-2/Si (oblique view). The micrographs show blisters and knobs on the Ta surfaces.

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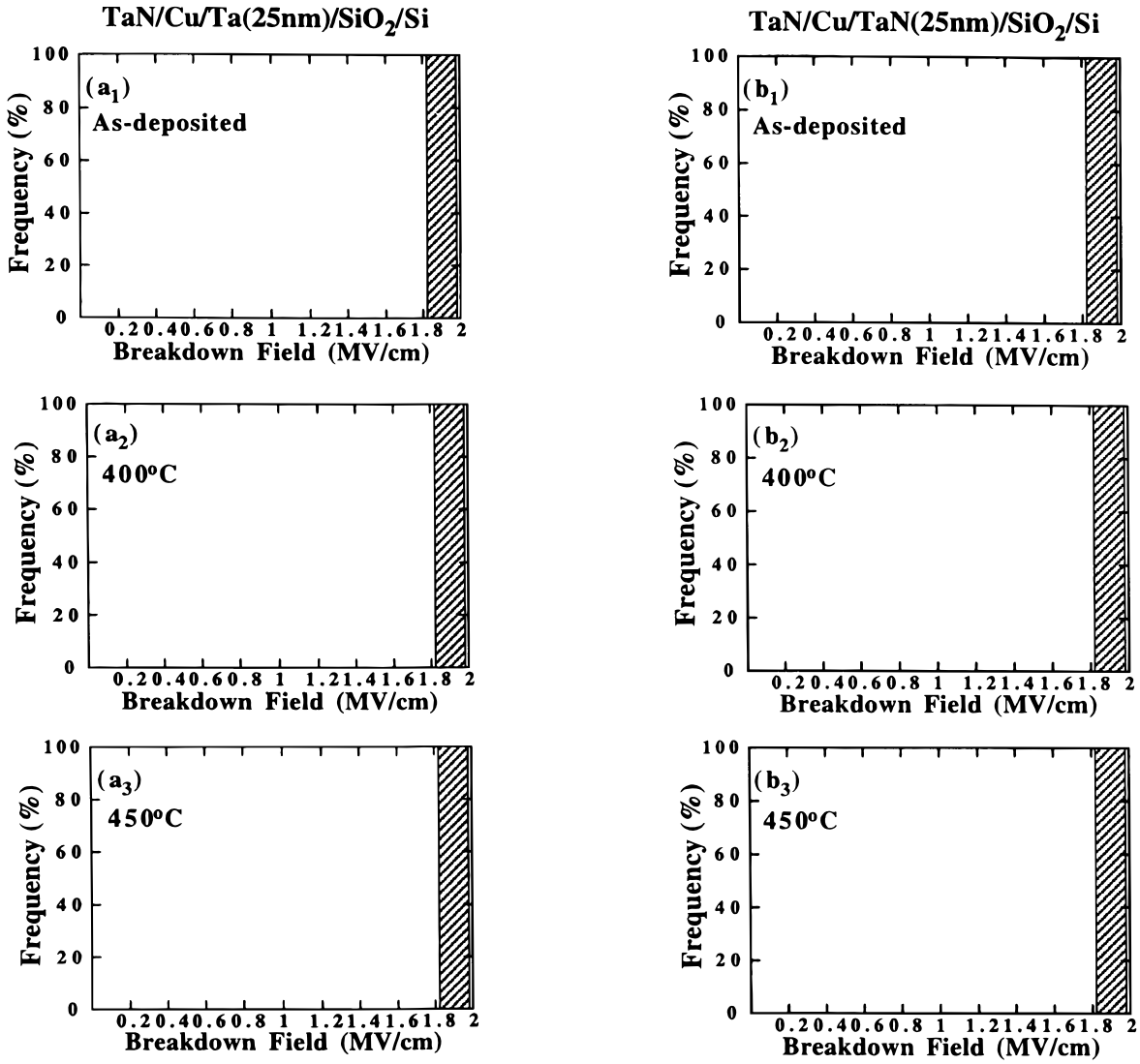

Figure 10. Breakdown field distributions of (a) TaN/Cu/Ta/SiO_2/Si and (b) TaN/Cu/TaN/SiO_2/Si capacitors annealed at various temperatures.

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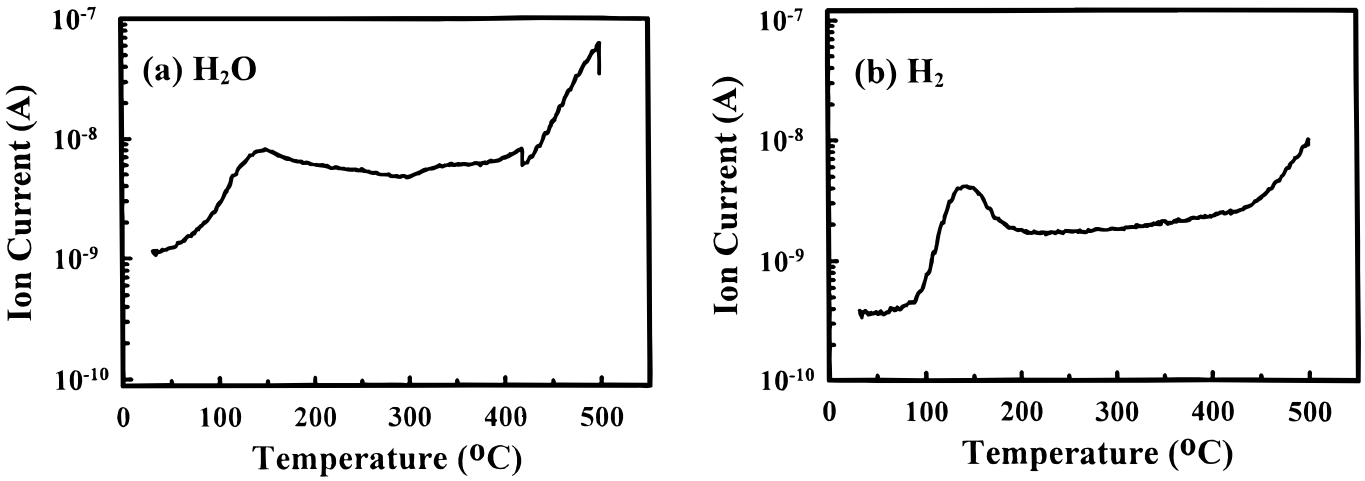

Figure 11. Typical TDS spectra of (a) H_2O and (b) H_2 obtained from the PAE-2 film.The PAE-2 film was fully cured at 425°C before the TDS analysis.

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