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Observation of carrier depletion and emission effects on capacitance dispersion in relaxed $In_{0.2}Ga_{0.8}As/GaAs$ quantum wells

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Strong changes in capacitance over frequency are found for highly relaxed $In_{0.2}Ga_{0.8}As/GaAs$ quantum well. The high-frequency dispersion is explained by a resistance–capacitance time constant effect due to the existence of a high resistive layer while the low-frequency dispersion is due to carrier emission from traps. The high-resistance layer is created by carrier depletion when InGaAs thickness increases beyond the critical thickness. Excellent agreement is found between the data from capacitance–frequency spectra and deep-level transient spectroscopy, permitting us to conclude that both the carrier depletion and emission effects observed in capacitance–frequency spectra are due to the existence of an acceptor trap at 0.33 eV. This trap is generated when the InGaAs thickness is beyond its critical thickness and is due to defect states associated with misfit dislocations. *© 1999 American Institute of Physics.*
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The InGaAs/GaAs material system has many important applications for electronic and optoelectronic devices. However, due to lattice mismatch between InGaAs and GaAs, there exists a critical thickness[1,2] of InGaAs beyond which strain relaxes accompanied by generation of misfit dislocations.[3–8] Carrier depletion[9,10] is found to accompany the generation of misfit dislocations. For highly relaxed samples, significant carrier depletion will result in an existence of a high-resistive layer which complicates characterizing techniques such as deep-level transient spectroscopy (DLTS). The *RC* time constant effect from the high-resistive layer may give rise to DLTS signals[11] and can be misinterpreted. We have previously observed DLTS signals due to the *RC* time constants from a high-resistive layer in low-temperature grown GaAs.[11] Therefore, in this investigation, we use admittance spectroscopy to characterize and derive its equivalent circuit model for highly relaxed InGaAs/GaAs quantum well.

The $In_{0.2}Ga_{0.8}As/GaAs$ quantum well structures with different $In_{0.2}Ga_{0.8}As$ well width were grown on n^+-GaAs (001) substrates by Varian Gen II molecular beam epitaxy. The InGaAs quantum well was 0.3 μm from the Schottky surface. Both the InGaAs quantum well and the total 0.6-μm-thick GaAs epilayer were Si doped with a concentration of 6×10^{16} cm^{-3}. The whole structure was grown at 550 °C. The thickness and composition of InGaAs were determined by oscillation of reflection high energy electron diffraction and cross-sectional transmission electron microscopy (TEM). Schottky diodes were fabricated by evaporating Au on samples with a dot diameter of 1500 μm. A HP4194 gain-phase analyzer was used to measure the capacitance–frequency (C–F) spectra. The small signal oscillation level was kept at 100 mV.

Figure 1 shows the C–F spectra measured at $V=-0.5$ V for samples with InGaAs well widths of 100 and 1000 Å. In contrast to the 100 Å sample, a significant decrease in capacitance with increasing frequency can be seen for the 1000 Å sample. To understand the origin of this capacitance drop, let us examine their apparent carrier concentration as shown in the inset, which was derived from capacitance–voltage data. In contrast to the 100 Å case where a carrier confinement in the quantum well can be seen, a significant carrier depletion is observed for the 1000 Å case. The critical thickness for our samples was between 200 and 300 Å determined from x-ray diffraction.[10] This carrier depletion for the 1000 Å case is so significant that it goes beyond the quantum well region and spreads to GaAs layers on both sides.

For the 1000 Å sample, an acceptor level is assumed to account for the significant carrier depletion which produces a relatively high-resistance layer at the vicinity of the InGaAs region. A band diagram pertaining to this effect is shown in Fig. 2(a), which contains a Schottky barrier and a high-resistive layer which can be represented by a large resistance R in parallel with capacitance C_r. This circuit is then connected in series with the Schottky depletion capacitance C_D. The carrier emission from the acceptor traps is represented by R_t and C_t, which are in parallel with C_D. The emission

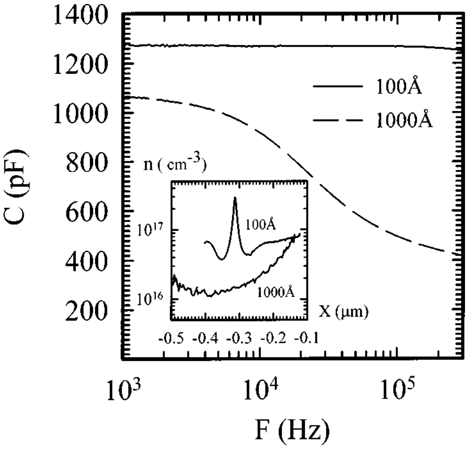

FIG. 1. The frequency-dependent capacitance measured at $V=-0.5$ V for $In_{0.2}Ga_{0.8}As/GaAs$ quantum well with InGaAs well widths of 100 and 1000 Å. The inset shows their corresponding apparent carrier concentrations.

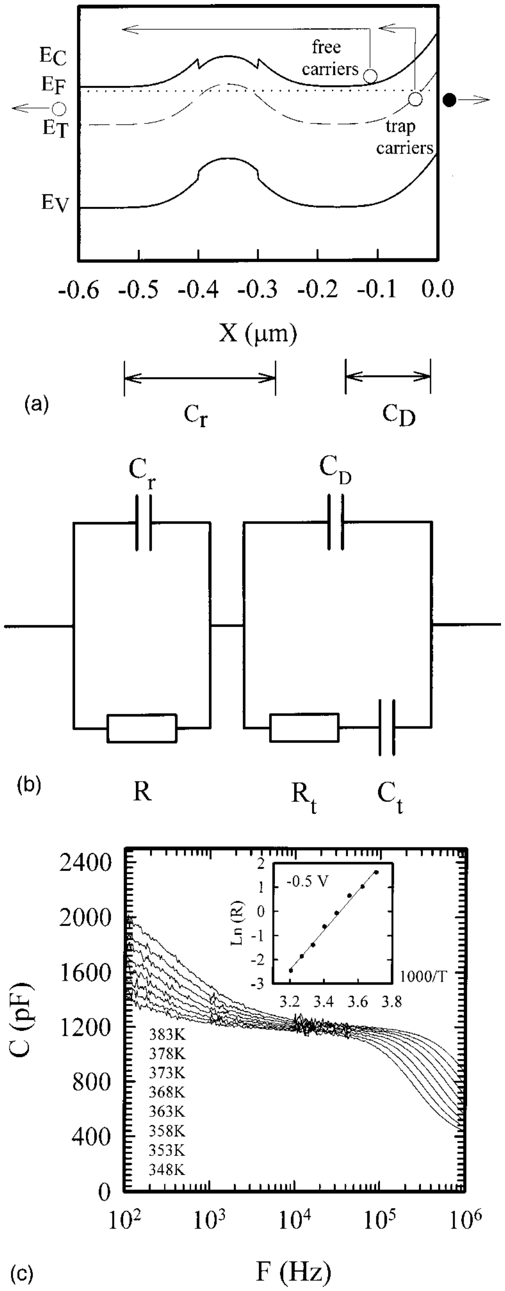

FIG. 2. (a) A band diagram for the 1000 Å sample. Significant carrier depletion introduces a high-resistance layer at the vicinity of the InGaAs region. (b) The overall equivalent circuit. (c) The *C–F* spectra as a function of temperature for the 1000 Å sample. An activation energy of 0.33 eV is obtained and is shown in the inset.

time constant of the trap is $\tau_t = R_t C_t$. The overall equivalent circuit is shown in Fig. 2(b).

The equivalent circuit in Fig. 2(b) will give rise to two capacitance trapping effects as shown in Fig. 2(c). At high frequencies where $1/\omega \ll (C_d + C_r)R$, the high-resistive layer behaves as a perfect insulator because free carriers cannot follow the frequency to traverse through it; the observed high-frequency capacitance C_h should be the series combination of C_D and C_r. From Fig. 1, C_h is about 400 pF corresponding to 0.51 μm which, as expected, is less than the total epitaxial thickness of 0.7 μm. At middle frequencies where $1/\omega \gg R(C_d + C_r)$ and $1/\omega \ll \tau_t$, the free carriers can traverse through the high-resistive layer so that the observed mid-frequency capacitance should be the Schottky depletion capacitance C_D. Figure 1 shows C_D is about 1200 pF which corresponds to a thickness of 0.17 μm. As a result, the effective thickness of the high-resistive layer is 0.25 μm obtained from C_r using $C_h = C_D C_r / (C_D + C_r)$. These values allow us to construct the band diagram as in Fig. 2(a). At low frequencies where $1/\omega \gg \tau_t$, carriers can emit from traps and traverse through the high-resistive layer, contributing to additional low-frequency capacitance.

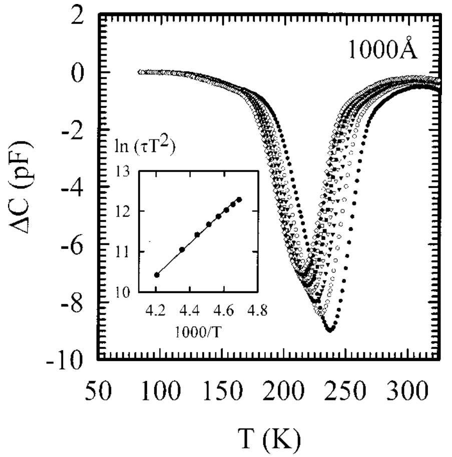

FIG. 3. The DLTS spectra for the 1000 Å sample taken by sweeping voltage from 0 to -4 V with the fill time set at 5 s at 0 V. The rate window is 0.59, 1.18, 1.78, 2.37, 2.97, 3.56, 4.16, and 4.75 s^{-1} for each curve. Shown in the inset is the modified emission time τT^2 vs $1000/T$, an activation energy of 0.33 eV (capture cross section $= 8 \times 10^{-16}$ cm^2) was obtained.

As discussed above, the *C–F* spectra show two inflexion frequencies at which the capacitance drops from high to low plateaus. The high-frequency inflexion frequency ω corresponds to a *RC* time constant effect: $\omega = 1/R(C_d + C_r)$. By fitting to the experimental data in Fig. 2(c), we obtained $R = 3000\ \Omega$ for $T = 308$ K, which is close to a series resistance of 2800 Ω obtained from fitting the forward current–voltage *(I–V)* bending at large voltage by using $I = I_s \exp[q(V - RI)/nkT]$. The slightly large R from the inflection frequency may result from a reverse bias used for the admittance measurement while a forward bias is applied for *I–V* fitting where the effect of carrier injection cannot be neglected. The activation energy of R determined from its Arrhenius plot was 0.33 eV.

Assume R is limited by the bulk-limited conduction, that is, $R = d/e\ \ \mu nA$, where d is the effective thickness of the high-resistive layer and μ is the electron mobility. The high-resistance layer originates from a carrier depletion due to an acceptor trap level. If the acceptor concentration is larger than the shallow donor concentration (6×10^{16} cm^{-3}), the Fermi level is almost pinned to the acceptor level; the activation energy (0.33 eV) of R should be close to the energy position of the acceptor level. We will discuss this point further later.

Figure 2(c) shows that the low-frequency inflection capacitance cannot be accurately determined because the low-frequency capacitance plateau cannot be clearly seen. But we can estimate the range of the inflection frequency, for example, at $T = 383$ K which should be between 100 and 1000 Hz, corresponding to a time constant τ between 3.2×10^{-3} and 3.2×10^{-4} s. In order to prove whether this is the emission time constant for the traps, Fig. 3 shows the DLTS spectra measured by a HP4194 gain-phase analyzer by sweeping voltage from 0 to -4 V with the fill time set at 5 s at 0 V. It can be seen that the sample has a dominating DLTS signal at around 200 K, which was also observed for samples with InGaAs thickness of 300 and 400 Å but was absent for samples with InGaAs thicknesses of 100 and 200 Å, which are below the critical thickness. By plotting the modified emission time τT^2 vs $1000/T$, as shown in the inset, the activation energy (capture cross section) was determined to be 0.33 eV (8×10^{-16} cm^2). Because this trap exists only when the InGaAs thickness is beyond the critical thickness, it should be associated with defect states related to misfit dislocations introduced by lattice relaxation. By extrapolating the time constant from DLTS, the time constant τ_t at $T = 383$ K was estimated to be about 5×10^{-4} s which is close to τ (between 3.2×10^{-3} and 3.2×10^{-4}) estimated from low-frequency inflection frequency in C–F spectra. This agreement supports that the low-frequency capacitance trapping is due to the emission of carriers from traps. In addition, the activation energy of the trap determined from DLTS is equal to that of R, indicating that the carrier depletion in relaxed $\mathrm{In_{0.2}Ga_{0.8}As/GaAs}$ quantum well is due to the same trap at 0.33 eV. This trap is thought to be the trap at 0.395 eV ($\sigma = I\times 10^{-16}$ cm^2) observed by Uchida, Kakibayashi, and Goto[9] in their $\mathrm{In_{0.2}Ga_{0.8}As/GaAs}$ system, which is created when the InGaAs thickness increases beyond its critical thickness and is due to the defect states related to misfit dislocations.

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