H_2/O_2 Plasma on Polysilicon Thin-Film Transistor

Horng Nan Chern, Chung Len Lee, *Member, IEEE,* and Tan Fu Lei

Abstract—**This letter reports that the H_2 plasma followed by the O_2 plasma is more effective to passivate grain boundary states in the polysilicon thin film. Polysilicon thin-film transistors (TFT's) made after applying H_2/O_2 plasma treatment can exhibit a turn-on threshold voltage of -0.1 V, a subthreshold swing of 0.154 V/decade, an ON/OFF current ratio I_{on}/I_{off} over 1×10^8, and an electron mobility of 40.2 $cm^2/V \cdot s$.**

I. INTRODUCTION

MANY techniques have been investigated to improve the electrical characteristics of polysilicon thin-film transistors (TFT's). One of the methods to reduce the defect states at the grain boundaries is to apply the H_2 plasma treatment on the polysilicon film [1]. Recently, it has been found that treatment by O_2 plasma can enhance the hydrogen passivation of the polysilicon defects [2]. This paper reports that by jointly applying the H_2 and O_2 plasma treatment to polysilicon TFT's, significant improvement in their characteristics can be obtained.

II. EXPERIMENTS

Amorphous silicon films of 600 Å thickness were deposited on thermally oxidized silicon wafers by a low-pressure chemical vapor deposition (LPCVD) system at 550°C. The wafers were then annealed at 550°C for 48 h to transform the film to polysilicon. After defining the active islands, 385-Å gate oxide was grown in dry O_2 at 1000°C. Another 3500-Å-thick polysilicon film was then deposited at 625°C by the LPCVD system for the gate electrode. A self-aligned phosphorous implantation of a dose of 5×10^{15} cm^{-2} was performed to form the source, drain, and gate electrodes. The dopants were activated at 900°C for 30 min in nitrogen gas. Hydrogenation was performed in a commercial 13.5-MHz parallel-plate plasma reactor at 300°C for 30 min with a power density of 0.7 W/cm^2 in H_2 and N_2 gas (80 sccm/80 sccm) mixture at 0.1 torr. The wafers were then subjected to an O_2 plasma treatment in the same plasma system at 300°C for 30 min with the same power density. For comparison, some wafers were subjected to H_2 or O_2 plasma treatment only. All wafers were covered with 5000-Å plasma-enhanced chemical vapor deposition (PECVD) SiO_2 for passivation. Contact holes were opened, and Al was deposited and then patterned. Finally, some of the wafers were annealed in N_2 ambient at 400–500°C for 15–30 min.

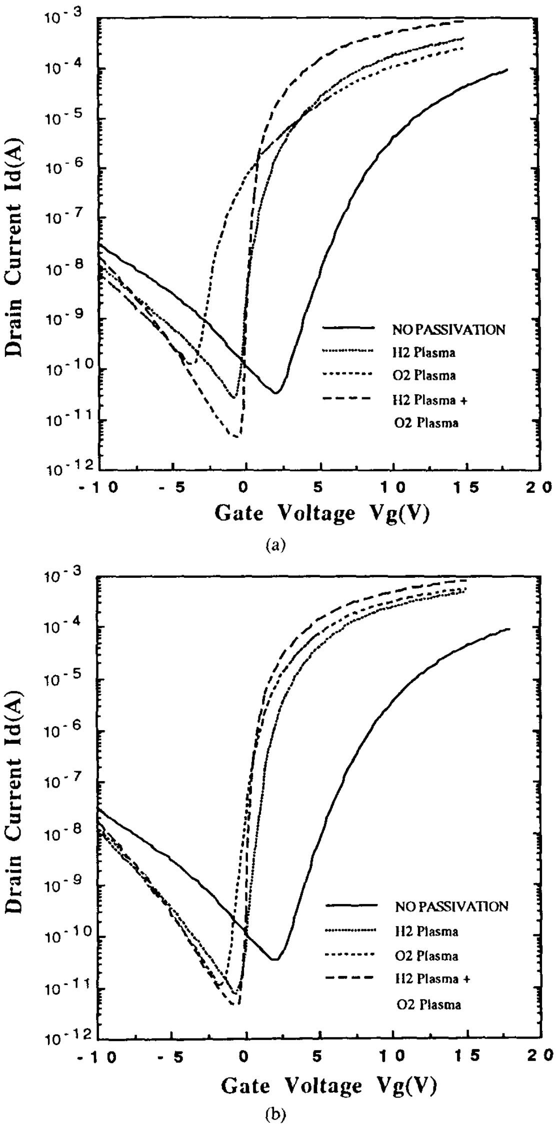
III. RESULTS AND DISCUSSIONS

Fig. 1 shows the typical I_d–V_g characteristics at $V_d = 5$ V of polysilicon TFT's which were treated with H_2, O_2, H_2/O_2, and without plasma treatment, respectively. It is seen that the H_2/O_2-plasma-treated device exhibits the best characteristics. The devices with O_2 plasma treatment also show better performance than those without plasma treatment. Table I shows the threshold voltage (V_{th}), the subthreshold swing (S), I_{on}/I_{off}, the minimum leakage current (I_{off}), and the mobility (μ) derived from the I_d–V_g characteristics of the devices annealed at 400°C for 15 min. More than two times of magnitude improvement on I_{on}/I_{off} and S have been obtained for the H_2/O_2-plasma-treated device over the other devices. Also, much improvement on V_{th}, I_{off}, and μ was obtained. In a previous work [2], it was reported that O_2 plasma treatment can enhance the hydrogen effect to reduce the dangling bonds in the succeeding H_2–N_2 annealing step. However, our O_2-plasma-treatment device which was not annealed in an H_2-rich ambient also shows passivation effects. Hence, the passivation effect of the O_2 plasma treatment is not only caused by hydrogen atoms but also caused by oxygen atoms. Also, when these O_2-plasma-treated devices were subjected to thermal annealing at 450–500°C for 30 min, they exhibited a better stability than the H_2-plasma treated devices. It is suggested that during the O_2 plasma treatment process, the negatively charged atoms (O^- and O^{2-}) diffuse through the polysilicon layer under the attraction of positively charge Si ions [3] and passivate the dangling bonds of grain boundaries of the active polysilicon layer. For our devices the *CV* measurement did not show any detectable thickness difference on the gate oxide thickness, although it had been reported that a thin oxide layer would be formed on the surface after O_2 plasma treatment [3]. Hence, by applying O_2 plasma to H_2-plasma-treated devices, there are two passivation effects to reduce the dangling bonds of grain boundaries. One is the passivation effect by oxygen atoms themselves and the other is the enhanced passivation effect of the existing hydrogen by O_2 plasma treatment [2]. Therefore, the performance of polysilicon TFT's can be improved significantly by applying H_2/O_2 plasma treatment.

Manuscript received September 9, 1992; revised December 10, 1992. This work was supported by the National Science Council of The Republic of China through Contract NSC-81-0404-E009-138.

The authors are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, Republic of China.

IEEE Log Number 9207335.



(a)

(b)

Fig. 1. The I_d–V_g characteristics at the drain voltage $V_d = 5$ V of polysilicon TFT's with the H_2, the O_2, the H_2/O_2 plasma treatment and without plasma treatment, respectively. The devices were treated at (a) no thermal annealing, and (b) 400°C for 15 min annealed. All devices were measured at the dimension of $W/L = 40\ \mu m/10\ \mu m$.

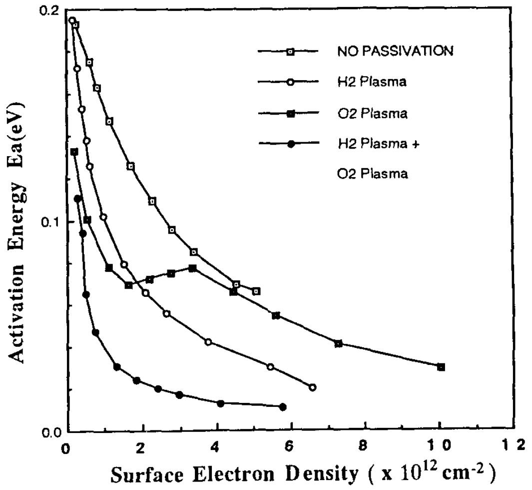


Fig. 2. The activation energy curves of the drain currents for the devices of Fig. 1(a) plotted in terms of the surface electron density $N_S = C_{ox}(V_g - V_{th})/q$. Data were measured at $V_d = 0.1$ V in the temperature range of 20 to 150°C.

TABLE I

THE VALUES OF THE DEVICE PARAMETERS OF POLYSILICON TFT'S WITH THE H_2, THE O_2, THE H_2 / O_2 PLASMA TREATMENT, AND WITHOUT ANY PLASMA TREATMENT

The devices were annealed at 400°C for 15 min. The threshold voltage is extracted from the $I_d^{1/2}$–V_g plot by operating the device in the saturation region. The mobility is derived from the I_d–V_g characteristics in the linear region.

Parameters / Condition	V_{th}(V)	S (V/dec)	I_{on}/I_{off}	I_{off} (pA)	Mobility ($cm^2/V \cdot s$)
No Plasma treatment	6.50	1.040	4.0×10^5	33.1	10.8
H_2 Plasma treatment	0.75	0.338	3.0×10^7	7.5	29.6
O_2 Plasma treatment	0.01	0.367	2.1×10^7	10.3	30.0
H_2 Plasma + O_2 Plasma treatment	−0.10	0.154	1.1×10^8	3.8	40.2

The temperature dependence of the drain current of all devices was also measured in the temperature range from 20 to 150°C at $V_d = 0.1$ V. The activation energies of the drain current were derived and plotted in Fig. 2 in terms of the surface electron density, $N_S = C_{ox}(V_g - V_{th})/q$, where C_{ox} is the capacitance of the gate oxide, V_g is the gate voltage, and q is the electron charge [4]. The value of the activation energy reflects the carrier transport barrier of the grain boundary of the channel polysilicon film [5]. It is seen that the H_2/O_2 plasma treatment is more effective to passivate defect states of the grain boundaries than those with H_2 or O_2 plasma treatment only. It is noted that for no thermally annealed devices, the activation energy of the O_2-plasma-treated device behaves much differently from that of the H_2 or H_2/O_2-plasma-treated devices. In the range of N_S less than 2×10^{12} cm^{-2}, the activation energy is lower than that of H_2-plasma-treated devices. This is consistent with the result that the O_2 plasma-treated devices exhibit a smaller deep-state density determined by the method of the field effect conductance [6] than the H_2-plasma-treated devices. Furthermore, within the N_S range of 2×10^{12} to 3.5×10^{12} cm^{-2}, the activation increase, and after 3.5×10^{12} cm^{-2}, the activation energy decreases again. This is believed to be due to the existence of some kind of band-tail states, created by the O_2 plasma treatment. As the surface electron density is larger than 2×10^{12} cm^{-2}, the Fermi level reaches the energy level of these states and these states are occupied with electrons. At this point, the barrier height at the grain boundaries increase, and the drain current has a higher activation energy. The existence of these band-tail states can also be observed by noting in Fig. 1(a) the highest value of I_{off} among the four devices. These states increase the level-assisted thermionic field emission between grain boundaries, and thus increase the I_{off} current [4]. They could be easily annealed out through a thermal treatment. In our experiments, it had been found that a 400°C thermal annealing in N_2 decreased the I_{off} value to a level lower than that of the unplasma-treated device, and the phenomenon of the increase at the activation energy curve disappeared. In the activation energy curve of the H_2/O_2-plasma-treated device shown in Fig. 2, the behavior of the O_2-plasma treated device described above is not observed. This indicates that the O_2-plasma treatment after the H_2-plasma treatment does not produce tail states, but on the contrary, it helps to passivate grain boundary states more effectively.

IV. CONCLUSIONS

This letter reports that the H_2 plasma treatment followed by O_2 plasma treatment is much more effective to passivate grain boundary states in polysilicon thin films. The O_2 plasma treatment following the H_2 plasma treatment helps the H atom to reduce grain boundary states and thus improves the device performance. The polysilicon TFT's made after applying the H_2/O_2 plasma treatment exhibit a superior performance than those by applying the H_2 plasma treatment or the O_2 plasma treatment only. The TFT with the H_2/O_2 plasma treatment can achieve a V_{th} of −0.1 V, S of 0.154 V/decade $I_{\mathrm{on}}/I_{\mathrm{off}}$ over 8 decades, and mobility of 40.2 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$.

REFERENCES

[1] I. Yudasaka and H. Ohshima, "Polysilicon thin film transistor," *Mater. Res. Soc. Symp. Proc.*, vol. 182, p. 333, 1990.

[2] S. Ikeda *et al.*, "A polysilicon transistor technology for large capacity SRAM," in *IEDM Tech. Dig.*, 1990, p. 469.

[3] H. Kinoshita, "Low-energy ion etching and oxidation of Si in O_2 magnetron plasma," *Appl. Surf. Sci.*, vol. 33/34, p. 1101, 1988.

[4] I. W. Wu, T. Y. Huang, W. B. Jackson, A. G. Lewis, and A. Chiang, "Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation," *IEEE Electron Device Lett.*, vol. 12, p. 181, 1991.

[5] T. Kamins, *Polysilicon Silicon for Integrated Circuit Application.* Boston: Kluwer Academic, 1988.

[6] G. Fortunato and P. Migliorato, "Determination of gap state density in polycrystalline silicon by field-effect conductance," *Appl. Phys. Lett.*, vol. 49, p. 1025, 1986.