Suppression of Boron Penetration for p^+ Stacked Poly-Si Gates by Using Inductively Coupled N_2 Plasma Treatment

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***Abstract*— Nitridation of the stacked poly-Si gates by the inductively coupled N_2 plasma (ICNP) treatments has been shown to suppress the boron penetration and improve the gate oxide integrity. The ICNP treatments on the stacked poly-Si layers would create the nitrogen-rich layers not only between the stacked poly-Si layers but also in the gate oxide after post implant anneal, thus resulting in effective retardation of boron diffusion. In addition, the position of ICNP treatment closer to gate oxides leads to higher nitrogen peaks in the gate oxide region, resulting in further suppression of boron penetration and improvement of gate oxide reliability.**

I. Introduction

SURFACE-CHANNEL p-MOSFET's with p^+ poly-Si gates have been investigated [1] in place of the buried-channel devices with n^+ poly-Si gates due to superior short-channel behavior, better turnoff characteristics, lower threshold voltage operation, much less sensitivity to process tolerances [2], and improved hot-carrier reliability [3]. However, it has been reported that boron impurities from the B^+-doped poly-Si gate could readily diffuse through the gate oxide during high-temperature anneals [4], [5]. This boron penetration can result in flat-band voltage $(V_{\rm fb})$ shift, increase of the subthreshold swing and leakage current, and deterioration of the gate oxide quality. Therefore, different structures have been investigated, such as the as-deposited a-Si gates [6] in place of the poly-Si gate, the stacked a-Si (or poly-Si) gate structure [7]–[9], nitrogen implantation into the gate electrodes [10]–[12], and various nitridized gate oxides [13]–[15], to retard the boron diffusion into underlying Si substrates. However, for the process of NH_3-nitridized stacked poly-Si gates [9], nitrogen is incorporated into poly-Si gates by extra high-temperature NH_3-annealed process, which is not suitable as the process temperature is decreased for the future deep-submicron technology.

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In this paper, nitridation at the interfaces of stacked poly-Si gates by the inductively coupled N_2 plasma (ICNP) treatment is proposed to suppress the boron penetration and improve the integrity of gate oxides, by creating the nitrogen-rich layers not only between the stacked layers but also in the gate oxide. Furthermore, no extra thermal cycles are applied to the samples during the ICNP process. Hence, the ICNP treatment at the interface of stacked poly-Si gates is attractive to provide nitrogen incorporation without extra thermal cycles in the advanced CMOS technology.

II. Experiments

We used (100) oriented, $3 \sim 5\ \Omega$-cm, n-type Si wafers. Field oxides of 450 nm thickness were thermally grown for patterning the active regions of MOS capacitors. Thin gate oxides of about 7.5 nm thickness were grown at 900 °C in a dry O_2 ambient. Immediately, an undoped poly-Si film with a total thickness about 200 nm was deposited for all the samples by low-pressure chemical-vapor-deposition (LPCVD) at 620 °C in three steps: 50 nm first deposition, followed by 50 and 100 nm deposition, accordingly. During the stacked poly-Si deposition process, some samples were nitridized by inductively coupled plasma (ICP) system, either between the first and the second layers (PNPP) or between the second and the third layers (PPNP) of poly-Si. The experimental procedure was shown in Fig. 1. The N_2 plasma exposure for all the treated samples was operated at RF power of 200 W and flow rate of 40 sccm for 10 min. For comparison, some samples with the same stacked poly-Si gate but without the nitridation (PPP) were also fabricated. To remove the native oxide at the interfaces of stacked layers, all the samples were soaked in diluted HF between the stacked poly-Si deposition. Then, all the specimens were BF_2^+-implanted at 40 keV to a dose of 5×10^{15} cm^{-2}. Post implant anneal was via furnace annealing (FA) at an annealing temperature of 900°C for 30 min. After that, Al was deposited and sintered at 400 °C in N_2 for 30 min to form capacitors. The resultant integrity of gate oxides was characterized by conductance–voltage (I–V) and capacitance–voltage (C–V) measurements, respectively.

III. Results and Discussion

The SIMS boron and nitrogen profiles of the PPP, PPNP, and PNPP samples, respectively, annealed at 900°C for 30 min were illustrated in Fig. 2. The nitrogen peaks of PPNP

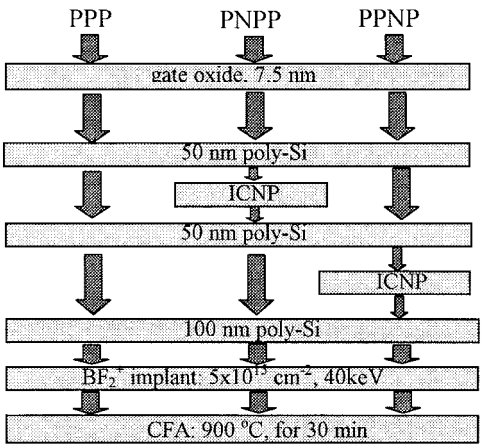

Fig. 1. Sample preparation procedure.

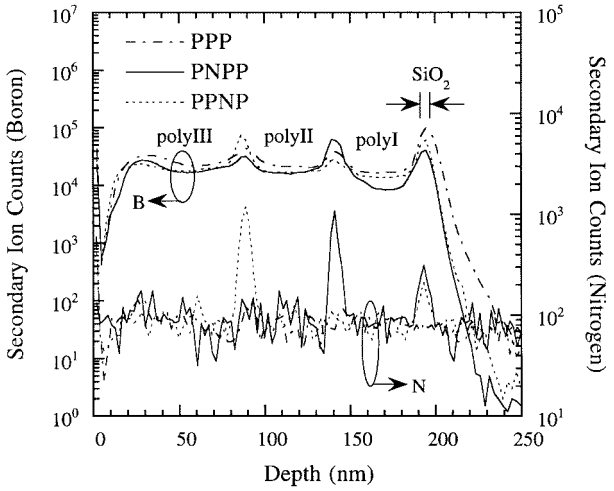

Fig. 2. The SIMS boron and nitrogen profiles for the PPP, PNPP, and PPNP samples annealed at 900 °C for 30 min, respectively.

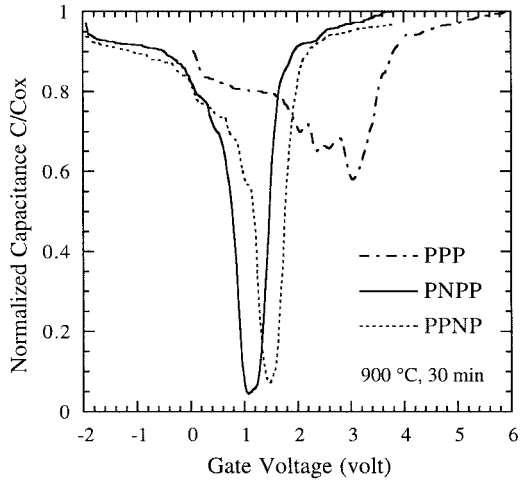

Fig. 3. Normalized quasistatic C–V curves for the PPP, PNPP, and PPNP samples annealed at 900 °C for 30 min, respectively.

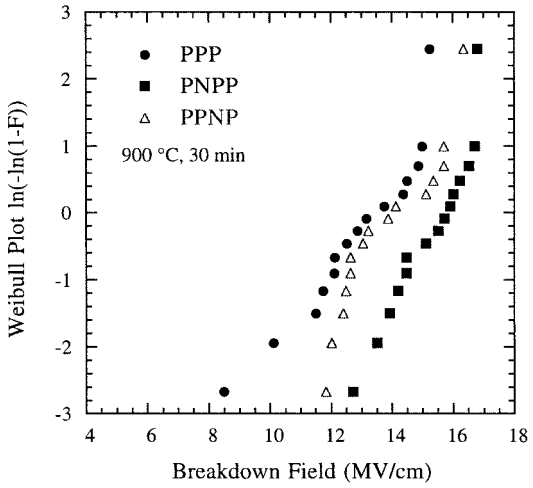

Fig. 4. The Weibull plot of breakdown field for the PPP, PNPP, and PPNP samples annealed at 900 °C for 30 min, respectively.

samples were observed not only between the second and the third layers but also in the gate oxide, indicating that the ICNP treatments would incorporate nitrogen atoms into the plasma-treated stacked layers and the gate oxide after post implant anneal. These nitrogen-rich layers can effectively block the boron diffusion and thus reduce the amount of boron impurities in the Si substrate. Furthermore, nitrogen peaks were also found for the PNPP samples between the first and the second layers as well as in the gate oxide. The nitrogen peak of PNPP samples in the gate oxide region was higher than that of PPNP ones, leading to much more effective retardation of boron penetration through gate oxides. It is attributed to the fact that the position of ICNP treatments for the PNPP sample was much closer to the gate oxide region as compared to that for the PPNP one.

Fig. 3 shows the normalized quasistatic C–V curves for all the samples annealed at 900 °C for 30 min. The Cox value is defined to be maximum high-frequency capacitance at the accumulation region. The C–V curve of PPP samples is much distorted and shifted to the right as compared to the PNPP and PPNP ones, indicating a large amount of boron penetration has occurred and thus deteriorated he gate oxide quality [4]. Moreover, although the oxide gettering effect has been reported to retard the boron penetration [16], large flat-band voltage $(V_{\rm fb})$ of 3.5 V and distorted C–V curve was measured for the PPP sample. It indicates that such a thin residual oxygen layer between stacked poly-Si films after HF dip leads to extremely minor effect on suppressing boron penetration. On the other hand, the dramatically distorted C–V curve of PPP sample is not observed in the PNPP and PPNP specimens, reflecting the suppressed boron penetration. The shift of a C–V curve for the PNPP sample was less than that for the PPNP one, attributable to further suppression of boron diffusion. In addition, the resultant flat-band voltages of PPP, PPNP, and PNPP samples were measured to be 3.5, 1.85, and 1.5 V, respectively. The $V_{\rm fb}$ value of 3.5 V for the PPP sample was reduced to be 1.5 V for the PNPP sample, indicating the significant effect of ICNP treatments on the suppression of boron penetration. Moreover, the $V_{\rm fb}$ value of 1.5 V for the PNPP sample can be further improved to be smaller by increasing poly-Si gate thickness or reducing dopant implantation energy.

Fig. 4 shows the Weibull plot of TZDB results for all the samples annealed at 900 °C for 30 min. The PPNP samples

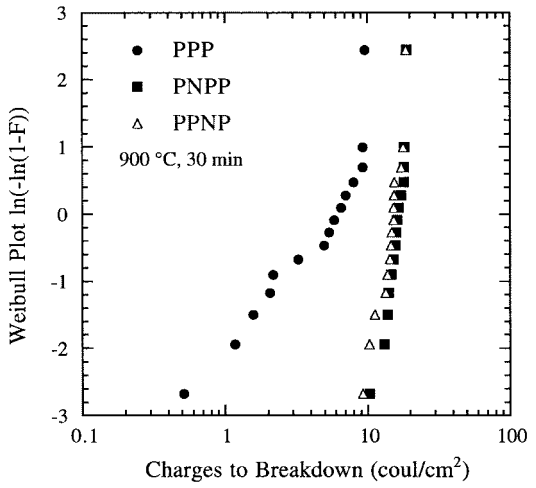

Fig. 5. The Weibull plot of charge to breakdown for the PPP, PNPP, and PPNP samples annealed at 900 °C for 30 min, respectively. The stress current density of 100 mA/cm^2 is used, with the stress area of 1.767×10^{-4} cm^2.

exhibit higher breakdown field $(E_{\rm bd})$ distribution than the PPP specimens, indicating that these two nitrogen-rich layers of PPNP samples can effectively suppress the boron diffusion and improve the gate oxide quality. In addition, the $E_{\rm bd}$ characteristics of PNPP samples can be further improved as compared to that of the PPNP ones, due to much more nitrogen incorporation by ICNP treatments closer to the gate oxide region. Furthermore, Fig. 5 indicates the Weibull plot of charge to breakdown $(Q_{\rm bd})$ for all the samples annealed at 900 °C for 30 min. The stress current density of 100 mA/cm^2 was used, with the stress area of 1.767×10^{-4} cm^2. Slight variation of $Q_{\rm bd}$ distribution was found between both the PPNP and PNPP specimens. However, the PNPP and PPNP samples possess much larger $Q_{\rm bd}$ values and sharper distribution than the PPP ones, indicating the remarkable improvement of gate oxide reliability by ICNP treatments between the stacked poly-Si layers.

IV. Conclusions

In conclusion, nitridation by ICNP treatments between the stacked poly-Si layers can create the nitrogen-rich layers, not only between the stacked poly-Si layers, but also in the gate oxide after post implant anneal, thus significantly suppressing the boron diffusion and further improving the integrity of gate oxides. In addition, the nitrogen peak of samples in the gate oxide region by ICNP treatments between the first and the second poly-Si layers was much higher than that by ICNP treatments between the second and the third layers, leading to much better integrity of gate oxides.

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