Electrical Characteristics of Textured Polysilicon Oxide Prepared by a Low-Temperature Wafer Loading and N_2 Preannealing Process

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Abstract—**A low-temperature wafer loading and N_2 preannealing process is used to grow a thin textured polysilicon oxide. The polyoxide grown on the heavily doped polysilicon film exhibits less oxide tunneling leakage current and higher dielectric strength when the top electrode is positively biased.**

I. Introduction

TEXTURED polysilicon oxides (polyoxides) have been widely used in nonvolatile memories [1]. Due to the nonuniformity of oxide thickness and the asperity at the polyoxide–polysilicon interface, the electrical properties and the dielectric strength of polyoxides are inferior to those of oxides grown on the single-crystal silicon [2].

It is well known that polyoxides exhibit a higher conductance and a lower dielectric breakdown field when the top electrode is applied by a positive bias [2]. This is due to the higher local field induced by the interface roughness at the lower polyoxide–polysilicon interface caused by the enhanced oxidation at the grain boundaries [2]. Recently, it has been reported that the electrical characteristics of polyoxides grown on a textured polysilicon layer are independent of the applied voltage polarity [3].

This letter reports a thin textured polyoxide, prepared by using a low-temperature wafer loading and N_2 preannealing process, which exhibits a lower leakage current and a higher breakdown field when the top electrode is positively bias.

II. Experimental Procedures

Thin textured polyoxide capacitors were fabricated on a 3000-Å polysilicon film (poly 1) deposited on a substrate that was thermally oxidized an oxide of 1000 Å. The poly 1 was deposited in an LPCVD system at 625°C and then doped by $POCl_3$ at 925 or 950°C. A 1000°C, $N_2 + O_2$, 30-min drive-in process was performed to activate the dopant and simultaneously to texturize the poly 1 due to the enhanced oxidation at grain boundaries [3]. After the texturization process, the sheet resistance of the textured polysilicon layer was measured to be about 55 $\Omega/\square$ for the 925°C predeposition sample (referred to as median-doped polysilicon) and 22 $\Omega/\square$ for the 950°C predeposition sample (referred to as heavily doped polysilicon). The polyoxide was prepared by loading the wafers into furnace at a low temperature (e.g., 600°C) to reduce the thermal stress and to minimize the native oxide growth [4]. Then, the temperature was gradually raised to 1000°C in an N_2 ambient. After an N_2 preannealing stage for about 30 min, thin polyoxides with thicknesses ranging from 90 to 250 Å were grown by turning on O_2 while turning off N_2. After the polyoxide formation, a second layer of polysilicon (poly 2) of a thickness of 4000 Å was deposited and doped by $POCl_3$ to the sheet resistance of 20 $\Omega/\square$.

III. Results and Discussions

Fig. 1 shows the J–E characteristics of the polyoxides of about 130 Å grown on the median-doped (M) and heavily doped (H) polysilicon films, respectively. It is seen that the median-doped polyoxide conducts a higher Fowler–Nordheim (F–N) current and has a lower dielectric breakdown field (E_{bd}) when poly 2 is positively biased, i.e., electrons are injected from the lower polyoxide–polysilicon interface. This is consistent with previous reports [2]. However, for the heavily doped polyoxide, the polarity asymmetry is opposite, i.e., the heavily doped polyoxide has less tunneling current and a higher E_{bd} value when poly 2 is positively biased. Besides, the heavily doped polyoxide has a higher E_{bd} value in both the positive bias and the negative bias as compared to the median-doped polyoxide. The trapping behaviors of these polyoxides stressed by a constant current of 100 $\mu A/cm^2$ are shown

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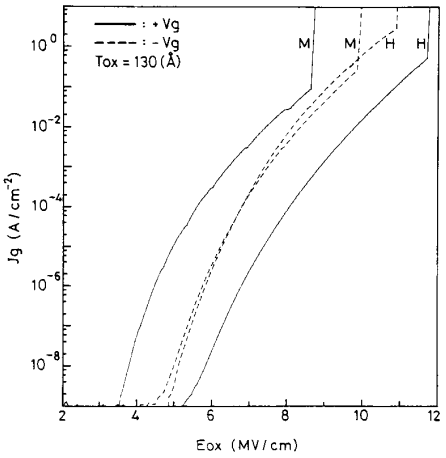

Fig. 1. The J–E characteristics of polyoxides of about 130 Å grown on the median-doped (M) and heavily doped (H) polysilicon, respectively.

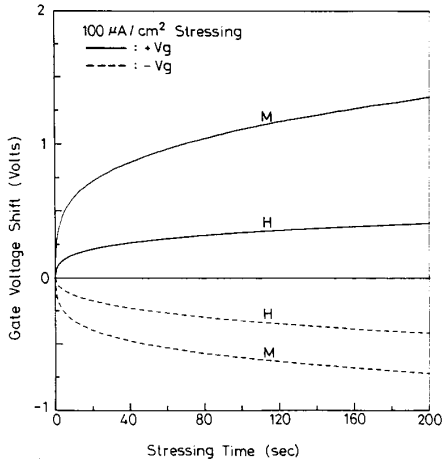

Fig. 2. The gate voltage shift versus stressing time of polyoxides under a constant current of ± 100-μA/cm^2 stressing. The area of polyoxide capacitor is 1.256×10^{-3} cm^2.

in Fig. 2. The gate voltage shifts in both polarities of the median doped polyoxide are much larger than those of the heavily doped polyoxide. Also, for the heavily doped polyoxide, the voltage shifts for both polarities are almost the same. The results in Figs. 1 and 2 indicate that the heavily doped polyoxide has a better quality as well as a smoother polysilicon–polyoxide interface as compared to the median-doped polyoxide. Fig. 3(a) and (b) shows the cross-sectional transmission electron microscopy micrographs of the median-doped and heavily doped polyoxides, respectively. It is seen that the polysilicon–polyoxide interfaces of the heavily doped polyoxide are much smoother than those of the median-doped polyoxide. This is because during the low-temperature wafer loading and N_2 preannealing process [4], the grain sizes of the heavily doped polysilicon were significantly increased and the number of grain boundaries were reduced as compared to the case of the median-doped polysilicon, as seen from the figure. This results in a smoother polyoxide–polysilicon interface.

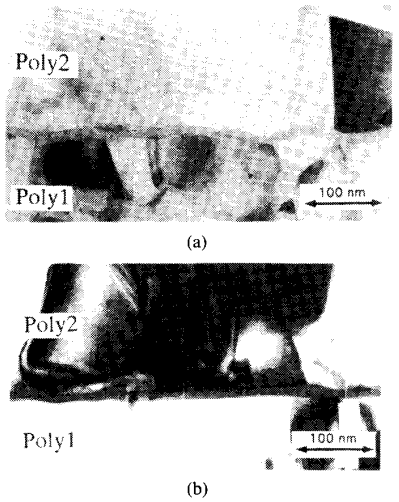

Fig. 3. The TEM micrograph of polyoxide–polysilicon interface of (a) the median-doped polyoxide and (b) the heavily doped polyoxide.

IV. Conclusion

The low-temperature wafer loading and N_2 preannealing process can produce a smoother surface of the heavily doped polysilicon such that the lower polysilicon–polyoxide interface is smoother than that of the upper one. As a result, the heavily doped polyoxide has less tunneling current and a higher E_{bd} value when poly 2 is positively biased. This asymmetrical J–E characteristic may have special advantages for the application of EEPROM [1].

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