A Comprehensive Study of Hot Carrier Stress-Induced Drain Leakage Current Degradation in Thin-Oxide n-MOSFET's

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***Abstract*— The mechanisms and characteristics of hot carrier stress-induced drain leakage current degradation in thin-oxide n-MOSFET's are investigated. Both interface trap and oxide charge effects are analyzed. Various drain leakage current components at zero V_{gs} such as drain-to-source subthreshold leakage, band-to-band tunneling current, and interface trap-induced leakage are taken into account. The trap-assisted drain leakage mechanisms include charge sequential tunneling current, thermionic-field emission current, and Shockley–Read–Hall generation current. The dependence of drain leakage current on supply voltage, temperature, and oxide thickness is characterized. Our result shows that the trap-assisted leakage may become a dominant drain leakage mechanism as supply voltage is reduced. In addition, a strong oxide thickness dependence of drain leakage degradation is observed. In ultra-thin gate oxide (30 Å) n-MOSFET's, drain leakage current degradation is attributed mostly to interface trap creation, while in thicker oxide (53 Å) devices, the drain leakage current exhibits two-stage degradation, a power law degradation rate in the initial stage due to interface trap generation, followed by an accelerated degradation rate in the second stage caused by oxide charge creation.**

***Index Terms*— Drain leakage degradation, hot carrier, thin oxide.**

I. Introduction

THE REDUCTION of drain leakage current at zero V_{gs} has been a major concern in CMOS device scaling. Gate-induced drain leakage (GIDL) current resulting from band-to-band tunneling has been recognized as one of the major drain leakage mechanisms in thin-oxide n-MOSFET's [1]. The tunneling leakage current becomes more serious when negative word-line voltage is used in DRAM's [2], [3]. Recently, hot carrier (HC) stress-induced device degradation has received much interest [4]–[8]. However, most of the studies were concentrated on device driving current and transconductance deterioration. The stress-induced drain leakage current degradation has not received as much attention. The HC effects on drain leakage current are twofold [9], [10]; One is interface trap (N_{it}) generation, and the other is fixed oxide charge (Q_{ox}) creation; N_{it} generation can introduce additional drain leakage mechanisms including Shockley–Read–Hall (SRH) thermal generation current, thermionic-field emission current, and sequential tunneling current [9]. At reduced supply voltages, while band-to-band tunneling can be greatly alleviated, the N_{it}-assisted leakage may become the dominant drain leakage mechanism in thin-oxide devices. The Q_{ox} effect on drain leakage degradation is through the modification of the Si surface field. The build up of negative oxide charge in an n-MOSFET can shift the device flatband voltage and increase the Si surface field. As a result, band-to-band tunneling current and the N_{it}-assisted tunneling current are enhanced.

In addition, experimental results showed that the N_{it}-assisted leakage exhibits a temperature dependence [3], [11]. The thermal effect becomes increasingly important at a lower operating voltage when tunneling is relatively weak. In a certain bias range, the leakage current becomes much aggravated at an elevated temperature and may have an impact on DRAM refresh time. Furthermore, research showed that Q_{ox} growth characteristic varies with gate oxide thickness [5]. In ultra-thin oxides, Q_{ox} generation is almost negligible since trapped charge can easily escape via direct tunneling [7]. In this work, we intend to investigate various HC stress-induced drain leakage degradation mechanisms and to compare the degradation characteristics at different oxide thicknesses.

In measurement, the test devices are 0.35-μm n-MOSFET's with source/drain extension. The gate oxide thicknesses t_{ox} are 53, 40, and 30 Å, and the gate width W is 100 μm. The choice of gate length is arbitrary since the HC stress-induced leakage current flows from the drain to the substrate and is almost independent of gate length. A maximum substrate current stress at $V_{gs} = 2$ and $V_{ds} = 4.5$ V is applied in this work. Interface trap creation is monitored by using a charge pumping (CP) technique. Two-dimensional device simulation [12] is performed to obtain the electric field and carrier concentration distributions in the measured devices.

II. Drain Leakage Current Mechanisms

The various drain leakage paths in an HC stressed n-MOSFET are illustrated in Fig. 1. The prestress drain leakage currents include band-to-band tunneling current I_{BB}, drain-to-

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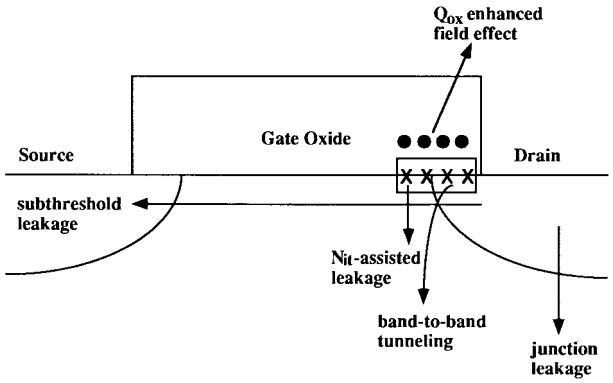

Fig. 1. Illustration of various drain leakage current paths in an HC stressed n-MOSFET's. Full circles in the gate oxide represent negative oxide trapped charge and the crosses at the Si/SiO_2 surface are interface traps.

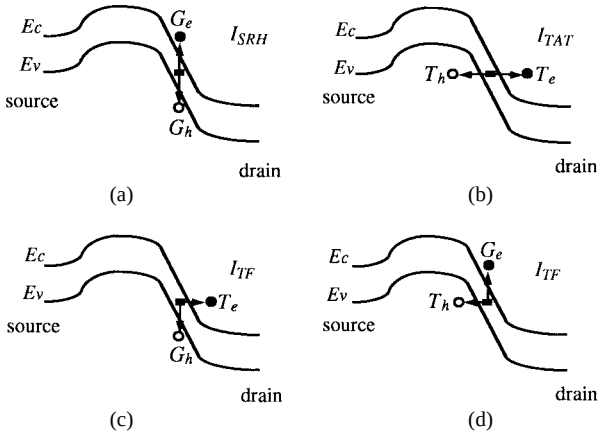

Fig. 2. Illustration of various interface trap-assisted carrier transition processes in the lateral direction. G_e and G_h are electron and hole thermionic emission rates, and T_e and T_h are electron and hole tunneling rates. I_{SRH} is the Shockley–Read–Hall current, I_{TAT} is charge sequential tunneling current, and I_{TF} is thermionic-field emission current.

source subthreshold current I_S, and junction leakage current

$$I_{BB} = AF_s^2 \exp(-B/F_s) \tag{1}$$

$$I_S = I_0 \exp\left(\frac{q}{nkT} V_{gs}\right) \tag{2}$$

where the parameters A and B are defined in [13]. F_s denotes the Si surface field and other variables have their usual definitions. Drain junction leakage current is small here and can be ignored.

A. N_{it}-Assisted Drain Leakage Mechanisms

The N_{it}-assisted drain leakage mechanisms are illustrated in Fig. 2, where the carrier transition processes in the lateral direction are shown. G_e and G_h in the figure denote electron and hole thermionic emission rates, and T_e and T_h represent electron and hole tunneling rates, respectively. A complete N_{it}-assisted leakage path is formed at the Si/SiO_2 surface by hole emission from interface traps to the valence band and electron emission from the traps to the conduction band. Both electron and hole transitions can be carried out via either thermionic emission or tunneling. The carrier transition processes in Fig. 2(a) represent the SRH current (I_{SRH}), where

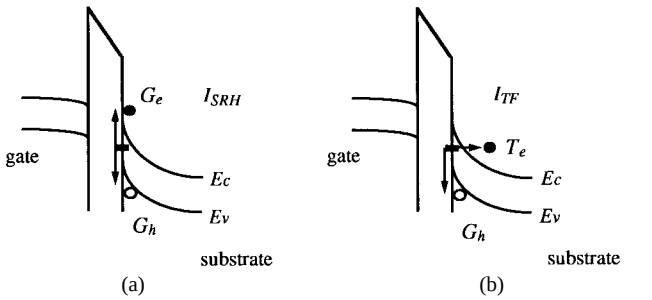

Fig. 3. Interface trap-assisted carrier transition processes in the vertical direction.

both electron and hole transitions are through thermionic emission. Fig. 2(b) is sequential tunneling current (I_{TAT}). Fig. 2(c) and (d) are thermionic-field emission current (I_{TF}), i.e., one carrier transition through thermionic emission and the other through tunneling. Carrier transition processes in the vertical direction are shown in Fig. 3. Note that hole transition is through thermionic emission only in Fig. 3. Hole tunneling from the trap states to the valence band is not permissible in the vertical direction because of energy conservation in charge tunneling. Therefore, T_h is a function of only the lateral field, while the tunneling processes I_{BB} and T_e are dependent on the total field. The calculation of the charge thermionic and tunneling rates can be found in our previous publication [9]. The closed-form expressions for the N_{it}-assisted leakage currents are written below

$$I_{TAT} = qW \int_{\Delta L} \int_{E_g} N_{it}(x, E) \frac{T_e T_h}{G_e + T_e} \, dE \, dx \tag{3}$$

$$I_{TF} = qW \int_{\Delta L} \int_{E_g} N_{it}(x, E) \frac{T_e G_h + T_h G_e}{G_e + T_e} \, dE \, dx \tag{4}$$

$$I_{SRH} = qW \int_{\Delta L} \int_{E_g} N_{it}(x, E) \frac{G_e G_h}{G_e + T_e} \, dE \, dx \tag{5}$$

where ΔL is the length of the HC stress region and E_g denotes the Si bandgap. The total N_{it}-assisted leakage current ΔI_d is the sum of these three components

$$\Delta I_d = I_{TAT} + I_{TF} + I_{SRH} = qW \int_{\Delta L} \int_{E_g} \cdot N_{it}(x, E)(G_e + T_e) \, dE \, dx. \tag{6}$$

In addition, it can be shown that I_{TAT} in (3) can be further reduced to an analytical expression [9]

$$I_{TAT} \propto N_{it} \exp(-B_{it}/F_s) \tag{7}$$

where the parameter B_{it} is determined by the ratio of the surface fields in the vertical and the lateral directions. In modeling, the field-dependent parameters are electron and hole tunneling times and the temperature-dependent parameters are the bandgap, thermal velocity, and intrinsic carrier concentration [14].

B. Q_{ox}-Enhanced Drain Leakage Degradation

A change of the Si surface field ΔF_s resulting from oxide charge generation is Q_{ox}/ε_{si}, where Q_{ox} is defined as the equivalent areal density at the Si/SiO_2 surface. Assuming ΔF_s

is small, the variation of I_{BB} can be approximated by

$$\begin{aligned} I_{BB}(Q_{ox}) &= A(F_s+\Delta F_s)^2 \exp(-B/(F_s+\Delta F_s)) \\ &\approx AF_s^2 \exp(-B/F_s)\exp(B\Delta F_s/F_s^2) \\ &= I_{BB}(Q_{ox}=0)\exp(BQ_{ox}/\varepsilon_{si}F_s^2). \end{aligned} \tag{8}$$

Similarly, the Q_{ox}-induced I_{TAT} degradation is shown as follows:

$$\begin{aligned} I_{TAT}(N_{it}, Q_{ox}) = I_{TAT}(N_{it}, Q_{ox}=0) \\ \cdot \exp\left(B_{it}Q_{ox}/\varepsilon_{si}F_s^2\right). \end{aligned} \tag{9}$$

Two points should be mentioned: first, I_{TAT} is linearly dependent on N_{it} (7) but has an exponential dependence on Q_{ox}. A small amount of Q_{ox} can result in significant drain leakage current degradation. Second, since I_{BB} is affected only by Q_{ox} (8), while I_{TAT} is influenced by both N_{it} and Q_{ox} (9), we can characterize the N_{it} and Q_{ox}-induced degradations separately by measuring I_{BB} and I_{TAT}.

C. Drain Leakage Degradation Rates

It was reported that the growth rates of N_{it} and Q_{ox} follow a power law dependence on stress time [15], i.e.,

$$N_{it}(t) = A_1 t^{n_1} \quad \text{and} \quad Q_{ox}(t) = A_2 t^{n_2}. \tag{10}$$

Substituting (10) into (8) and (9), the degradation rates of I_{BB} and I_{TAT} are obtained. In case that N_{it} generation is dominant,

$$I_{BB}(t) \sim \text{constant} \tag{11}$$

$$I_{TAT}(t) \propto N_{it} \propto t^{n_1}. \tag{12}$$

On the other side, if Q_{ox} generation is dominant

$$I_{BB}(t) \propto \exp\left(BQ_{ox}/\varepsilon_{si}F_s^2\right) = \exp\left(BA_2t^{n_2}/\varepsilon_{si}F_s^2\right) \tag{13}$$

$$I_{TAT}(t) \propto \exp\left(B_{it}Q_{ox}/\varepsilon_{si}F_s^2\right) = \exp(B_{it}A_2t^{n_2}/\varepsilon_{si}F_s^2). \tag{14}$$

III. Results and Discussion

The measured prestress and poststress I_d–V_{gs} characteristics in a 40-Å oxide n-MOSFET at $T = 292$ K are shown in Fig. 4. The stress condition is $V_{ds} = 4.5$ V and $V_{gs} = 2.0$ V for 3000 s. N_{it} generation is evidenced by the change of the subthreshold swing. Q_{ox} creation is minimal in the stressed device because the prestress and poststress GIDL currents converge to each other at a large V_{dg}. The drain-induced barrier lowering effect [16] is insignificant in this device.

The dependence of prestress and poststress $V_{gs} = 0$ V drain leakage currents on supply voltage (V_{dd}) at two temperatures, $T = 292$ K and $T = 353$ K, are shown in Fig. 5. The interface trap annealing at $T = 353$ K is insignificant. The stress and temperature-enhanced drain leakage current factor, defined as the ratio of the poststress drain leakage to the prestress $T = 292$ K drain leakage, is shown in Fig. 6. The N_{it}-induced drain leakage current enhancement is particularly pronounced around a supply voltage of 2.1 V. An enhancement factor of 18 at $T = 292$ K is obtained. As temperature rises ($T = 353$ K),

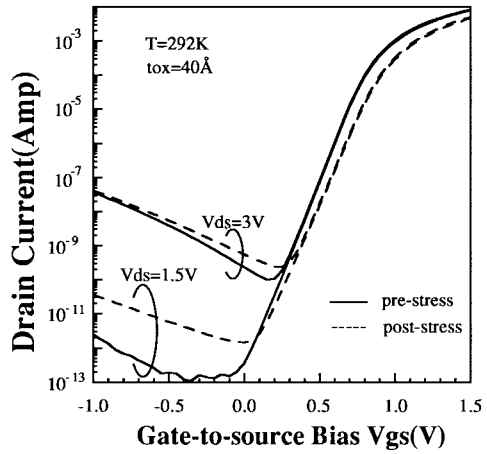

Fig. 4. Prestress and poststress I_d–V_{gs} characteristics in a 40-Å gate oxide n-MOSFET at $T = 292$ K. The stress condition is $V_{ds} = 4.5$ and $V_{gs} = 2.0$ V for 3000 s.

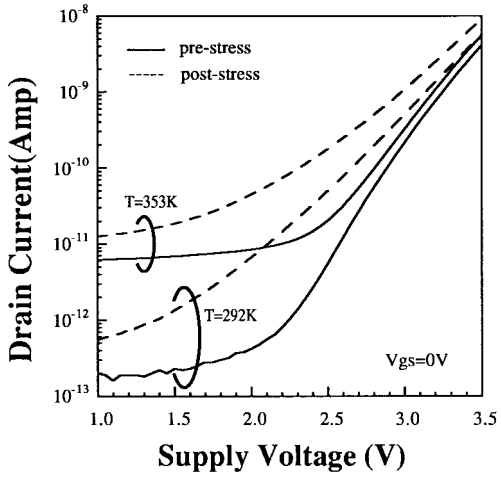

Fig. 5. Measured prestress and poststress drain leakage currents at $V_{gs} = 0$ V versus supply voltage ($t_{ox} = 40$ Å).

the enhancement factor is further increased up to 110. The temperature effect becomes more significant at a lower V_{dd}. For example, the enhancement factor at $V_{dd} = 1.3$ V is 5 at $T = 292$ K and 80 at $T = 353$ K. The poststress drain leakage currents are decomposed in Fig. 7 ($T = 292$ K) and Fig. 8 ($T = 353$ K). The solid lines are from measurement and the circles represent calculated result. In measurement, I_S is monitored at the source, ΔI_d is obtained from the difference between the prestress and poststress drain leakage currents, and I_{BB} is assumed to be equal to its prestress result because of negligible Q_{ox} generation in the 40-Å oxide device. In calculation, N_{it} is 1.4×10^{12} cm^{-2}, and the length of the N_{it} distribution ΔL is assumed to be 400 Å.

In Fig. 7, band-to-band tunneling current I_{BB} manifests itself as a dominant mechanism at a large supply voltage ($V_{dd} \geq 3.1$ V). The drain leakage current degradation arising from N_{it} creation is relatively unimportant in this V_{dd} range. By comparing Figs. 7 and 8, the I_{BB} at $T = 353$ K (1.9 nA at $V_{dd} = 3.3$ V) is slightly above that at $T = 292$ K (1.4 nA at $V_{dd} = 3.3$ V). The reason is that the bandgap reduces at a higher temperature, and thus the tunneling current

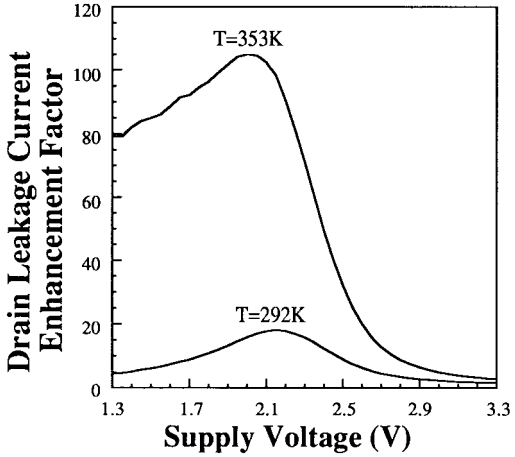

Fig. 6. The ratio of the poststress drain leakage current to the prestress drain leakage current at $T = 292$ K versus supply voltage.

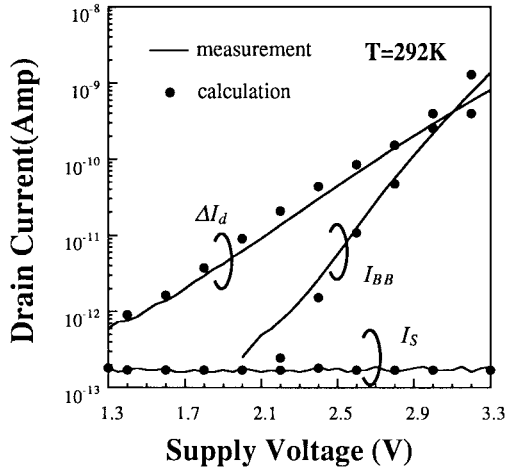

Fig. 7. Various zero V_{gs} drain leakage current components from measurement (solid lines) and calculation (full circles) ($T = 292$ K).

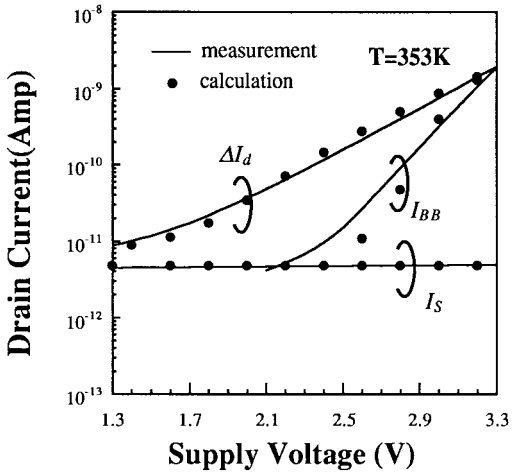

Fig. 8. Various zero V_{gs} drain leakage current components from measurement (solid lines) and calculation (full circles) ($T = 353$ K).

increases. In Figs. 7 and 8, the N_{it}-assisted leakage current ΔI_d shows a weaker field dependence than I_{BB} due to a smaller tunneling barrier from the traps to conduction band (electron tunneling) or to the valence band (hole tunneling).

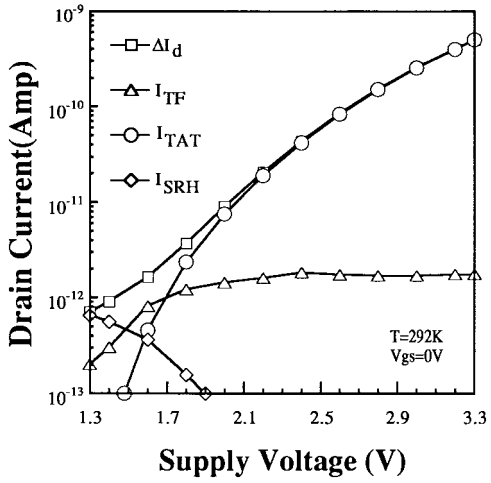

Fig. 9. Calculation of various interface trap-assisted drain leakage currents at $T = 292$ K.

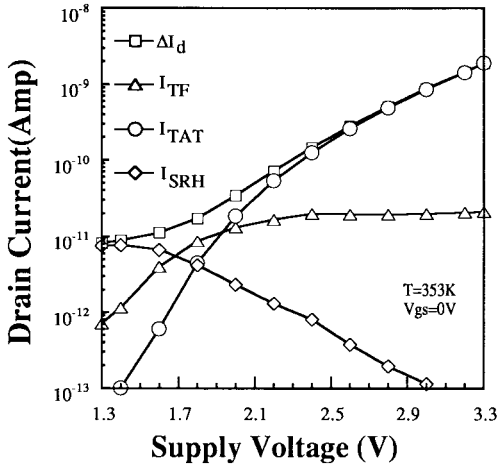

Fig. 10. Calculation of various interface trap assisted drain leakage currents at $T = 353$ K.

In other words, the B_{it} in (7) is smaller than the parameter B in (1). Consequently, as supply voltage scales down, I_{BB} drops more quickly and ΔI_d becomes dominant for $V_{dd} \leq 3.1$ V. When V_{dd} is further reduced ($V_{dd} \leq 1.5$ V), the tunneling effect is unimportant and the drain leakage current enhancement results mainly from the SRH generation current. Thus, the N_{it} effect is most significant at a medium V_{dd} and the enhancement factor in Fig. 6 peaks around 2.1 V.

Furthermore, we analyze the components of the N_{it}-assisted leakage current ΔI_d in Fig. 9 ($T = 292$ K) and Fig. 10 ($T = 353$ K). In Fig. 9, ΔI_d is dictated by I_{TAT} for $V_{dd} > 1.7$ V, by I_{TF} for $1.7\ \text{V} \geq V_{dd} \geq 1.5$ V, and by I_{SRH} for $V_{dd} \leq 1.5$ V. In Fig. 10, the thermally related components I_{TF} and I_{SRH} are more prominent. For example, the I_{SRH}-dominant region extends from $V_{dd} \leq 1.5$ V at $T = 292$ K to $V_{dd} \leq 1.7$ V at $T = 353$ K.

The oxide thickness dependence of drain leakage current degradation is investigated in Fig. 11. The drain leakage current degradation rates in two different oxide thickness (30 and 53 Å) devices are compared. Note that the oxide thickness 30 Å is already in the direct tunneling regime. The measurement bias is $V_{ds} = 2.5$ V and $V_{gs} = 0$ V, and the

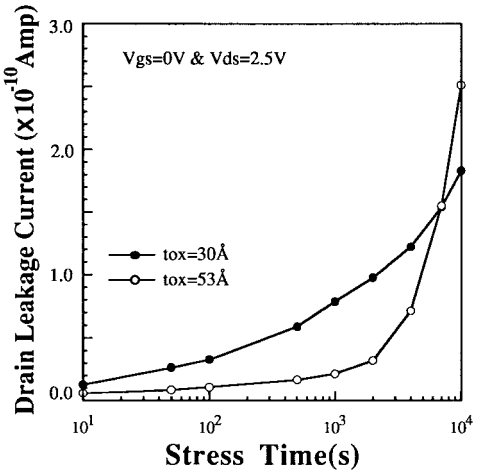

Fig. 11. Comparison of the drain leakage current degradation in the 30-Å oxide and 53-Å oxide n-MOSFET's measured at $V_{gs} = 0$ and $V_{ds} = 2.5$ V. The stress bias is $V_{gs} = 2.0$ and $V_{ds} = 4.5$ V.

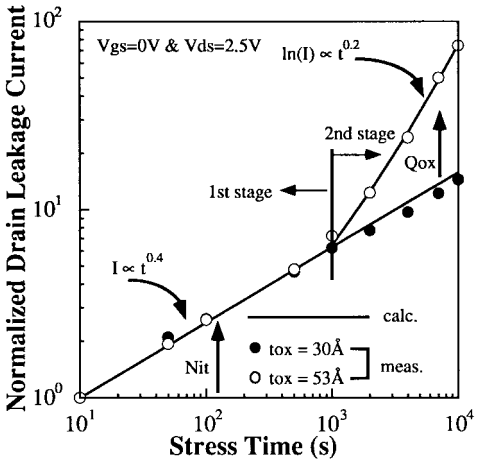

Fig. 12. Normalized drain leakage currents versus stress time in the 30-Å oxide and 53-Å oxide n-MOSFET's measured at $V_{gs} = 0$ and $V_{ds} = 2.5$ V. The solid lines represent fitting results and the circles are measured data points.

dominant drain leakage current is I_{TAT} from Fig. 9. Although the drain leakage current in the 53-Å oxide device is smaller initially, it shows a faster degradation rate when stress time is sufficiently long. A crossover of these two drain leakage currents is observed. To explore the reason for the drastic drain leakage degradation in the 53-Å oxide device, we replot the two leakage currents on a log–log scale in Fig. 12. For the purpose of comparison, the two currents are normalized to have the same starting value. The corresponding CP currents in the two devices are shown in Fig. 13. In Fig. 12, the I_{TAT} in the 30-Å oxide device follows a power law degradation rate in the entire stress period. The power factor is about 0.4, which correlates with the stress time dependence of the CP current reasonably well and reflects the growth rate of N_{it}. In contrast, the I_{TAT} degradation in the 53-Å oxide device exhibits a distinctly different feature. A two-stage degradation process is noticed [10]. In the first stage ($t \leq 10^3$ s), N_{it} is dominant and the degradation follows a power law dependence. In the second stage, Q_{ox} becomes dominant and I_{TAT} shows an accelerated degradation rate. The calculated results from (12) and (14)

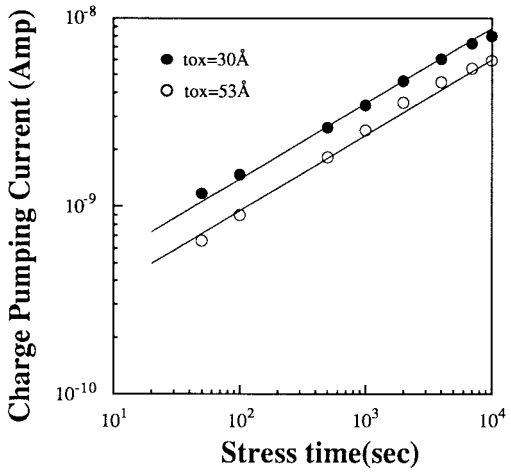

Fig. 13. Charge pumping current versus stress time in the 30-Å oxide and 53-Å oxide n-MOSFET's. The CP measurement frequency is 100 kHz.

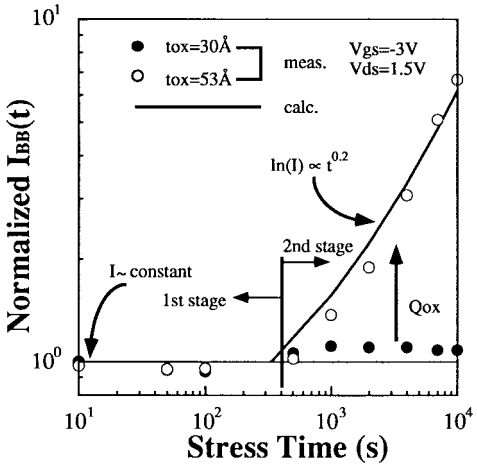

Fig. 14. Normalized band-to-band tunneling currents in the 30-Å oxide and 53-Å oxide n-MOSFET's measured at $V_{gs} = -3$ and $V_{ds} = 1.5$ V.

are shown by the solid lines in Fig. 12. The extracted Q_{ox} power factor n_2 is about 0.2, and the estimated Q_{ox} density at $t = 10^4$ s is about 1.6×10^{12} q/cm^2. Note that the I_{TAT} degradation rate is even faster than the Q_{ox} growth rate in the second stage since Q_{ox} has an exponential effect on I_{TAT}. The exponential degradation of the drain leakage current due to Q_{ox} creation may potentially impose a severe limit on device lifetime.

Since I_{BB} is only affected by Q_{ox}, measurement of the drain leakage current at $V_{ds} = 1.5$ V and $V_{gs} = -3$ V, where I_{BB} is dominant, can be used to monitor oxide charge creation. The normalized I_{BB}'s in the two devices are shown in Fig. 14. The I_{BB}'s are nearly constant for $t \geq 10^3$ s, which implies minimal Q_{ox} creation. A slight decline in the I_{BB}'s in this period can be explained by a small amount of net positive oxide charge (or interface charge) creation. For $t \geq 10^3$ s, the I_{BB} in the 30-Å oxide device remains still constant. This result is consistent with the statement by Momose *et al.* [7] that Q_{ox} creation is unlikely in ultra-thin oxides in the direct tunneling regime. The I_{BB} in the 53-Å oxide device, however, increases significantly in the second stage. The increase of the I_{BB} can be well fitted by using (13) (solid line) with $n_2 = 0.2$.

IV. Conclusion

Various drain leakage current degradation mechanisms have been modeled and characterized. At scaled supply voltages, the N_{it}-assisted leakage current becomes a dominant drain leakage mechanism in the current devices. An oxide thickness dependence of drain leakage degradation has been observed. In ultra-thin oxide (30 Å) devices, the HC stress-induced drain leakage degradation is mostly attributed to interface trap generation, while in thicker oxide (53 Å) devices, the degradation is driven by both interface trap and oxide charge creation. By using a thinner gate oxide, oxide charge generation is negligible and the stress-induced drain leakage degradation can be much improved.

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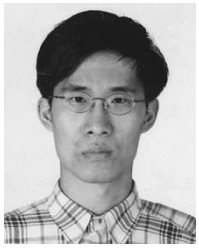

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