AIP Applied Physics Letters

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Citation: Applied Physics Letters **75**, 1092 (1999); doi: 10.1063/1.124607
View online: http://dx.doi.org/10.1063/1.124607
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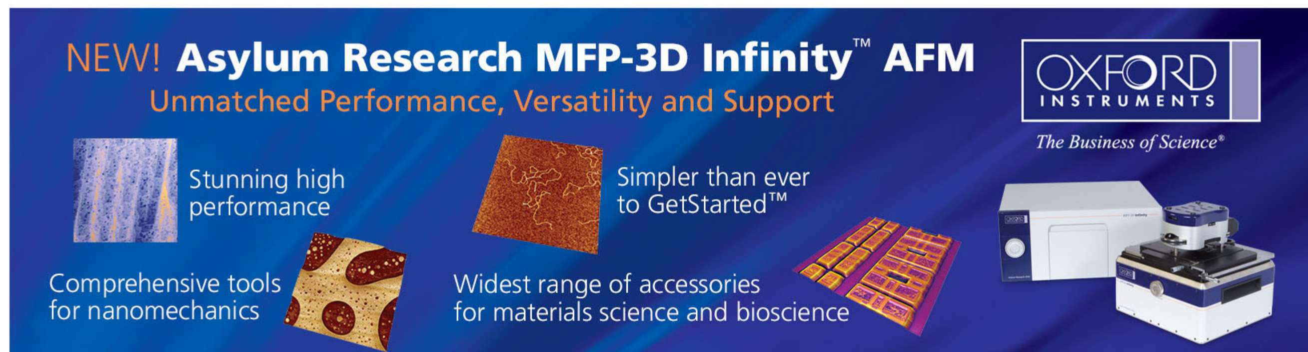

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Observation of abnormal capacitance-frequency behavior in $In_{0.12}Ga_{0.88}As$/GaAs *p-i-n* superlattice grown at low temperature

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(Received 9 March 1999; accepted for publication 29 June 1999)

Capacitance-frequency measurement is used to study $In_{0.12}Ga_{0.88}As$/GaAs p-i-n superlattice, with superlattice layer grown at 300 °C by molecular-beam epitaxy. Three traps are observed, and their parameters are consistent with those obtained from deep-level transient spectroscopy. Among these three traps, the trap ($E_a = 0.45 \pm 0.02$ eV, $\sigma = 6 \pm 4 \times 10^{-17}$ cm^2) shows an abnormal increase of capacitance with increasing frequency, similar to that observed from the 0.66 eV trap in low-temperature grown GaAs p-i-n structure, suggesting that it is created by the low-temperature growth and is a generation-recombination center. This result also shows that the capacitance-frequency measurement is effective in studying the generation-recombination centers. © *1999 American Institute of Physics.* [S0003-6951(99)01434-5]

Annealed GaAs grown by molecular-beam epitaxy (MBE) at a low temperature (LT) has been shown to have a very high resistivity and short carrier lifetime.[1–3] Recently, the low-temperature grown technique has been extended to the InGaAs/GaAs superlattice[4–6] and a reduction of the carrier lifetime[4] has been reported and is proposed to be related to the presence of a large fraction of defects. Although defect properties of LT–GaAs are extensively studied, there are few reports on the properties of deep traps in the InGaAs/GaAs system. Therefore, in this work, we extend our studies of deep levels from LT–GaAs[3] to a LT–$In_{0.12}Ga_{0.88}As$/GaAs system and use capacitance-frequency ($C-F$) measurement and deep-level transient spectroscopy (DLTS) to characterize its defects.

Samples studied here were grown by a Varian Gen-II MBE system on n^+-(001) GaAs substrates. Figure 1 shows the detailed structure of a $p-n$ junction sandwiched with a 30 period undoped $In_{0.12}Ga_{0.88}As$ (150 Å)/GaAs (100 Å) superlattice grown at a low temperature of 300 °C. Except for the superlattice, the rest of the structures were grown at 620 °C.

The sample shows the typical rectified current–voltage characteristics with a forward-bias ideality factor close to two around room temperature. At 77 K, it shows a large turn-on voltage similar to the feature of a trap-filling effect in a LT-grown n^+-LT-n^+ GaAs structure. This sample was then investigated by a $C-F$ measurement using a HP4194 gain-phase analyzer. The detail theory about the $C-F$ spectra can be found elsewhere.[7] The small-signal oscillation level was kept at 50 mV and the sample was biased at a reversed voltage of -1 V.

Figure 2 shows the $C-F$ results for the sample, in which three drops in C representing three traps, labeled as E1, T1, and H1, were observed. Among them, the trap parameters for the T1 and H1 traps were determined from their inflexion frequency versus temperature. However, the E1 trap occurred at a frequency so low that the low-frequency plateau could not be seen without much noise. Therefore, the DLTS spectra were also taken for determining the trap parameters for E1. The inset of Fig. 2 presents the DLTS spectra at different rate windows measured by the HP4194 gain-phase analyzer. Three traps were clearly observed and their parameters are consistent with those from the $C-F$ measurement as shown in the Arrhenius plot in Fig. 3. The big difference in the measuring temperatures between the DLTS and $C-F$ methods enabled us to determine their parameters more accurately. The parameters of these three traps are determined to be $E_a = 0.73$ eV, $\sigma = 4.6 \times 10^{-11}$ cm^2 for H1, $E_a = 0.45$ eV, $\sigma = 6.0 \times 10^{-17}$ cm^2 for T1, and $E_a = 0.75$ eV, $\sigma = 3.7 \times 10^{-15}$ cm^2 for E1, respectively.

Among these traps, the origins of the H1 and E1 traps are briefly described here. The H1 trap was also observed in the reference sample which was of the same structure but with the superlattice layer grown at $T = 550$ °C. Both the $C-F$ and DLTS data of the reference sample exhibit only one trap as shown in Fig. 3 and should belong to the H1 trap when plotted as hollow and solid triangles in Fig. 4. Therefore, the H1 trap is irrelevant to the low temperature growth. This result is also collaborated by Ashizawa *et al.*[8] who observed a trap labeled as their H2 in InGaAs/GaAs p^+n diodes with a similar In composition and proposed that it was due to the lattice mismatch. From the position in the Arrhenius plot, our trap H1 is very close to their H2 trap. Therefore,

0.1μm p$^+$-GaAs (1x10^{18}cm^{-3} Be)
0.4μm p-GaAs (5x10^{17}cm^{-3} Be)
0.025μm undoped GaAs
$In_{0.12}Ga_{0.88}As$/GaAs 150Å/100Å x30 periods grown at 300°C
0.025μm undoped GaAs
0.2μm n-GaAs (5x10^{17}cm^{-3} Si)
n$^+$-GaAs substrate

FIG. 1. Structure of the $In_{0.12}Ga_{0.88}As$/GaAs superlattice with superlattice grown at a low temperature of 300 °C.

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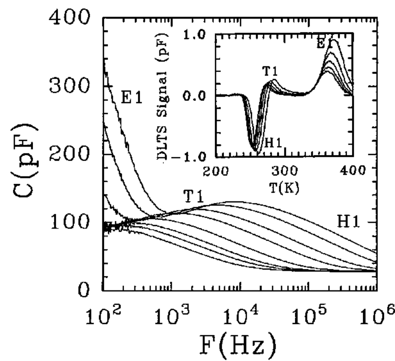

FIG. 2. $C-F$ spectra at a reverse bias of 1 V for the LT superlattice sample. The measuring temperature are 421, 407, 390, 376, 358, 346, 340, and 332 K from the top curve to the bottom one. Three traps are observed and labeled as E1, T1, and H1, for convenience. The same three traps were also observed by DLTS as shown in the inset. The rate window is 1.60, 1.97, 2.56, 3.65, and 6.40 s^{-1} for each curve with peaks shifting to the right.

we believe that the H1 trap is not created by the LT growth and is probably related to the lattice mismatch between GaAs and InGaAs. As to the E1 trap, it occurs very close to the previously reported EL2 level[9] (shown as a dotted line). A photo transient capacitance measurement was performed at 77 K and a photocapacitance quenching effect was observed,[10] further supporting that the E1 observed by us is EL2. A. C. Irvine and D. U. Palmer[11] observed EL2 in InGaAs grown on GaAs by MBE and deduced that the origin of EL2 is related to the interaction of Ga vacancies with misfit dislocations created by the lattice mismatch between InGaAs and GaAs. Because the Ga vacancies are created in LT-grown GaAs, it is reasonable to suggest that the Ga vacancies are also created in LT-grown InGaAs/GaAs superlattice. Therefore, EL2 is likely to exist in the LT-grown InGaAs/GaAs superlattice sample.

A careful examination of the $C-F$ behavior for the T1 trap shows that its capacitance increase with frequency, a feature which is different from those of the H1 and E1 traps. This abnormal feature is more pronounced when the $C-F$ data are taken at 0 V as shown in Fig. 5. From the relationship between its inflexion frequency and temperatures, parameters of this trap were determined to be $E_a = 0.46$ eV and $\sigma = 1.0\times10^{-16}\,\text{cm}^2$ which corresponded to those determined by DLTS, as shown in the Arrhenius plot in Fig. 3. This

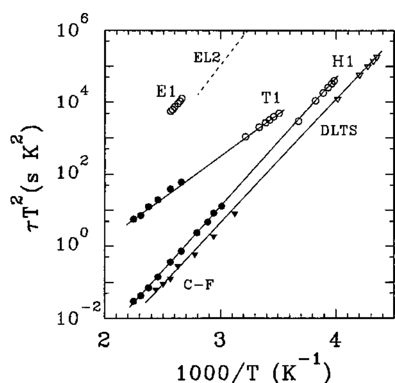

FIG. 3. Arrhenius plots for LT *p-i-n* InGaAs/GaAs sample. The solid points are obtained by DLTS, while the hollow points are obtained by $C-F$ measurement. The hollow and solid triangles are the data from the reference sample and should belong to the H1 trap. Results observed by both methods are consistent. The dash line is the EL2 reported by A. Mircea (see Ref. 9).

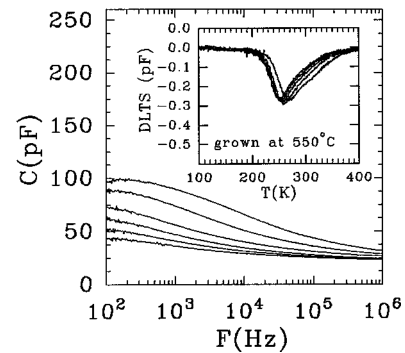

FIG. 4. $C-F$ spectra at a reverse bias of -1 V for the reference sample. The measuring temperatures are 390, 360, 340, 320, 299, and 280 K from the top curve to the bottom one. The DLTS spectra for the same sample is shown in the inset. The rate windows are 1.60, 1.97, 2.56, 3.65, and 6.40 s^{-1} for each curve with peaks shifting to the right. One trap was observed by both method.

abnormal behavior is not due to the effect of an unwanted inductance in the measuring cable, for its effect on an equivalent R–C circuit would decrease the capacitance with frequency.

Theoretically, if a trap captures or emits electrons, the trap will exhibit a transient current $\delta V(\delta C/\tau)\exp(-t/\tau)$ which reduces to zero after a time constant τ when the device is subjected to an applied step voltage δV. This transient current is the so-called charging and discharging current. This current component, after a Fourier transformation, can be decomposed into a capacitance and conductance in the frequency domain. The capacitance will decrease with frequency like a step-like curve: $C(\omega) = C_\infty + \delta C/1+(\omega\tau)^2$. The E1 and H1 traps in Fig. 2 follow this behavior. However, if a trap interacts not only with electrons but also with holes, when a reverse step voltage is applied, the device may exhibit a conducting current: $\delta V G_t[1-\exp(-t/\tau_t)]$ which exponentially increases to its steady state with an inertial time constant. When the steady state is reached, it does not mean that the trap no longer emits electrons but mean that its electron emission rate is equal to its hole emission rate. This inertial conduction, after a Fourier transformation, will cause the measured capacitance increase with frequency. Summing up the charging-discharging current and the inertia conduction current, the frequency-dependent capacitance is[12]

$$C_p(\omega) = C_\infty - (G_t\tau_t - \delta C_t) + \frac{(\omega\tau_t)^2(G_t\tau_t - \delta C_t)}{1+(\omega\tau_t)^2}.$$

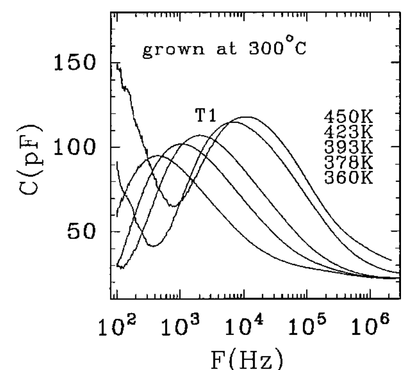

FIG. 5. The $C-F$ behavior at a bias of 0 V for the T1 trap of the LT *p-i-n* InGaAs/GaAs sample. The capacitance shows a pronounced abnormal increase with frequency.

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Because the existence of a large generation-recombination current at 0 V conductance G_t is markedly larger at 0 V than at -1 V. Therefore, the condition $G_t > \delta C_t / \tau_t$ is more satisfied at 0 V than at -1 V, rendering the abnormal behavior more pronouncedly observed at 0 V as shown in Fig. 5 than in Fig. 2.

Several groups have studied the inertial conduction current which needs time to establish[12–14] when the device is subjected to a small voltage step. For trap T1 in our sample, we feel that among all possibilities, the most likely origin of this inertial conducting current is the generation-recombination current. When a small reverse voltage step is applied, the trap occupation probability will change. Consider a situation in which the change in the trap occupation probability influences the generation-recombination current. Therefore, the generation-recombination current has a time constant which relates to the trap occupation parameters. We had observed a similar abnormal capacitance behavior for a generation-recombination center at 0.66 eV in a LT-grown GaAs p-LT-n structure,[12] which is responsible for the reverse-bias leakage current. Since the T1 trap exhibits a similar abnormal capacitance behavior, it leads us to believe that the T1 trap is created by the LT growth and is a generation-recombination center, which contributes to part of the reverse-bias leakage current. Finally, it should be noted that because the abnormal capacitance was only observed by the $C-F$ spectra and not by DLTS, the $C-F$ measurement is useful to study the generation-recombination centers.

The authors would like to thank the National Science Council of the Republic of China for providing financial support of this work under Contract No. NSC-87-2112-M-009-022.

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