A Novel Lightly Doped Drain Polysilicon Thin-Film Transistor with Oxide Sidewall Spacer Formed by One-Step Selective Liquid Phase Deposition

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Abstract— **We have proposed and successfully demonstrated a novel process for fabricating lightly doped drain (LDD) polycrystalline silicon thin-film transistors (TFT's). The oxide sidewall spacer in the new process is formed by a simple one-step selective liquid phase deposition (LPD) oxide performed at 23 °C. Devices fabricated with the new process exhibit a lower leakage current and a better ON/OFF current ratio than non-LDD control devices. Since the apparatus used for LPD oxide deposition is simple and inexpensive, the new process appears to be quite promising for future high-performance poly-Si TFT fabrication.**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistor (poly-Si TFT) is one of the most promising candidates for the switching elements in future high-performance large-area active matrix liquid-crystal display (AMLCD) systems. However, conventional poly-Si TFT's suffer from an anomalous OFF-state leakage current which increases with drain voltage and gate voltage [1]. This undesirable OFF-state leakage current thus makes poly-Si TFT's unacceptable for switching device applications, as a low OFF-state leakage current less than 1 pA per pixel is needed for a gray-scale active matrix LCD [2].

It has been well known that the dominant mechanism of the leakage current in poly TFT's is field emission via grain boundary traps due to the high electric field near the drain junction [3]. An effective method to reduce the electric field in the drain depletion region is to incorporate a lightly doped offset region between the active channel region and the heavily doped drain region. Various methods have been proposed to achieve such an offset region. However, these structures require either an additional photolithographic step for defining the nonself-aligned offset region [4], [5], or the deposition of an oxide layer and subsequent etch-back for forming the self-aligned sidewall spacer [6]. In addition, in the first approach length control of the offset region is difficult due to misalignment errors, while the second approach may cause plasma damage during the etch-back step.

In this letter, we propose a novel lightly doped drain (LDD) poly-Si TFT to reduce the leakage current. The oxide sidewall spacer in the new process is formed by a simple one-step selective liquid phase deposition (LPD). The new process thus appears to be quite attractive for future high-performance AMLCD applications.

II. Experiments

The chemical solution for LPD oxide deposition has been described elsewhere [7]. Briefly, 35 g of silica (SiO_2) powder (99.999%) was first added to 1 L of hydrofluosilicic acid (H_2SiF_6, 4 mol/l). The solution became saturated with silicic acid [$Si(OH)_4$] after being stirred at 23 °C for 17 h. The solution was then filtered to remove the undissolved silica. Deionized water (H_2O) was added to the saturated solution as it was stirred, so that the solution became supersaturated with silicic acid. The quantity of H_2O added was 25 ml per 100 ml of the immersing solution.

Key processing steps for fabricating the novel TFT device are illustrated in Fig. 1. First, a 50-nm undoped amorphous silicon layer was deposited on an oxidized silicon substrate by low-pressure chemical vapor deposition (LPCVD) at 460 °C for 15 min with Si_2H_6 as the gaseous source. The amorphous silicon layer was then crystallized at 600 °C for 24 h by furnace anneal and patterned into active device islands. A 10-nm oxide layer was grown by thermal oxidation at 950 °C, and a 30-nm nitride layer was deposited by LPCVD at 800 °C to form the composite gate insulator. It is worth noting that although we have applied high-temperature processing (i.e., 800–900 °C) to demonstrate the feasibility of the new spacer, the proposed spacer formation method can be easily applied to low-temperature glass-compatible AMLCD process with processing temperature less than 600 °C. Next, a 300-nm polycrystalline silicon layer was deposited by LPCVD at 620 °C with SiH_4 as the reaction gas. Then, the polycrystalline silicon gate was defined by photolithography and etching [Fig. 1(a)]. It should be noted that an optional LDD implant can be performed at this stage to form the LDD transistors. However, no LDD implant is applied in our experiment to simplify the processing (i.e., so offset devices are obtained instead). Afterwards, wafers were placed into the chemical

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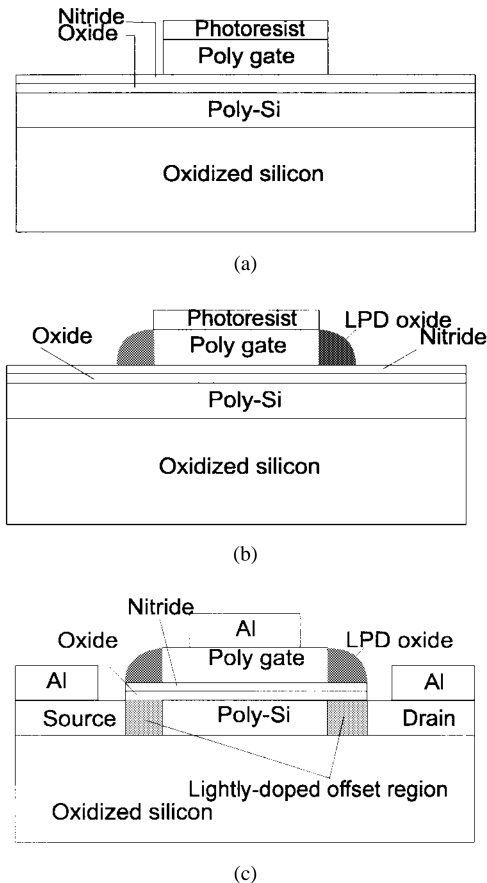


Fig. 1. Key processing steps for fabricating the novel poly-Si TFT: (a) after poly-Si gate definition, (b) after selective deposition of oxide sidewall spacer by one-step selective liquid phase deposition, and (c) final structure of the novel TFT.

solution as described above at 23 °C for 8 h in order to grow the selective LPD oxide spacer, which is formed laterally along the sidewall of poly-Si gate [Fig. 1(b)]. Finally, self-aligned source and drain regions were formed by phosphorous (with 5×10^{15} cm^{-2} at 55 KeV) or BF_2 (with 5×10^{15} cm^{-2} at 90 KeV) implant for n- and p-channel transistors, respectively. An Al film was then deposited and patterned to form the electrodes [Fig. 1(c)], followed by nitrogen anneal at 400 °C for 30 min. A N_2O plasma treatment was also performed for 30 min to enhance the device performance before device measurements [8].

III. Results and Discussion

Based on the growth mechanism we proposed [7], the LPD oxide can only be deposited on surfaces with OH bonds, such as oxide and polycrystalline silicon with thin native oxide, but not on surfaces without OH bonds, such as Si_3N_4 and photoresist. The key feature of the new structure, shown in Fig. 1(b), is the oxide sidewall spacer which is formed by a simple one-step selective LPD, thus avoiding the difficulty of an extra photolithographic step and the risk of plasma damage. Furthermore, the apparatus used for LPD-oxide is easy and inexpensive, and LPD can be easily performed at room temperature. As shown in Fig. 2, the SEM photograph indeed confirms that the selective deposition of LPD oxide spacer occurs only on the exposed sidewall of polycrystalline silicon gate, but not on the overlying photoresist and the underlying Si_3N_4. The width of the oxide sidewall spacer measured from the SEM photograph is about 170 nm.

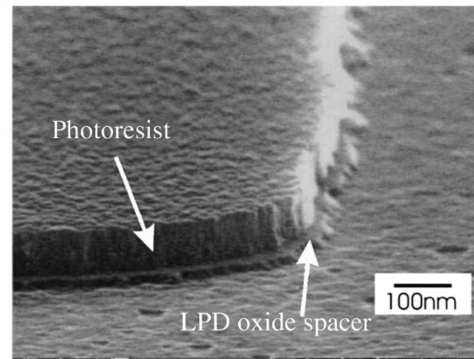
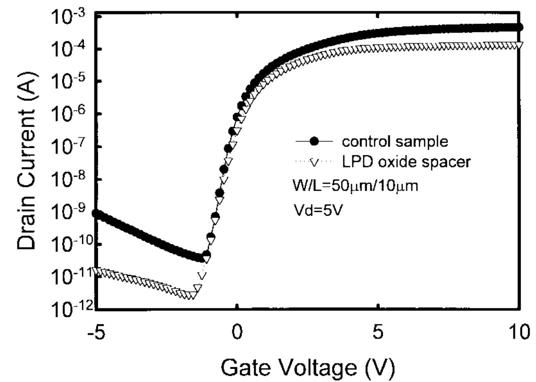
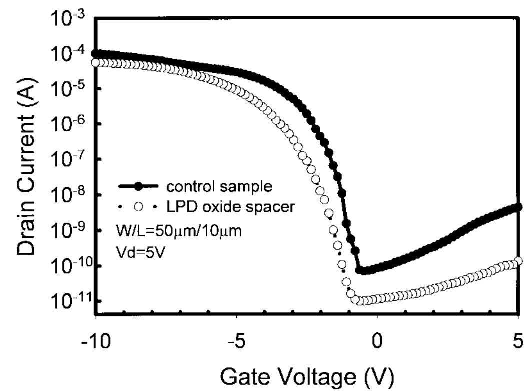


Fig. 2. SEM photograph displaying poly-silicon gate with LPD oxide sidewall spacer.



(a)



(b)

Fig. 3. Typical transfer characteristics for poly-Si TFT's with and without LPD oxide sidewall spacer for (a) n-channel poly-Si TFT and (b) p-channel poly-Si TFT.

Typical transfer characteristics of TFT's with and without LPD oxide spacer are shown in Fig. 3(a) and (b) for n- and p-channel TFT's, respectively. The ON current, OFF current, ON/OFF current ratio, threshold voltage, and mobility are summarized in Table I. Although the ON-state current is slightly decreased for TFT's with LDD oxide spacer, however, the leakage current is reduced significantly. Consequently, the

TABLE I
SUMMARY OF ON CURRENT, OFF CURRENT, ON/OFF CURRENT RATIO, THRESHOLD VOLTAGE, AND MOBILITY FOR VARIOUS DEVICES. ON CURRENT IS MEASURED AT $Vg = 10$ V (-10 V) AND $Vd = 5$ V (-5 V) FOR n(p)-CHANNEL TFT. OFF CURRENT IS MEASURED AT $Vg = -5$ V (5 V) AND $Vd = 5$ V (-5 V) FOR n(p)-CHANNEL TFT

	Ioff(A)	Ion(A)	ON/OFF ratio	Vth(V)	Mobility (cm^2/V-s)
N	8.97×10^{-10}	4.67×10^{-4}	5.2×10^{5}	0.43	22.3
N(LPD oxide spacer)	1.61×10^{-11}	1.39×10^{-4}	8.6×10^{6}	0.72	13.2
P	4.49×10^{-9}	1.02×10^{-4}	2.3×10^{4}	-3.13	3.4
P(LPD oxide spacer)	1.36×10^{-10}	5.62×10^{-5}	4.1×10^{5}	-4.38	2.5

ON/OFF current ratio of TFT's with LPD oxide spacer is greatly improved for both n- and p-channel devices. Specifically, the ON/OFF current ratio is increased from 5.2×10^5 to 8.6×10^6 for the n-channel TFT, while for the p-channel TFT, the ratio is increased from 2.3×10^4 to 4.1×10^5.

IV. CONCLUSION

We have proposed and successfully demonstrated a novel process for fabricating LDD poly-Si TFT's to reduce the leakage current. The key feature of the new process is that the oxide sidewall spacer is formed by a simple one-step selective LPD and is self-aligned to the poly-Si gate. The leakage current is greatly reduced with only a slight ON current reduction, thus resulting in a significant improvement in the ON/OFF current ratio. The new process is simple, inexpensive, requires fewer steps than the conventional methods, and appears to be quite promising for fabricating polysilicon TFT's in future high-performance large-area liquid crystal displays.

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REFERENCES

[1] K. Ono, T. Aoyama, N. Konishi, and K. Miyata, "Analysis of current–voltage characteristics of low-temperature-processed polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 39, p. 792, Apr. 1992.
[2] I. W. Wu, "Poly-Si TFT LCD technology and prospect of future displays," in *EDMS'97*, p. 309.
[3] K. R. Olasupo and M. K. Hatalis, "Leakage current mechanism in submicron polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 43, p. 1218, Aug. 1996.
[4] K. Tanaka, H. Arai, and S. Kohda, "Characteristics of offset-structure polycrystalline-silicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 9, p. 23, Jan. 1988.
[5] K. R. Olasupo, W. Yarbrough, and M. K. Hatalis, "The effect of drain offset on current–voltage characteristics in submicron polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 43, p. 1306, Aug. 1996.
[6] C. T. Liu and K. H. Lee, "An experimental study on the short-channel effects in undergated polysilicon thin-film transistors with and without lightly doped drain structures," *IEEE Electron Device Lett.*, vol. 14, p. 149, Mar. 1993.
[7] C. F. Yeh, C. L. Chen, and G. H. Lin, "The physicochemical properties and growth mechanism of oxide ($SiO_{2-x}F_x$) by liquid phase deposition with H_2O addition only," *J. Electrochem. Soc.*, vol. 141, no. 11, p. 3177, 1994.
[8] F. S. Wang, C. Y. Huang, and H. C. Cheng, "Plasma passivation effects on polycrystalline silicon thin-film transistors utilizing nitrous oxide plasma," *Jpn. J. Appl. Phys.*, vol. 36, pt. 1, no. 4A, p. 2028, 1997.