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Suppression of Fluorine Penetration by Use of *In Situ* Stacked Chemical Vapor Deposited Tungsten Film

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In this study, amorphous-like tungsten films were deposited by a chemical vapor deposition (CVD) process. The deposited film has shown reduced resistance compared with WSi_2, and it also blocked the fluorine atoms from diffusing into the gate oxide. Furthermore, when the amorphous-like tungsten film was deposited prior to a typical CVD tungsten film with a columnar structure, it not only showed excellent barrier characteristics in impeding fluorine impurities, but its resistance was also substantially lower than a single layer of a-W film. It is also found in our work that a bilayer film containing typical CVD tungsten/amorphous-like CVD tungsten is a better wordline structure due to its extraordinarily low resistivity and low fluorine contamination.
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With the continuous scaling down of devices for higher speed and higher density in the semiconductor industry, metallization technologies in ultralarge-scale-integrated (ULSI) circuits have become increasingly complex. For increasing circuit performance, metal interconnections have become a critical limiting factor for circuit speed. For many years tungsten silicide has been studied as a gate electrode (polycide) and a material for interconnection technology.[1-4] However, when using tungsten silicide, wordline delay becomes a serious issue for large dimension memory application such as 64 Mbit dynamic random access memory. One alternative to this problem is to deposit pure metal on top of the polysilicon wordline. A typical CVD tungsten film (c-W) on polysilicon reduces the sheet resistance, thereby reducing resistance-capacitance (RC) time constants. However, c-W deposition exhibits a higher fluorine concentration in the underlayers, for example, polysilicon and oxide. Generally speaking, the typical tungsten CVD film is deposited through the mechanism of surface reaction. The reaction chemistry associated with the reduction of WF_6 to W can generate the fluorine by-product and diffuse into the polysilicon and gate oxide. Therefore, the surface reaction causes a much larger amount of fluorine atoms diffusing much deeper into the substrate. These fluorine atoms, once incorporated into the gate oxide, can damage the electrical characteristics of the device.

Mcinerney *et al*.[5] have reported that the spontaneous gas-phase reaction occurs when the gas-flow ratio of SiH_4/WF_6 is above 1. He also reported that the nucleation rate of silicide deposition depends strongly on the pressure and the carrier gases. In our work, a gas-phase nucleated tungsten was deposited with a SiH_4/WF_6 gas flow ratio of 2.5. X-ray diffraction (XRD) patterns confirmed that this W film was in an amorphous-like phase. Then this amorphous-like tungsten (a-W) film was used as a diffusion barrier layer in our experiment as we designed our wafer configurations. We found out that the by-product of fluorine atoms was effectively blocked by this barrier layer. Although the a-W film successfully suppresses the diffusion of the fluorine impurities, the resistivity of a-W film is about one order higher than c-W film. The purpose of this work is to present a novel method of deposition using CVD technology to deposit a bilayer of c-W/a-W and c-W/a-WN_X film on a polysilicon gate electrode.

Experimental

Four different structures are fabricated in this study: (*i*) aluminum (Al)/polysilicon/SiO_2/Si substrate (control sample), (*ii*) Al/c-W/polysilicon/SiO_2/Si substrate, (*iii*) Al/c-W/a-W/polysilicon/SiO_2/Si substrate, and (*iv*) Al/c-W/a-WN_X/polysilicon/SiO_2/Si substrate. First, n-type silicon wafers of <100> orientation with a resistivity of 5-7 Ω cm were selected and chemically cleaned prior to a subsequent film deposition. Next, the 250 nm thick polysilicon films were doped with phosphorus prior to the metal film deposition. The sheet resistance of the polysilicon films was in the range of 28-35 Ω/□. The polysilicon substrates were dipped in a H_2O:HF (100:1) solution for 2 min etch, followed by a deionized (DI) water rinse prior to loading in the vacuum chamber of W-CVD.

The thickness of a-W film is 50 nm. And all of the c-W films are deposited with the same thickness, *i.e.*, 200 nm. These films were all prepared by CVD process. The deposition conditions for c-W films were prepared as follows: the substrate temperature was 300°C, the gas pressure was 0.1 Torr, and the flow rates of SiH_4/WF_6 were 8/20 sccm. The a-W films were deposited in the same conditions, except that the flow rates of SiH_4/WF_6 were 12.5/5 sccm. The bilayer c-W/a-W films were formed by *in situ* deposition of a c-W film on the a-W layer. The c-W/a-WN_X films were formed by using *in situ* N_2 plasma to treat the a-W film at 300°C for 5 min before the c-W film was deposited. Rapid thermal annealing (RTA) was used to anneal these wafers at 600 to 800°C for 1 to 5 min. The comparisons of the sheet resistance of these three different kinds of tungsten films are also included in this paper.

All as-deposited and annealed samples were subjected to the following measurements. The sheet resistance of each metal film without Al layer was randomly measured on five different locations by a four-point prober. The thickness of each film was determined by using a scanning electron microscopy (SEM) to inspect the cross section of the films. The intermetallic formation of the silicon-tungsten interface was analyzed by utilizing X-ray diffraction (XRD). Surface morphologies were investigated by the use of optical microscopy (OM) and SEM and the atomic concentrations of P, F, Si, and W in sample wafers were examined by secondary ion mass spectrometry (SIMS). Finally, the correlation between the redistribution of fluorine atoms and its corresponding electrical properties after annealing was analyzed by the HP4156B semiconductor parameter analyzer and the Keithley package 82 system.

Results and Discussion

The sheet resistance of as-deposited CVD tungsten was measured randomly with a four-point probe. The samples were measured on five different locations. The resistivies of a-W film and c-W film were found to be 160 and 16 μΩ cm, respectively. After nitrogen plasma treatment, the resistivity of the a-WN_X sample had increased to 176 μΩ cm. Although both a-W and a-WN_X films revealed good thermal stability, their resistivity showed much higher values as compared with c-W film. Subsequently, we deposited c-W film on a-W and a-WN_X film to form two separate bilayer structures of c-W/a-W and c-W/a-WN_X film. After analysis, we found that the sheet resistance of both bilayer tungsten films (0.95 Ω/□ for c-W/a-W, 1.1 Ω/□ for c-W/a-WN_X) was very close to the sheet resistance level of c-W film (0.89 Ω/□).

Moreover, adding a-W or a-WN_X films to the sample wafer could provide us with an additional benefit. It was found that both a-W and

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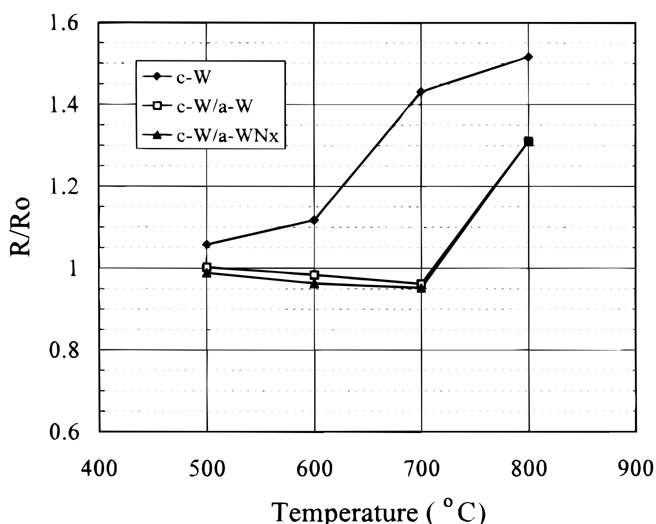
a-WN_X films are excellent barrier materials for reducing junction spiking. The sheet resistance increase in Fig. 1 is defined as the ratio of R to R_0 of which R_0 denotes the sheet resistance of as-deposited c-W/a-W bilayer film and R is the sheet resistance of the various annealed polycide films. In Fig. 1a, the c-W sheet resistance increased 45% after annealing at 700°C for 1 min. However, when annealing bilayer tungsten film at 800°C for 1 min, there was only a 30% increase in sheet resistance. We also found that the bilayer tungsten films sheet resistance decreases when the annealing temperature is below 700°C. This demonstrates that a bilayer tungsten film (c-W/a-W or c-W/a-WN_X) has a more stable interface structure than a single layer c-W film. In Fig. 1b, both c-W/a-W and c-W/a-WN_X are excellent thermal stable materials even annealed at 700°C for 5 min. The decreasing of the sheet resistance is attributed to the following: (*i*) The crystalline structure of c-W possessed an amorphous-like phase when it was deposited on an amorphous-like phase seed layer, and this c-W film was recrystallized to the lower resistivity of α-phase tungsten [α-W(110)] after postthermal treatment (see Fig. 3b and 3c); (*ii*) the grain size of bilayer tungsten grew larger during annealing process.[6]

Figure 2a shows 200 nm of as-deposited c-W film on polysilicon film. We found that almost 50 nm of polysilicon was consumed;



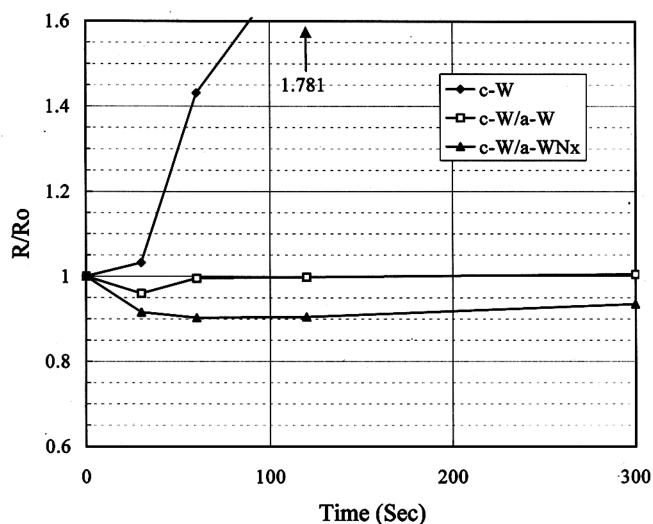
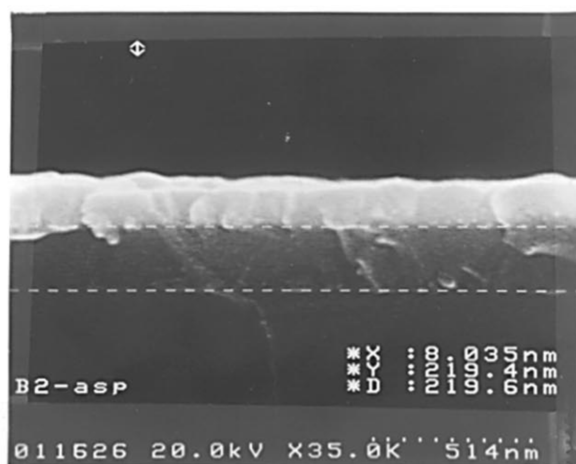
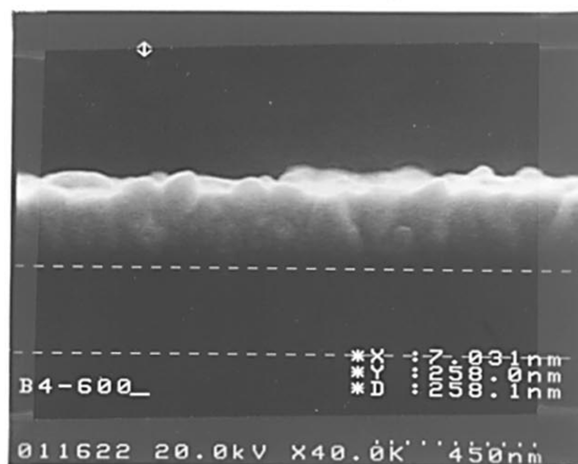


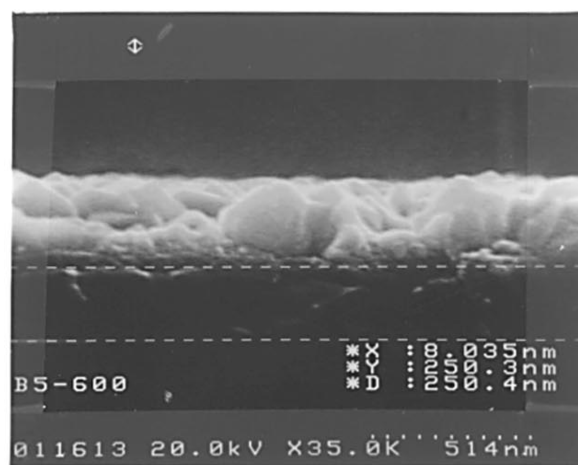
Figure 1. Change of sheet resistance of c-W, C-W/a-W, and C-W/a-WN_X films on poly-Si substrate (R_0 is about 0.95 Ω/□) (a, top) after annealing in N_2 ambient at various temperatures for 60 s, (b, bottom) afer annealing in N_2 ambient at 700°C for different annealing times.



(a)



(b)



(c)

Figure 2. The cross section of (a) as-deposited c-W (200 nm)/polysilicon (250 nm) structure, (b) c-W (200 nm)/a-W (50 nm)/polysilicon (250 nm) structure after annealing in N_2 ambient at 600°C for 5 min, and (c) c-W (200 nm)/a-W (50 nm)/polysilicon (250 nm) structure after annealing in N_2 ambient at 600°C for 5 min.

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thus, even without thermal treatment the thickness of polysilicon film was difficult to control. However, when depositing a 250 nm thickness of bilayer tungsten [c-W (200 nm)/a-W (50 nm) or c-W (200 nm)/a-WN_X (50 nm)] on the polysilicon film, we could not find any significant consumption of the polysilicon film. This implies that the thickness of polysilicon can be adequately controlled by a-W film. This also indicates that a thin a-W or a-WN_X layer is a good propagating layer for c-W deposition. Further, after annealing at 600°C for 5 min, we also found no significant consumption in the polysilicon film as shown in Fig. 2b and c. This again demonstrates that a thin a-W or a-WN_X barrier film will improve the stability between the metal and polysilicon interface.

Figure 3 shows the diffraction patterns of three types of tungsten samples. Figure 3a reveals the single layer c-W on polysilicon metal oxide semiconductor (MOS) capacitors after various annealing conditions. From curve B in this figure, we found that a hexagonal tungsten silicide H-WSi_2(002) appeared after annealing at 600°C for 5 min. The hexagonal tungsten silicide will transform into tetragonal phase after being further annealed, such as 700°C (curve C) and 800°C (curve D). The as-deposited single layer film c-W film exhibits a major tungsten peak of α-W(110) (curve A). On the other hand in Fig. 3b and c, the as-deposited bilayer tungsten film (c-W/a-W and c-W/a-WN_X) shows an amorphous-like phase [no α-W(110) peak was observed]. Again from curve B in Fig. 3b and c, we found that the amorphous-like bilayer tungsten film was recrystalized to α-phase tungsten after being annealed at 600°C for 5 min. From our previous work,[7] we could not find this α-phase tungsten peak, α-W(110), after a single layer of a-W film was annealed. In Fig. 3b and c however, we found this α-phase W(110) after the wafer was annealed at 600°C for 5 min. We inferred that the top c-W layer was changed into a low resistivity α-phase tungsten, as mentioned above. From the sheet resistance measurements shown in Fig. 1, we found that the sheet resistance of c-W films began to sharply increase at 700°C. This indicates that the Si atoms diffuse into the c-W film as the rapid thermal annealing (RTA) temperature reaches 700°C (Fig. 3a curve C). In Fig. 3b and c, we did not find any tungsten silicide peaks in the c-W/a-W and c-W/a-WN_X bilayer structures after annealing at 700°C for 5 min (curve C). The a-W and a-WN_X film again show good thermal stability. This is consistent with the findings shown in Fig. 1. After further annealing at 800°C for 5 min, curve D shown in Fig. 3a, b, and c, resulted in many tungsten silicide peaks. This is due to the fact that the tungsten films were reacting with the underlayer polysilicon.

Figure 4a shows the c-W/polysilicon/SiO_2/<Si> multilayer SIMS depth profile. In this group from which wafers were not exposed to

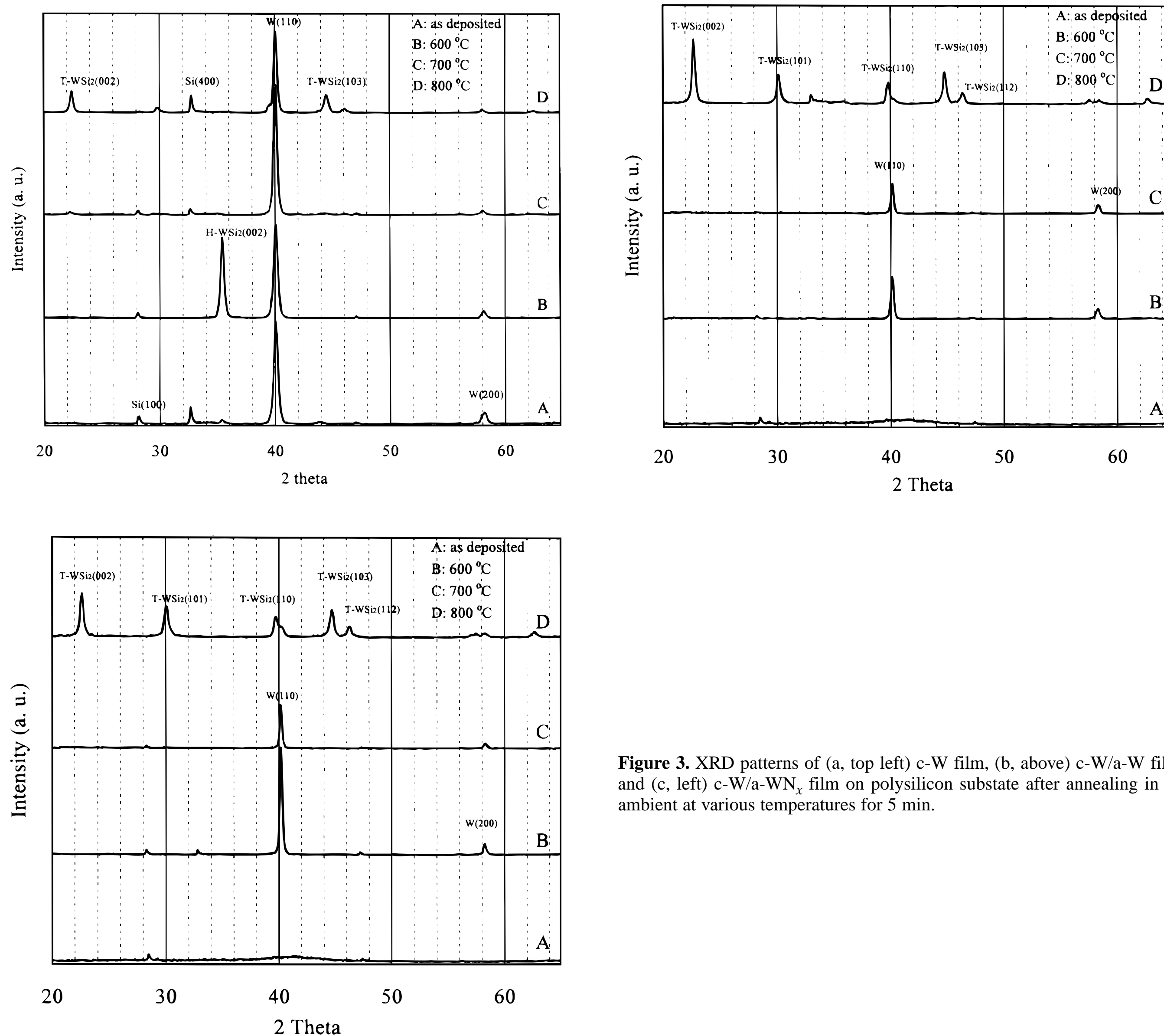

Figure 3. XRD patterns of (a, top left) c-W film, (b, above) c-W/a-W film, and (c, left) c-W/a-WN_x film on polysilicon substate after annealing in N_2 ambient at various temperatures for 5 min.

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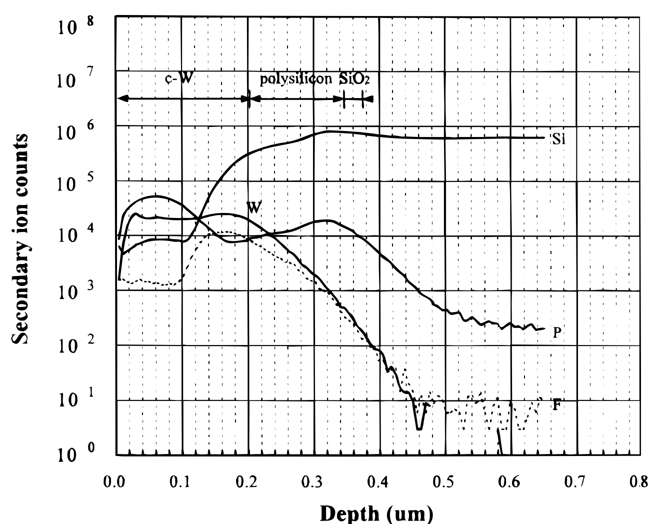
thermal treatment, we found that fluorine atoms can diffuse into the gate oxide and phosphorus atoms can diffuse into the c-W film. We also found that a significant thickness of the polysilicon film was consumed during the c-W film deposition. This is consistent with the SEM picture of Fig. 2a. This again shows that during the c-W film deposition, surface reaction is the dominant factor. At the same time this consumption of polysilicon can cause a large amount of phosphorus atoms in polysilicon getting into the c-W film. Therefore, what we need is a CVD tungsten process that can retard fluorine atom penetration, phosphorus atom redistribution, and silicon consumption. In Fig. 4b, we found that the bilayer c-W/a-W tungsten structure, without having the N_2 plasma treatment, possessed the abovementioned characteristics. As shown in Fig. 2b and c, no consumption of the polysilicon was found after the bilayer tungsten film's deposition. We deduced that the a-W film deposition process is dominated by gas-phase nucleation. Furthermore, examining various samples of different film configuration we observed that a-W thickness stays the same when it is deposited on SiO_2 and the Si substrate.

Yeh *et al.*[8] had reported that the CVD c-W gate MOS capacitor is much better than the sputtering tungsten gate MOS capacitor. We agree with his observation. However, we believe that as c-W is directly deposited on the SiO_2, its MOS capacitor structure can induce stress and cause fluorine incorporation problems. In this study, we have found that c-W film makes a large amount of fluorine penetrating into the gate oxide even when a stress relief layer of doped polysilicon is present. Some authors[9-10] reported that a polysilicon buffer layer was necessary when using tungsten silicide as a gate electrode. They also suggested that the polysilicon buffer layer should be thicker than tungsten silicide film. We investigated the dielectric strengths of tungsten gate MOS capacitors as shown in Fig. 5a and b. Figure 5a indicates that the as-deposited bilayer tungsten gate MOS capacitor's electrical breakdown field (E_{BD}) distribution is comparable to the control sample. Figure 5a also shows that the E_{BD} of c-W samples is about 2 MV/cm less than the control samples. According to previous reports,[11-15] high concentration of fluorine atoms will break Si–O bonds in the gate oxide causing the structure to weaken. This in turn induces further degradation of the gate oxide after constant current stress. This is consistent with our findings in Fig. 4a, *i.e.*, even without thermal treatment, a large amount of fluorine atoms can diffuse into the gate oxide layer. After RTA annealing at 600°C for 5 min, a further degradation of E_{BD} in c-W gate



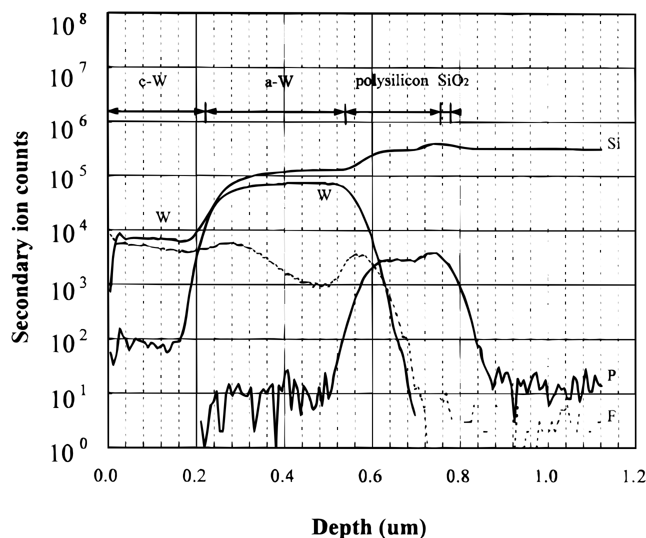
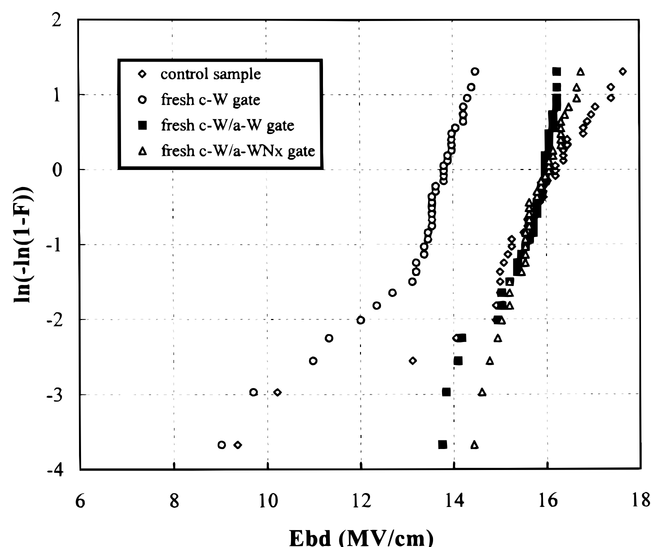


Figure 4. SIMS depth profiles of a multilayer MOS capacitor (a, top) as-deposited c-W (200 nm)/poly-Si (250 nm)/SiO_2 (10 nm)/<Si> structure and (b, bottom) c-W (200 nm)/a-W (300 nm)/poly-Si (250 nm)/SiO_2 (10 nm)/<Si> structure after annealing in N_2 ambient at 600°C for 5 min.



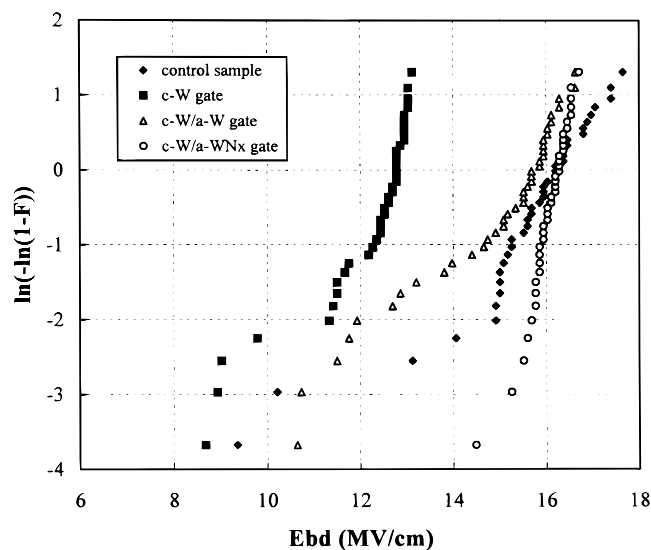


Figure 5. Weibull plot of MOS capacitors' electrical breakdown field (E_{BD}) distribution of (a, top) as-deposited (b, bottom) after annealing at 600°C for 5 min. The MOS capacitors with c-W, c-W/a-W, c-W/a-WN_X, and n^+ polysilicon (control sample) electrodes.

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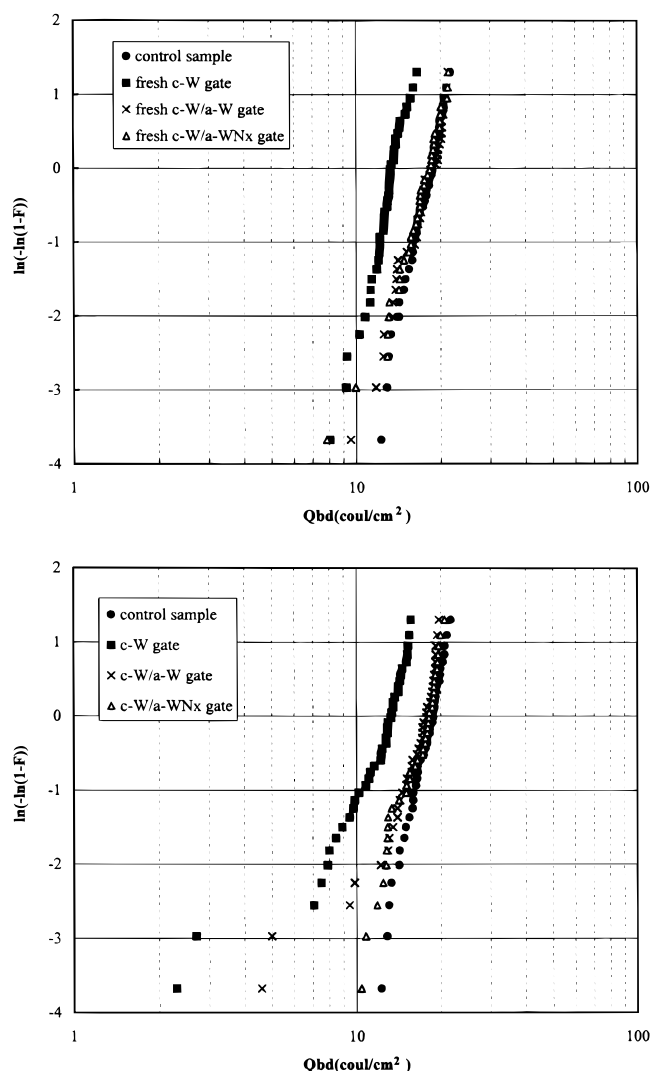

Figure 6. Weibull plot of MOS capacitors' charge to breakdown (Q_{BD}) distribution of (a, top) as-deposited (b, bottom) after annealing at 600°C for 5 min. The MOS capacitors with c-W, c-W/a-W, c-W/a-WN_X, and n^+ poly-Si (control sample) electrodes. The stress current density is 100 mA/cm^2.

MOS capacitors occurred as shown in Fig. 5b. In this figure we also find that the bilayer tungsten samples can maintain high level of E_{BD}. This implies that a bilayer tungsten MOS capacitor structure can successfully retard fluorine atomic diffusion even after a thermal treatment at 600°C.

Next, to test the reliability of 10 nm gate oxide films, we applied a constant current stress of 100 mA/cm^2 on wafers until gate oxide breakdown is detected. Figure 6a reveals the Weibull plots of charge to breakdown (Q_{BD}) for the c-W, c-W/a-W, c-W/a-WN_X, and control polysilicon MOS capacitors. All samples were as-deposited. We found that the c-W samples reveal a degradation in terms of Q_{BD} distribution and the bilayer sample wafers have kept similar distributions with control samples. After further RTA at 600°C for 5 min, we also found that the Q_{BD} of bilayer c-W/a-W MOS capacitors displayed almost no degradation of Q_{BD} as shown in Fig. 6. Furthermore, the bilayer c-W/a-WN_X MOS capacitors exhibited better distribution of Q_{BD} than control samples. Because gate oxides, being fluorinated properly during deposition, receive a beneficial effect of strain relaxation.[12,16,17] As mentioned before, we believe that the poor dielectric strength of c-W gate MOS capacitors is caused by the massive incorporation of fluorine atoms in the gate oxide. We have found that in our bilayer structures, the problem of massive incorporation of fluorine atoms can be significantly reduced.

In this study, we have compared two kinds of bilayer tungsten film structures, *i.e.*, c-W/a-WN_X and c-W/a-W and proved that both are much better than single layer c-W film. Which one of them is better for integrated circuit fabrication? Considering all of the film stacks studied so far, we feel that the bilayer c-W/a-WN_X film has shown slightly better blocking characteristics than the c-W/a-W film. However, from the process viewpoint, the c-W/a-WN_X film needs more cycle time to complete its nitridation process. Furthermore, we found that a "fog-like" surface formed after the c-W/a-WN_X CVD process. This may cause alignment problems during the lithography step. We found, however, by adding a-W film on WN_X as an adhesion layer prior to c-W deposition and this fog-like surface problem can be resolved. Concerning the c-W/a-W bilayer film, there was no fogging problem observed. Also, the c-W/a-W is only slightly less effective than the c-W/a-WN_X film in preventing fluorine atom from diffusion. Considering all of these aspects, we feel that it is more efficient to use the c-W/a-W bilayer film instead of the c-W/a-WN_X bilayer film, especially for the purpose of shortening the processing time.

Conclusion

Chemical vapor deposition is a well-known technology for tungsten film deposition. However, a large amount of fluorine atoms will diffuse into the poly-Si/SiO_2/<Si> multilayers during the deposition step through the grain boundaries of the c-W film. Based on the experimental results in this study, we conclude that in the typical CVD process, the fluorine incorporation has a dramatic impact on the electrical properties of the MOS capacitors. We demonstrated that bilayer tungsten films could both successfully retard the diffusion of fluorine atoms and maintain a lower resistivity than tungsten silicide. We also demonstrated that the charge to breakdown and breakdown field is comparable with the control sample. From this work we feel that the bilayer tungsten films are good film stack structure used for manufacturing gate electrode.

Acknowledgments

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