A Novel Cross-Coupled Inter-Poly-Oxide Capacitor for Mixed-Mode CMOS Processes

Ming-Jer Chen, *Senior Member, IEEE,* and Chin-Shan Hou, *Member, IEEE*

***Abstract*— The inter-poly-oxide (IPO) capacitor is one of the main elements in present mixed-mode CMOS process technologies. However, the phenomenon of poly depletion causes a significant change in the measured capacitance with applied voltage. This effect, expressed in terms of the voltage coefficient of capacitance (VCC), can seriously deteriorate analog precision. In this letter, a novel cross-coupled scheme is proposed for the IPO capacitors. The resulting VCC has a very low measured value of 2 ppm/V in a 0.35-μm standard mixed-mode CMOS process, achieved without any unconventional approaches.**

***Index Terms*—Analog circuits, capacitor, CMOS, mixed-mode, poly depletion, voltage coefficient of capacitance.**

I. Introduction

IT IS well known that the capacitance of a parallel-plate capacitor is normally a function only of the area of the electrode, the dielectric constant of the dielectric, and the thickness of the dielectric. This assumes that both electrodes are metallic conductors. However, if one of the electrodes is n^+ polysilicon, a depletion region extending into the polysilicon is formed at the polysilicon-dielectric interface, thereby rendering the capacitance of such a structure somewhat lower than if both electrodes had been metallic. An important consequence of this phenomenon [1] is that when voltage is applied across the plates, the depletion layer in the polysilicon grows or shrinks, depending on the polarity, thereby reducing or increasing the measured capacitance. This effect can be expressed in terms of the voltage coefficient of capacitance (VCC) [1]. In many integrated circuits this is not a problem but in the areas of analog or mixed-mode circuits (such as analog-to-digital converters, for example), this cannot be tolerated due to stringent precision requirements for scaled process technologies [2], [3]. To alleviate this problem, some approaches in the process phase such as extra metal-to-polycide capacitor module [2] and additional process steps or modifications [3] were reported.

In this letter, we present a CMOS compatible, cross-coupled scheme for the inter-poly-oxide (IPO) capacitors in present standard mixed-mode fabrication processes. This scheme can ensure a very low VCC value without any unconventional approaches.

Manuscript received November 11, 1998; revised January 26, 1999. This work was supported by the National Science Council under Contract NSC-87-2215-E009-038.

M.-J. Chen is with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

C.-S. Hou is with the R&D Department, Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan, R.O.C.

Publisher Item Identifier S 0741-3106(99)05674-8.

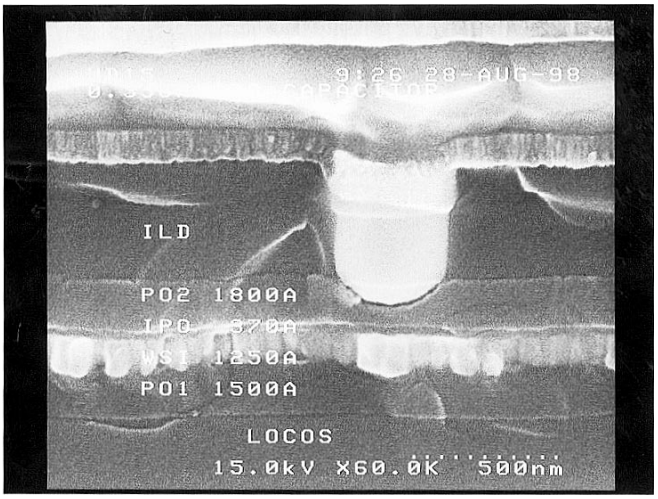


Fig. 1. SEM photograph of the cross section of an IPO capacitor. The corresponding oxide thickness was 370 Å.

II. Experiment and Results

A 0.35-μm mixed-mode polycide process was utilized to realize the IPO capacitors. In this process, the first layer of polysilicon Poly1 was deposited by *in situ* phosphorous doped poly at 570 °C to a thickness of 1500 Å. Then, a 1250-Å thick layer of tungsten silicide WSix was formed on the top surface of Poly1. Next, the dielectric was formed by oxidation at 800 °C to a thickness of 370 Å, which was followed by a 1800-Å thick Poly2 layer deposited by *in situ* phosphorous doped poly. Phosphorous was also implanted into Poly2 to increase the dopant concentration of Poly2. In our work, the phosphorous implant was split with a wide dose and energy range of 1×10^{15}– 1×10^{16} cm^{-2} and 60–100 KeV. Fig. 1 depicts the SEM photograph of one of the finished capacitors. It was found that the measured capacitance depends significantly on applied voltage, as reflected by a VCC of 120–150 ppm/V. This is a large value that cannot be tolerated and cannot pass the general specification of 100 ppm/V. Fig. 2 depicts capacitance–voltage (C–V) data carefully measured five times on one sample by using the HP4284 analyzer. In Fig. 2, the slope of the fitting line across the illustrated voltage range, divided by the zero-bias capacitance, determines a VCC of about 130 ppm/V. The mechanism responsible can be inferred from the measured doping profiles in Fig. 3. From these figures, we can observe four distinct regions: Poly2, IPO, WSix, and Poly1. A layer of tungsten silicide, which is a metallic conductor, is formed on Poly1, so it has a depletion free interface. Since there is no corresponding

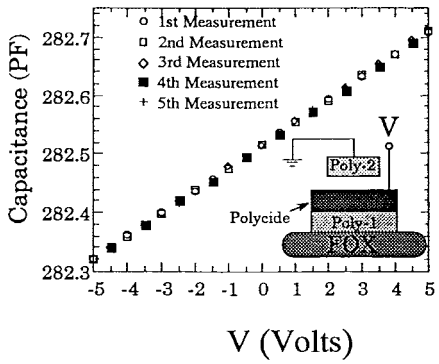
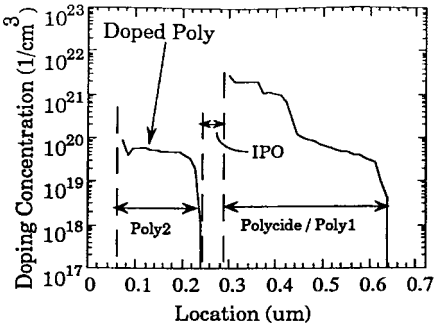


Fig. 2. Experimental C–V data of the IPO capacitor for five measurement times. This characteristic is dominated by odd term. The area $= 2 \times 300\ \mu\text{m} \times 500\ \mu\text{m}$. The inset shows the measurement condition. The phosphorous implant split condition was 80 KeV, $5 \times 10^{15}\ \text{cm}^{-2}$.



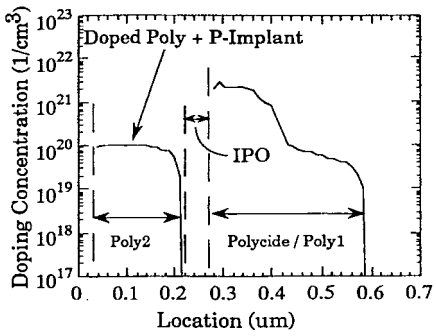


Fig. 3. Measured doping profiles by a spreading resistance probe for the IPO capacitors with and without P implant for Poly2. The latter split condition was 80 KeV, $1 \times 10^{16}\ \text{cm}^{-2}$.

layer of tungsten silicide between Poly2 and IPO, a depletion region develops only within the Poly2. With increasing applied voltage on Polycide/Poly1, this depletion region width shrinks, producing an increase in the measured capacitance as shown in Fig. 2.

Fig. 4 depicts the proposed cross-coupled scheme that is easily implemented during the layout phase. The two IPO capacitors are formed side-by-side and then cross connected; that is, the bottom plate of one of the capacitors is connected to the top plate of the other capacitor, and vice versa. This arrangement makes the two capacitors polarized in opposite directions at all times so that the corresponding VCC's cancel each other. Therefore, the combined structure with a net VCC close to zero can be expected. Indeed, this is true as shown in Fig. 4. Fig. 4 exhibits that the measured capacitance is almost

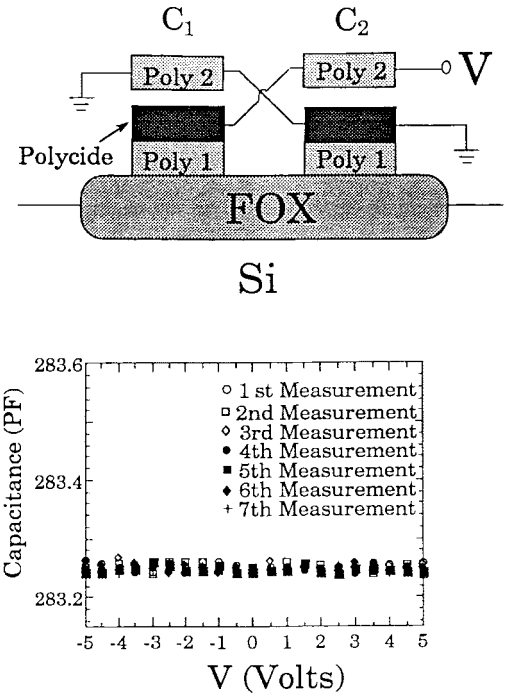


Fig. 4. Experimental C–V data of the cross-coupled IPO capacitor for seven measurement times. The total area $= 2 \times 300\ \mu\text{m} \times 500\ \mu\text{m}$. Also plotted is the cross-coupled scheme for two matched IPO capacitors C_1 and C_2. The phosphorous implant split condition is the same as that in Fig. 2. The effectiveness of the proposed method is determined by the presence of odd terms and absence of even terms.

unchanged for a wide voltage range of -5 to $+5$ V as well as for seven measurement times. The corresponding VCC is around 2 ppm/V. This is a very low value as compared with 3 ppm/V in 700-Å oxide metal-to-polycide capacitor [2] and 38 ppm/V in 0.3-μm mixed-mode process [3]. The other two merits of the cross-coupled scheme can be drawn. First, it is fully compatible with present standard mixed-mode CMOS processes. Thus, the advantages such as low cost and high yield can be maintained. The second is almost the same area consumption for the same capacitance value. In other words, in the layout phase an IPO capacitor can be separated equally into two matched parts. They are cross connected and adjacent to one another with a minimum separation of 0.6 μm in an 0.35-μm process. Apparently, this separation consumes far less area relative to the total IPO capacitor area.

III. Conclusion

A novel cross-coupled IPO capacitor in an 0.35-μm mixed-mode CMOS polycide process has successfully improved the voltage coefficient to 2 ppm/V, a very low value relative to those reported so far. This promising capacitor structure can be easily achieved in the layout phase, without introducing extra modules or additional process steps into the conventional mixed-mode process.

Acknowledgment

The authors would like to express their sincere thanks to the reviewers for their kind help in improving and editing the manuscript.

REFERENCES

[1] J. L. McCreary, "Matching properties, and voltage and temperature dependence of MOS capacitors," *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 608–616, Dec. 1981.

[2] C. Kaya, H. Tigelaar, J. Paterson, M. de Wit, J. Fattaruso, D. Hester, S. Kiriakai, K. S. Tan, and F. Tsay, "Polycide/metal capacitors for high precision A/D converters," in *IEDM Tech. Dig.*, Dec. 1988, pp. 782–785.

[3] T. Ishii, M. Miyamoto, R. Nagai, T. Nishida, and K. Seki, "0.3-μm mixed analog/digital CMOS technology for low-voltage operation," *IEEE Trans. Electron Devices*, vol. 41, pp. 1837–1842, Oct. 1994.