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A ULSI shallow trench isolation process through the integration of multilayered dielectric process and chemical–mechanical planarization

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Abstract

A multilayer thin film structure ($SiO_2/SiN_x/SiO_2$) with a one-step chemical–mechanical polish (CMP) process is developed for shallow trench filling and planarization for ULSI devices in the quarter micron regime. By fine-tuning the plasma-enhanced chemical vapor deposition (PECVD) conditions we successfully modified the stoichiometry and other characteristics of the as-deposited SiN_x and oxide films. As these film characteristics are changed, the CMP removal rate selectivity between sacrificial oxide and nitride stopper layer can also be adjusted. Correspondingly, the CMP process latitude for shallow trench isolation in 0.25 μm memory devices can be broadened by sequentially depositing multilayered oxide and nitride films with adjustable characteristics and CMP removal rates. Dishing-free wide trench areas with excellent planarity can be achieved through the integration of the proposed multilayered PECVD oxide/nitride scheme and the one-step CMP process. © 1999 Elsevier Science S.A. All rights reserved.

Keywords: Multilayer thin film; Chemical–mechanical polish; Dielectrics; Shallow trench isolation; Silicon local oxidation

1. Introduction

For a long time, local oxidation of Si (LOCOS) was the standard technology to provide electrical isolation between active devices for integrated circuits (IC). As demands for smaller geometry and higher circuit density become stronger, even more stringent requirements are being placed upon the isolation performance, and problems with LOCOS begin to surface. For example, the lateral encroachment of field oxide into device active areas and the poor planarity set the limitations for the utilization of this technology beyond 0.25 μm generation. In light of these limitations, an alternative process called shallow trench isolation (STI) has been pursued actively by IC manufacturers as the substitute to LOCOS for device isolation [1]. STI allows for higher chip density and thus promotes more efficient use of Si wafers. A typical STI process involves etching a trench pattern through a nitride layer, a thin pad oxide layer, and into the silicon. Subsequently, a chemical vapor deposited (CVD) oxide is laid on the entire wafer, filling into the trench area and overlying the nitride-protective active region. A chemical–mechanical polish (CMP) step follows then to planarize the topography from previous deposition processes and stops finally on the nitride layer. The remaining nitride is removed subsequently by wet chemistry or reactive ion etching (RIE). The planarization issue is perceived as the most critical step to the success of STI [2,3]. Specifically, due to pattern density effects, nitride thickness after CMP can vary, creating step height variation and, in some cases, promoting overpolish of nitride layer, leading to deleterious damage of the active region. Along with the overpolish and pattern density issues is the dishing into the oxide-filled trench region that may degrade the isolation performance. Extensive efforts have been invested to resolve these problems. These include adjustments in thickness of trench-fill layer [2] and its characteristics (e.g., Poly-Si, HDP-CVD, SOG, etc.) [3,4], modifying slurry chemistries to achieve high oxide/nitride polish selectivity [5,6], implementation of a post-CMP RIE step to assist planarization [7,8], and layering the trench oxide with an additional nitride [9].

From a process integration point of view, a feasible and manufacturable STI process should take into account simultaneously the thickness, characteristics and CMP performances of trench-fill layer and nitride stop layer, so as to optimize the process latitude while minimizing overpolish

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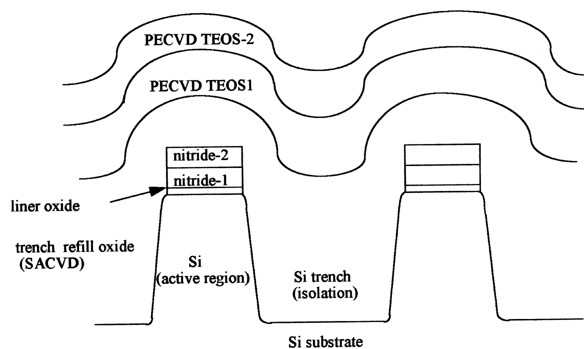

Fig. 1. Cross-sectional view of the multilayer thin film structure for shallow-trench-isolation process.

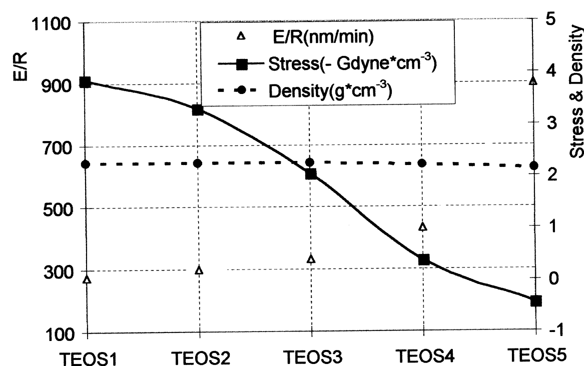

Fig. 2. Effects of $TEOS/N_2O$ gas flow ratio on film stress, NH_4F-buffered HF chemical wet etch rate and film density of oxides.

and dishing. In addition, to reduce process complexity, use of an additional stop or sacrificial layer or an extra RIE step to help achieve planarity should be avoided. Based on the perspectives above, in this investigation, we modify the stoichiometry and other characteristics of the plasma-enhanced chemical vapor deposition (PECVD) SiN_x stop layer and oxide trench fill layer, in order to optimize and improve the CMP process performances such as planarity, dishing, selectivity. Such modifications in thin film characteristics would help enhance the throughput of CMP process itself for the implementation of shallow trench isolation into 0.25 μm device manufacturing.

2. Experimental

In this study, the multilayer thin film structure for the STI process is manufactured by the combination of various thin film deposition/growth techniques. The process sequence is summarized as follows:

1. PECVD nitride stacks (nitride 1 and nitride 2) are grown on 150 mm Si wafers as the polish stopping layers. The NH_3/SiH_4 gas flow rate ratio is adjusted to modify nitride film properties. The thickness of the nitride stacks is varied to evaluate the CMP process latitude.
2. I-line lithography and trench etch.
3. Sidewall oxidation is performed to grow a thin oxide liner to protect the active region from subsequent processing and to achieve better process control and device performance.
4. Bilayer subatmospheric chemical vapor deposited (SACVD) oxides are filled into the 450 nm deep trench at 400°C with TEOS (tetraethoxysilane)/O_3 (ozone) gas mixtures. The ozone concentration is adjusted so that a low-ozone oxide (100 nm) and a high-ozone oxide (500 nm) can be deposited subsequently.
5. Dual-frequency PECVD TEOS oxides are deposited as CMP sacrificial layers. In this process, the N_2O gas flow rate is maintained at 4.8 l/min, while the flow rate of TEOS gas and low/high-frequency power ratio are both varied to modify the stoichiometry and characteristics of the deposited oxides. The $TEOS/N_2O$ gas flow ratio is increased from TEOS1 to TEOS5, representing different oxide film characteristics. The cross-sectional view of the entire thin film structure is shown in Fig. 1.

Table 1
PECVD TEOS oxide characteristics

TEOS	TEOS1	TEOS2	TEOS3	TEOS4	TEOS5
Stress (MPa)	386	330	205	38	−44
Density (g/cm^3)	2.27	2.27	2.26	2.23	2.16
R/R (nm/min)	185.6	218.7	245.6	261.7	333.1
E/R (nm/min)	273.3	301.1	332.1	433.9	898.9

CMP experiments were carried out in an IPEC 472 Avanti polisher with IC1000/Suba IV pad and SC-112 slurry. The down force, back pressure, platen rpm, and carrier rpm used were maintained at 7 psi, 2 psi, 30 rpm and 20 rpm, respectively.

After film deposition and CMP, physical and chemical characterization was performed. Standard wafer curvature measurement was used to determine the film stress based on Stoney's equation. Fourier transform infrared (FTIR) spectroscopy was employed to determine the bonding nature of the oxide and nitride films. Wet chemical etching rate was determined using 10:1 buffered oxide etchant (BOE). CMP

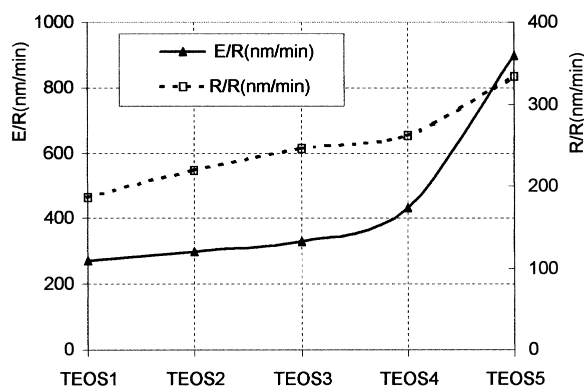

Fig. 3. Correlation between the wet etch rate and CMP removal rate of PE-TEOS oxide.

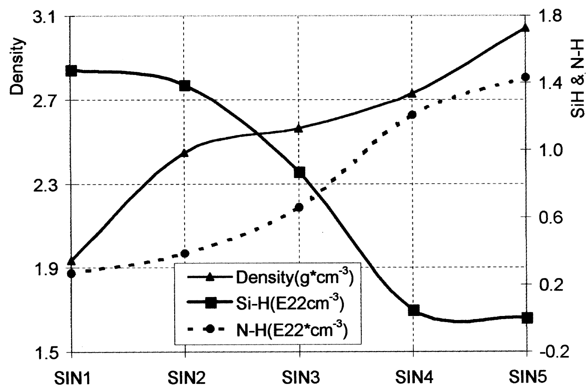

Fig. 4. Effects of hydrogen-related bond in PECVD silicon nitride films on film density.

removal rate (CMP R/R) was calculated from difference in film thickness measured at 49 points across the wafer.

3. Results and discussion

Table 1 summarizes the experimental results of PECVD TEOS oxide characteristics and their CMP results. These data are reproduced in Fig. 2, which shows that as the TEOS/N_2O gas flow ratio increases from TEOS1 to TEOS5, the as-deposited film stress changes from high tensile to low compressive, while the film density decreases slightly. This decrease in tensile stress is accompanied by the increase in NH_4F-buffered HF wet etch rate. Such an increase in wet etch rate also correlates well with the rise in CMP polish rate, as shown in Fig. 3.

However, the above findings seem contradictory to the work by Osenbach and Knolle [10]. They postulated that the presence of tensile stress in the silica structure would increase the electrochemical potential and hence chemical wet etch rate of the oxide film, when the film is immersed into the corrosive aqueous media. Another study [11] pointed out that the water diffusion rate in silica glass is a function of local stress. In that study, it was found that a higher local tensile stress in the film leads to a higher diffusion coefficient of water or H^+ in silica. As a result, films with higher tensile stress should have higher CMP removal rates through enhanced water/slurry diffusion and the stronger reactivity with the alkaline agent in slurry. However, the TEOS/N_2O vapor reactions in plasma environment produce moisture or hydroxyls in the oxide, whose concentration increase with the amount of TEOS [12]. A direct consequence of this is the reduction in film density because the existence of hydroxyl groups, in the form of Si–OH bonds, results in a more open structure in the oxide. Meanwhile, the hydrophilicity of the oxide is enhanced due to the formation of Si–OH bonds. Both of the scenarios above, i.e. reduction in film density and enhancement in hydrophilicity, will enlarge the contact area and hence accelerate wet etch and polish rates, as found in the current study.

The correlation between hydrogen bonding concentration in PECVD silicon nitride films and their respective film density is exhibited in Fig. 4. As shown, both the numbers of Si–H and N–H bonds change the film density significantly. The results are somewhat similar to previous studies on PECVD SiN_x films [13,14]. It has been reported that a higher Si–H/N–H bond density ratio corresponds to a lower SiN_x film density and higher chemical etch rate in aqueous fluoride or chloride media [5,6]. Therefore, it can be postulated that the existence of more Si–H bonds increases the porosity of the PECVD SiN_x, leading to increases in both the chemical etch rate and the CMP removal rate. Increasing the porosity of the dielectrics also increases the specific area immersed in the slurry during CMP process. During the polishing process, the large specific area on the surface will provide larger area for the abrasives in the slurry to scrub the weakly bonded and porous SiN_x film. All of these effects contribute to the enhancement in chemical wet etch rate and CMP polish rate dramatically as shown in Figs. 5 and 6. Table 2 summarizes the material characteristics of PECVD silicon nitride and their respective CMP polish rates. Further improvement in CMP performance can be realized by modifying the stoichiometry of the intermediate nitride stopping layer. This is achieved by modifying bias power while reducing SiH_4/NH_3 gas flow ratio during deposition of PECVD nitride films. The FTIR spectrum shows that the resulting PECVD nitride films have different Si–H content. Concurrently, these as-deposited nitrides exhibit different BOE wet etch rates and compressive stresses, suggesting a significant change in nitride film structure and hence different CMP removal rates. With these changes in film characteristics, a multilayer PECVD SiN_x film deposition process is implemented with the intention to induce high/low CMP removal rates. The process goals are to completely remove the remaining oxide on nitride stop layer, and to prevent CMP dishing effect resulting from over polish. This point will be elaborated later.

To incorporate the above oxide/nitride thin film stacks into the STI process, the thickness and deposition conditions are adjusted in order to broaden the process latitude while

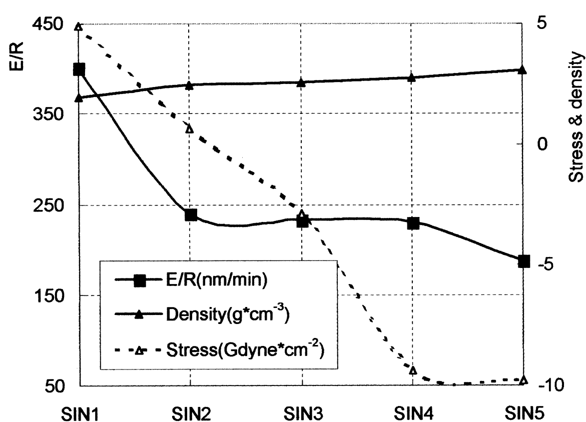

Fig. 5. Effects of stress and film density on chemical wet etch rate of PECVD nitride thin films.

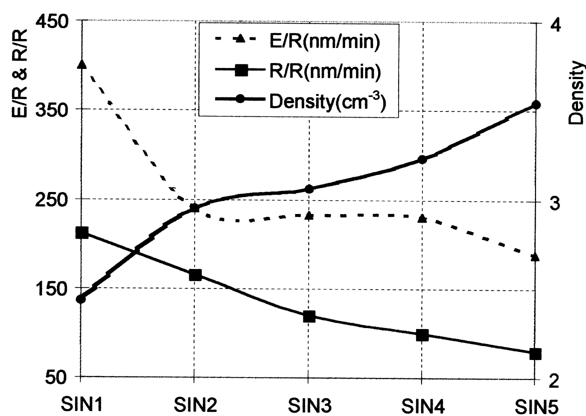

Fig. 6. Effects of chemical wet etch rate and film density on CMP removal rate of PECVD nitrides.

minimizing dishing effects during polishing. A 200-nm thick nitride layer was deposited first on the Si wafer. A 600-nm thick SACVD oxide was then filled into the 450-nm deep trench, whose width varies from 300 nm to 2000 nm. Subsequently, PECVD TEOS oxide layers of varying thickness were deposited and their CMP planarization performances were evaluated in order to optimize the process latitude.

For optimal planarization results, a 400-nm thick TEOS5 (CMP R/R = 333 nm/min) was deposited first followed by a 200-nm TEOS1 (CMP R/R = 186 nm/min). The nitride polish stop layers were formed by sequentially depositing a SIN1 (*nitride 1*, CMP R/R = 212 nm/min) layer of 130-nm thick followed by a SIN5 layer (*nitride 2*, CMP R/R = 80 nm/min). Such a oxide/nitride combination with high/low polish rates effectively enhances the throughput for the STI process. Initially, a TEOS5 oxide layer with a high R/R was adopted for bulk removal. The removal rate was reduced then by inserting a TEOS1 layer underneath, as the polish proceeds towards the oxide/nitride interface. Such a deceleration of polishing action effectively reduces the risk of overpolish and brings the dishing effect, if any, to a controllable extent. A nitride with a slightly higher removal rate (SIN1) than TEOS1 was utilized as the top polish stop layer (i.e. *nitride 1*) in order to compensate the drop in TEOS1 oxide removal rate due to the existence of the nitride substrate. Such a substrate effect [15] results when the vertical displacement during polishing is reduced as the abrasives indent into a film on top of a mechanically harder substrate. The removal rate (R/R) can then be expressed as a function of Young's modulus, the applied pressure, and relative velocity:

$$\mathrm{R/R} = k(1/E_p + 1/E_u) \times P \times V \quad (1)$$

where k is a parameter related to slurry concentration and chemical erosion effects; E_p and E_u are the Young's moduli of the film being polished and the underlying film (substrate); P is the applied down pressure; and V is the relative velocity. The PE-TEOS oxide directly above the

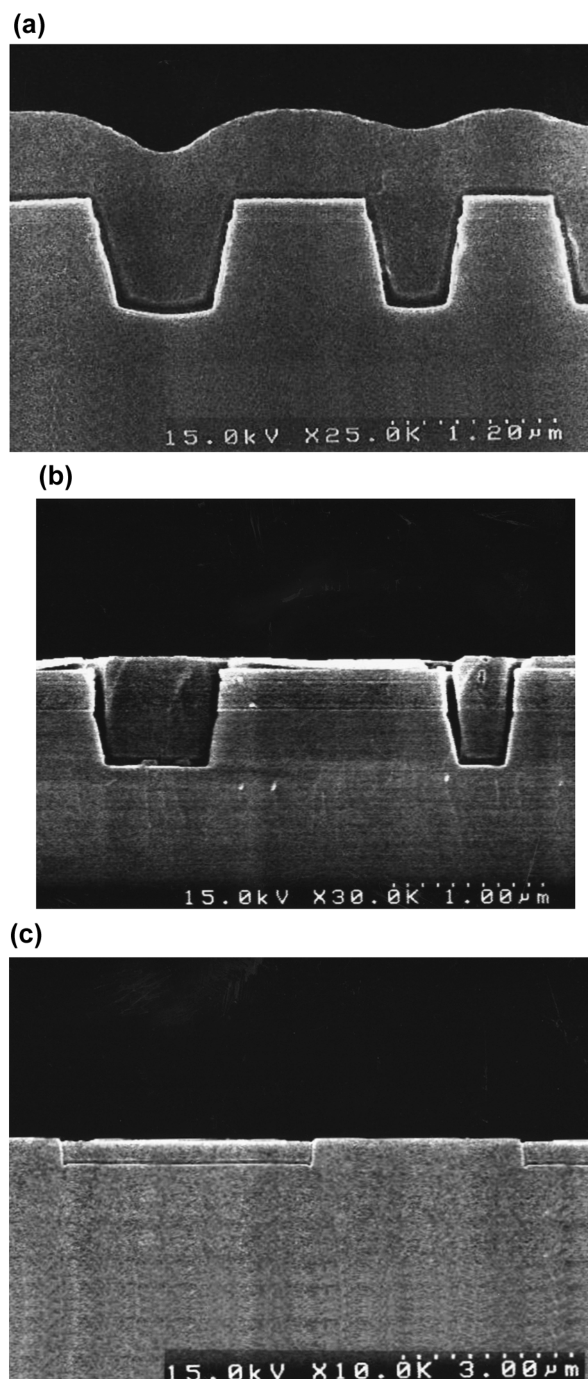

Fig. 7. (a) The multilayer STI structure before CMP and TEOS oxide deposition. (b) STI structure during an intermediate stage of CMP showing nitride remaining on the active region. The SEM sample is decorated to reveal the trench region. (c) The multilayered STI structure after CMP. Global planarization and minimum amount of dishing are achieved for wide trench patterns.

harder nitride layer would exhibit a lower removal rate due to this substrate effect, while that above the trench area would polish at the same rate. Therefore, to maintain a planarized surface, the top nitride layer should be removed at a slightly higher rate than the TEOS1 layer, in order to compensate the dishing into the trench area. Finally, the

Table 2
PECVD nitride characteristics

	SIN1	SIN2	SIN3	SIN4	SIN5
RI	2.28	2.06	1.96	1.90	1.89
E/R (nm/min)	400.4	239.4	232.8	230.4	188.4
CMP R/R (nm/min)	211.9	165.8	119.7	99.7	80.0
Density (g cm^{-3})	1.94	2.45	2.52	2.73	3.04
Si–H (E^{22} cm^{-3})	1.48	1.39	0.87	0.05	0.00
N–H (E^{22} cm^{-3})	0.27	0.39	0.66	1.21	1.43
Bonding ratio (Si–H/N–H)	5.48	3.58	1.32	4.05	1.54
Total-H (E^{22} cm^{-3})	1.76	1.78	1.54	1.36	1.43
Stress (MPa)	490	64	−290	−940	−980

nitride with the lowest removal rate (SIN5) was laid underneath as *nitride 2* to effectively stop the polish action at the interface. At this time, all the PECVD TEOS oxide layer was removed, exposing the underlying SACVD trench oxide and the residual SIN5 layer, which was removed subsequently by wet H_3PO_4 dip.

The above findings serve as useful guidelines to design a multilayer PECVD oxide/nitride dielectric scheme for shallow trench isolation process. Specifically, by introducing oxide/nitride layers with tunable CMP polish rates, the CMP dishing effect can be minimized easily without any modification in slurry chemistry [8] or the implementation of complicated two-step polishing processes [9]. Another advantage of the current process is that the CVD and CMP throughput and process latitude can be expanded simultaneously. Fig. 7a is a SEM micrograph showing the cross-sectional view of a typical thin film structure for STI before CMP. Trenches with different widths can be seen clearly. The STI structure during an intermediate CMP stage is exhibited in Fig. 7b. The SACVD low-ozone oxide was removed to decorate the trench. As shown in the picture, there is some residual nitride remaining on the active region. The final STI structure after CMP is displayed in Fig. 7c. As the picture shows, a wide (4.5 μm) trench with a fully planarized surface is attained and the STI structure is delineated successfully by the CVD/CMP process scheme proposed in this study.

4. Conclusion

By modifying the PECVD deposition conditions we can manipulate the stoichiometry and other characteristics of the as-deposited SiN_x and oxide films for application in the shallow trench isolation process. The CMP removal rates of the PECVD films are fine-tuned and a multilayer thin film stack is proposed in order to allow for a one-step CMP process for the definition of the shallow trench patterns. The implementation of the this multilayer PECVD dielectric process leads to enhancements in the CMP remove rate selectivity and the efficiency of polish stop layer. The integration of the proposed CVD and CMP processes produces a STI structure with a well-planarized surface and minimum amount of dishing.

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