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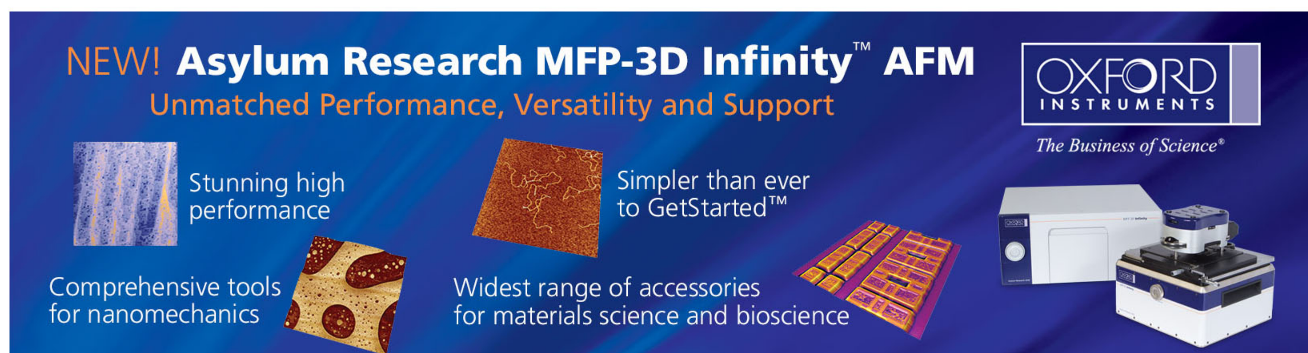

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Temperature-accelerated dielectric breakdown in ultrathin gate oxides

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Temperature-accelerated effects on dielectric breakdown of ultrathin gate oxide with thickness ranging from 8.7 to 2.5 nm are investigated and analyzed. Although superior reliability for ultrathin gate oxide at room temperature has been reported in recent literatures, a strong temperature-accelerated degradation of oxide reliability is observed in this study. Experimental results show that both charge-to-breakdown (Q_{bd}) and breakdown field (E_{bd}) characteristics are greatly aggravated for ultrathin oxide at elevated temperature. The Arrhenius plot also confirms that the activation energies of Q_{bd} and E_{bd} increase significantly as oxide thickness decreases, explaining the higher sensitivity to temperature for thinner oxides. © *1999 American Institute of Physics.* [S0003-6951(99)02024-0]

Ultrathin gate oxide, which is beneficial for low supply voltage and high driving capability, is indispensable for the continuous scaling of ultralarge scale integrated (ULSI) technology towards smaller and faster devices. The reliability of ultrathin oxide is therefore of major concern in the fabrication of state-of-the-art metal-oxide-semiconductor (MOS) devices. Recently, several studies have consistently showed that superior time-dependent dielectric breakdown characteristics are observed for ultrathin oxides at room temperature.[1,2] Therefore, devices with ultrathin gate oxides are expected to be more robust to process-induced damage. However, strong temperature dependence of oxide breakdown has also been reported for gate oxide with thickness of 4 nm.[3] Since in real wafer processing, the gate oxide is subjected to elevated temperature during many wafer processing steps, it is therefore important to study the temperature-accelerated effects in ultrathin oxide for realistic reliability consideration.

The main purpose of this letter is to explore the temperature acceleration effects on ultrathin oxide breakdown. Although it is generally accepted that high temperature degrades oxide breakdown characteristics due to increased interaction between tunneling electrons and oxide lattice,[4] enhancing electron trap generation rate,[5] thereby causing enhanced tunneling-induced trap generation[6] and reduced immunity to electrical stress,[7] however, the exact mechanism involves remains unclear. Many recent studies indeed confirmed that wafer temperature during processing is a crucial parameter for process-induced oxide degradation, and gate oxide is more susceptible to charging damage at elevated temperature.[4,8] However, these studies are limited to gate oxide thicker than 7 nm. In this letter, we investigated the aggravated temperature acceleration effects on oxide breakdown for oxide thickness ranging from 8.7 to 2.5 nm. Our experimental results indicated that ultrathin oxide depicts a much higher sensitivity to temperature.

Test devices used in this study were *n*-channel MOS capacitors and transistors. They were fabricated with a conventional localized oxidation of silicon (LOCOS) isolation with n^+ polycrystalline silicon gate on 6-in.-(100)-oriented *p*-type Si wafer. Gate oxides were thermally grown in O_2/N_2 ambient (with 1/6 flow ratio) at temperatures ranging from 800 to 900 °C. Oxide thickness, ranging from 2.5 to 8.7 nm, was verified by ellipsometry and also by TEM on the monitor wafer. In addition, the thickness was also confirmed by fitting the Fowler–Nordheim (FN) tunneling current on the fabricated devices.[9] Consistent results were obtained among three different methods. Constant current stress (CCS) and ramped $I-V$ measurements were performed to characterize oxide reliability. For oxides thinner than 5 nm, the soft breakdown was used as the breakdown criterion.

Figure 1 shows the 50% Q_{bd} values as a function of oxide thickness under both 25 and 180 °C stressing temperatures. Constant current with a density of 200 mA/cm^2 under gate injection polarity (i.e., $-V_g$) was applied. Typical voltage-time plot under CCS for 2.5 nm-oxide is also shown in the inset of Fig. 1. It is worthwhile noting that for 2.5 nm oxide under this stressing condition, the dominant tunneling mechanism is direct tunneling (i.e., $V_{ox}=V_g-V_{fb}<3.2$ V). It can be seen that the temperature-accelerated dielectric breakdown is aggravated with decreasing oxide thickness, which is believed to be correlated with the occurrence of soft breakdown and will be discussed later. For the thinnest oxide used in this study (i.e., 2.5 nm), more than three orders of magnitude in Q_{bd} degradation is observed when the stressing temperature is elevated to 180 °C from room temperature. As a result, the robustness weakens substantially at high temperature, despite the superior Q_{bd} value at room temperature for 2.5 nm oxide. It is worthy to note that in many processing

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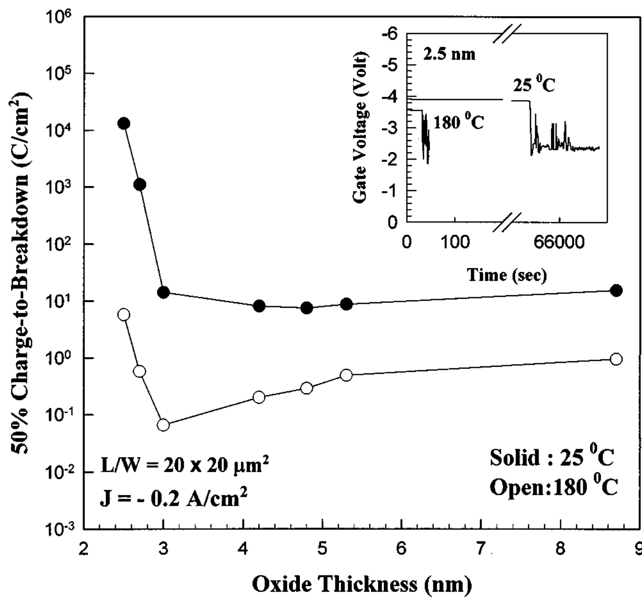

FIG. 1. 50% charge-to-breakdown measured at 25 °C (solid circle) and 180 °C (open circle) under gate injection of -0.2 A/cm^2 as a function of oxide thickness. The area of all capacitors is 4×10^{-6} cm^2. Insert shows typical $V-t$ curves of charge-to-breakdown tests on 2.5 nm oxide at 25 and 180 °C.

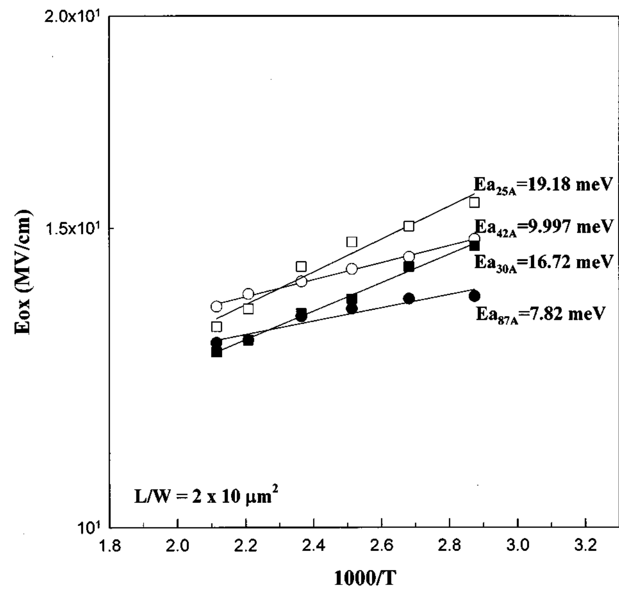

FIG. 3. The temperature acceleration effects on breakdown field, E_{bd}. The temperature is from 348 to 473 K. The polycrystalline silicon depletion effect is also taken into account. Activation energy E_a is also given.

steps (e.g., plasma deposition and etching, CVD, ashing, and ion implantation), the real wafer temperature is higher than the nominal process temperature, due to the heating effects by ion bombardment and electron heating, thereby exacerbating the situation.

The temperature-accelerated oxide breakdown was studied in detail. As shown in Fig. 2, the 50% Q_{bd} values under CCS injection are plotted against the reciprocal of absolute temperature (i.e., $1/T$) for four different oxide thickness splits. From the activation energy (E_a) of Q_{bd}, as extracted from the slope of the plot, the four curves can be roughly divided into two groups, i.e., those thicker or thinner than 4 nm. The activation energy increases by only 0.03 eV when oxide thickness decreases from 8.6 nm (0.30 eV) to 4.2 nm (0.33 eV), indicating a very weak thickness dependence on activation energy. For oxide thinner than 4 nm, however, the activation energy shows a strong dependence on oxide thickness. Specifically, E_a increases to 0.5 and 0.66 eV for 3 and 2.7 nm oxides, respectively. Thus, despite the superior Q_{bd} for the 2.7 nm oxide at room temperature, Q_{bd} becomes worse than that of 8.7 nm oxide when the stress temperature is elevated above 150 °C. The accelerated temperature dependence on dielectric breakdown for scaled oxide may be ascribed to the increasing fraction of the structural transition layer (STL) which is the structural imperfection due to the distorted Si–O_4 tetrahedron network as a result of high stress/strain in the Si/SiO_2 interface. In the STL, the existence of suboxides (Si_2O, SiO, and Si_2O_3) has been previously identified to exist by x-ray photoelectron spectra.[10,11] The built-in compressive strain in the Si–O bonds causes the reduction of the Si–O–Si average bond angle or the Si–Si second neighbor distance.[10,12] In addition, the Si–H bond which results mainly from post-metal anneal in forming gas ambient and the stretched Si–O bond in the STL are proposed to be the precursor of oxide breakdown[13] and is believed to be responsible for the temperature dependence of oxide breakdown.[3,14] It has been reported that the temperature dependence of oxide breakdown can be ascribed to both atomic and molecular hydrogen diffusion released from Si–H bond breaking caused by the anode hole injection[3,15] and that the presence of the compressive strain will lower the diffusion barrier of those hydrogen-related species.[10] Since the STL thickness is approximately 1.0 nm for all oxides,[10] the fraction of STL to gate oxide thickness will increase with scaling. Fourier transform infrared (FTIR) spectroscopy measurements further indicated that the strain at the SiO_2/Si interface indeed increases as oxide thickness decreases.[14] Therefore, the temperature acceleration effect will be enhanced for ultrathin oxides.

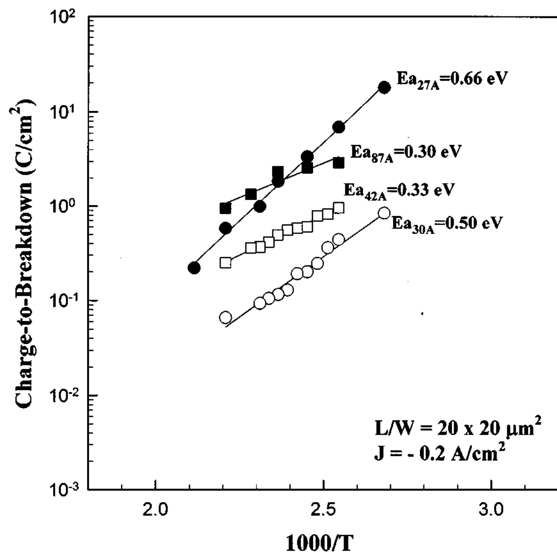

FIG. 2. The temperature acceleration effects on charge-to-breakdown, Q_{bd}. The temperature is from 348 to 473 K. Activation energy E_a is also given. The stress current density is 0.2 A/cm^2 under gate injection.

Figure 3 depicts the Arrhenius plot of oxide breakdown

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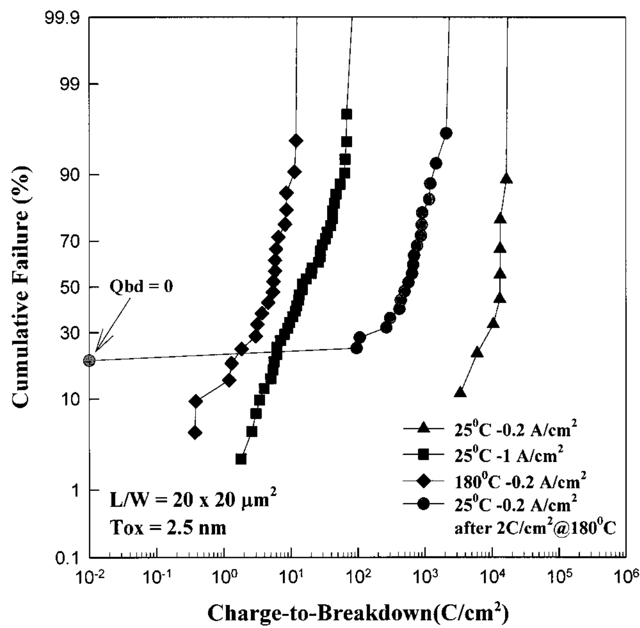

FIG. 4. Cumulative charge-to-breakdown (Q_{bd}) results for 2.5 nm oxide stressed under four different conditions.

field, extracted from ramped $I-V$ measurements, for various oxide thicknesses as a function of temperature in the range 75–200 °C. Test transistors with gate area of $2\times10\,\mu\mathrm{m}^2$ were stressed under substrate injection polarity (i.e., $+V_g$) with source/drain grounded. The polycrystalline silicon depletion effect was taken into account while extracting the breakdown field. At first glance, it is in general agreement with the fact that increasing stress temperature is accompanied by decreasing breakdown voltage, regardless of oxide thickness. As has been mentioned previously, this is ascribed to the increasing interaction between tunneling electrons and the lattice at elevated temperature. The activation energy of breakdown field exhibits the same behavior as that of Q_{bd}, i.e., the activation energy of breakdown field increases monotonously with decreasing thickness. Because of the strong temperature degradation effect in ultrathin oxides, breakdown field of the 2.5 nm oxide is lower than 4.2 nm oxide, while the breakdown field of the 3 nm oxide is lower than that of 8.7 nm oxide, when the stress temperature is raised above 150 °C.

Since the reliability of the 2.5 nm oxide exhibits such an enormous dependence on temperature, it was further analyzed under different stress conditions. As depicted in Fig. 4, MOS capacitors with 2.5 nm oxide were stressed at different temperatures (i.e., 25 and 180 °C) under gate injection polarity with different stressing levels (i.e., 0.2 and 1 A/cm^2). Some test capacitors also received a 2 C/cm^2 (at a stressing current density of 0.2 A/cm^2) prestress at 180 °C before subjected to the 0.2 A/cm^2 stress until failure at 25 °C (circles). As shown in Fig. 4, by increasing the stress level from 0.2 to 1 A/cm^2, three orders magnitude in Q_{bd} reduction is observed. This is because under higher stress levels, the dominant tunneling process changes from direct tunneling (DT) to (FN) tunneling, while electrons in the DT process typically deposit negligible energy in oxides. More importantly, our results also show that prestressing at elevated temperature for even a small stress level (e.g., 2 C/cm^2) can lead to significant Q_{bd} reduction in subsequent stressing at room temperature. Such results indicate that the cumulative nature of Q_{bd} is accelerated at high temperature stress. Hence, both temperature and stress level are important factors for Q_{bd}. One can conclude that any low-level stressing experienced at high temperature during the real wafer fabrication process may cause significant degradation of oxide reliability in the completed MOS devices with ultrathin oxide.

In summary, we have studied the accelerated effects of temperature on the breakdown characteristics of oxides as thin as 2.5 nm. It is shown that temperature-accelerated oxide breakdown is strongly aggravated for ultrathin oxide. Therefore, more attention should be paid to real wafer processing steps that require elevated temperature in order to ensure that gate oxide integrity for ULSI devices employing ultrathin gate oxide is not jeopardized.

[1] B. E. Weir, P. J. Silverman, D. Monroe, K. S. Krisch, M. A. Alam, G. B. Alers, T. W. Sorsch, G. L. Timp, F. Baumann, C. T. Liu, Y. Ma, and D. Huang, Tech. Dig. Int. Electron Devices Meet. **1997**, 73 (1997).
[2] H. Iwai and H. S. Momose, Tech. Dig. Int. Electron Devices Meet. **1998**, 163 (1998).
[3] K. Eriguchi and M. Niwa, Appl. Phys. Lett. **73**, 1985 (1998).
[4] S. Ma, J. P. McVittie, and K. C. Saraswat, IEEE Electron Device Lett. **16**, 534 (1995).
[5] C. F. Chen, C. Y. Wu, M. K. Lee, and C. N. Chen, IEEE Trans. Electron Devices **34**, 1540 (1987).
[6] P. P. Apte and K. C. Saraswat, IEEE Trans. Electron Devices **41**, 1595 (1994).
[7] K. F. Schuegraf and C. Hu, IEEE Trans. Electron Devices **41**, 1227 (1994).
[8] T. Brozekm, Y. D. Chan, and C. R. Viswanathan, IEEE Electron Device Lett. **17**, 288 (1996).
[9] H. C. Lin, M. F. Wang, C. C. Chen, S. K. Hsien, C. H. Chien, T. Y. Huang, C. Y. Chang, and T. S. Chao, Proc. Int. Reliab. Phys. Symp. 312 (1998).
[10] K. Eriguchi, Y. Harada, and M. Niwa, Tech. Dig. Int. Electron Devices Meet. **1998**, 175 (1998).
[11] T. Sorsch, W. Timp, F. H. Baumann, K. H. A. Bogart, T. Boone, V. M. Donnelly, M. Green, K. Evans-Lutterodt, C. Y. Kim, S. Moccio, J. Rosamilia, J. Sapjeta, P. Silvermann, B. Weir, and G. Timp, Symp. VLSI Tech. 222 (1998).
[12] S. Miayazaki, H. Nishimura, M. Fukuda, L. Ley, and J. Ristein, Appl. Surf. Sci. **113/114**, 585 (1997).
[13] D. Arnold, E. Cartier, and D. J. DiMaria, Phys. Rev. B **49**, 10278 (1994).
[14] H. Satake, N. Yasuda, S. Takagi, and A. Toriumi, Appl. Phys. Lett. **69**, 1128 (1996).
[15] J. D. Bude, B. E. Weir, and P. J. Silverman, Tech. Dig. Int. Electron Devices Meet. **1998**, 179 (1998).

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