An Improved BJT-Based Silicon Retina with Tunable Image Smoothing Capability

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***Abstract*—An improved bipolar junction transistor (BJT) based silicon retina with simple and compact structure is proposed and analyzed. In the proposed structure, the BJT smoothing network, which models the layer of horizontal cells in the vertebrate retina, is implemented by placing enhancement n-channel MOSFET's among the bases of parasitic BJT's existing in a CMOS process to form an unique and compact structure. Thus, the smoothing characteristics can be tuned in a wide range. Moreover, an extra emitter is incorporated with each BJT at the pixel to act as the row switch. This reduces the cell area of the silicon retina and increases the resolution. Using the proposed new structure, an experimental 64 $\times$ 64 BJT-based silicon retina chip has been fabricated by using 0.5-μm CMOS technology. The measurement results on the tunability of the smooth area in the smoothing network as well as the dynamic characteristics of the proposed silicon retina in detecting moving objects have been presented. It is believed that the improved structure is very suitable for the very large scale integration implementation of the retina and its application systems for CMOS smart sensors.**

***Index Terms*—Adaptive smoothing function, BJT-based silicon retina, BJT smoothing network, CMOS smart sensor, tunable smooth area, VLSI.**

I. Introduction

IT IS KNOWN that the retina is the early processing element in the visual nervous system of the vertebrate. It performs the early visual processing in a parallel manner to provide real-time information for the brain to perceive the images of the surrounding world [1]–[3]. Due to the superior processing capability of the retina, many efforts have been devoted to implement the functions of retina in the silicon integrated circuits (IC's) [4]–[9]. To implement the functions of the retina, analog circuits are superior to digital circuits because analog circuits have the advantages of compact structure to perform useful operations, small chip size, and low-power consumption [10]–[15].

Recently, a new silicon retina structure called the bipolar junction transistor (BJT) based silicon retina is proposed [16]–[17]. In the BJT-based silicon retina, the function of the horizontal cells is realized by the BJT smoothing network. The BJT's in the BJT smoothing network are used not only as photoreceptors, but as the smoothing devices. The spatial smoothing function on the images is realized by both carrier transport effect and base resistance bias effect [18]–[20] of the BJT's in the same base region. The structure of the BJT smoothing network is simple and compact. Moreover, it is suitable for the very large scale integration (VLSI) implementation.

As indicated in [21]–[25], the smoothing range of those images with wide-range variations on intensity or contrast is required to be adjustable. In the BJT smoothing network of [16] and [17], the extrinsic base resistance among the active bases of the BJT's can be designed to obtain different image smoothing ranges. However, it cannot be adjusted after fabrication. This limits the applications of the BJT-based silicon retina in smart sensors.

In this paper, the BJT smoothing network with an enhancement-mode n-channel MOSFET inserted between the bases of two parasitic p-n-p BJT's existing in an n-well CMOS process is proposed to increase the tunability of image smoothing ranges. It is shown that the inserted nMOSFET can be operated either in the strong-inversion region or subthreshold region to provide a wide range of resistance values to achieve the wide-range adjustment of smoothing ranges. As compared to the original BJT smoothing network [16], [17], the proposed BJT smoothing network has smaller chip area in realizing the same base resistance and higher tunability of image smoothing ranges.

In the focal-plane array (FPA) of the proposed BJT-based silicon retina, the access circuit of silicon retina cells is realized by using the multiemitter BJT's. Thus, the pixel area can be kept small. A 64 $\times$ 64 experimental chip has been designed and fabricated by using 0.5-μm n-well CMOS technology. The measurement results on both static and dynamic characteristics have verified the correct functions of the proposed BJT-based silicon retina.

In Section II, the structure of the proposed BJT-based silicon retina is described and both static and dynamic operations are also analyzed. In Section III, the FPA architecture of the silicon retina is presented. The experimental results of the 64 $\times$ 64 experimental chip are presented in Section IV. Finally, the conclusion is given.

II. Analyses of the Proposed BJT-Based Silicon Retina

The equivalent circuit of the proposed BJT-based silicon retina is shown in Fig. 1 where $I_{\rm ES}$ is the emitter currents of the smoothing pnp BJT in the BJT smoothing network, $I_{\rm EI}$ is the emitter currents of accompanying isolated pnp BJT's, and $V_{\rm EB}$ is the emitter–base junction voltage of the BJT's. In this structure, each pixel has two parasitic vertical

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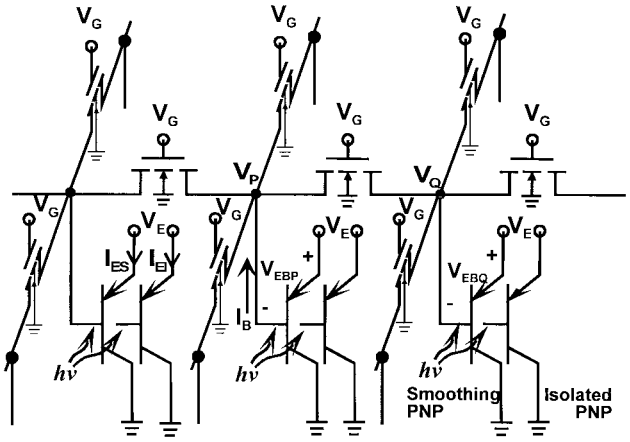


Fig. 1. The equivalent circuit of the proposed two-dimensional (2-D) BJT-based silicon retina.

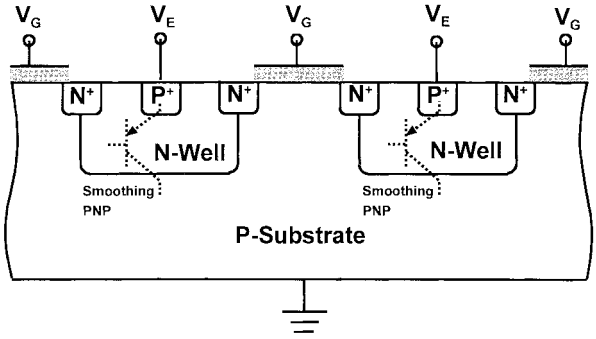


Fig. 2. The cross-sectional view of the BJT smoothing network, which contains one BJT and one enhancement nMOSFET in each pixel.

pnp BJT's existing in the CMOS process. The two BJT's (called isolated BJT and smoothing BJT) have an open base to serve as phototransistors. Moreover, an enhancement-mode n-channel MOSFET is inserted between the active bases of two smoothing BJT's to form the BJT smoothing network. Thus, the smoothing BJT can serve as phototransistor and smoothing device. The cross-sectional view of the two smoothing BJT's and one nMOSFET in the BJT smoothing network is shown in Fig. 2. The tunable conjunction resistance in the BJT smoothing network is efficiently realized by the channel resistance of the inserted nMOSFET's with adjustable common gate bias. As shown in Fig. 2, the n^+ source/drain of the nMOSFET is placed on the boundary of the n-wells, which are base regions of the parasitic pnp BJT's in n-well CMOS technology. This makes the proposed BJT smoothing network quite compact.

The BJT smoothing network is used to realize the smoothing function of the horizontal cells in the retina, whereas the accompanied isolated BJT at each pixel is used to realized the photoreceptor cell in the retina. The role of the BJT smoothing network is to compute the spatially and temporally weighted average of images. When the light is incident upon one pixel, it is simultaneously incident upon the two floating bases of both smoothing BJT and isolated BJT. Thus, electron–hole pairs are generated in and nearby the depletion region of the two base–collector junctions. Due to the electric field in the depletion region, the generated electrons are swept into the

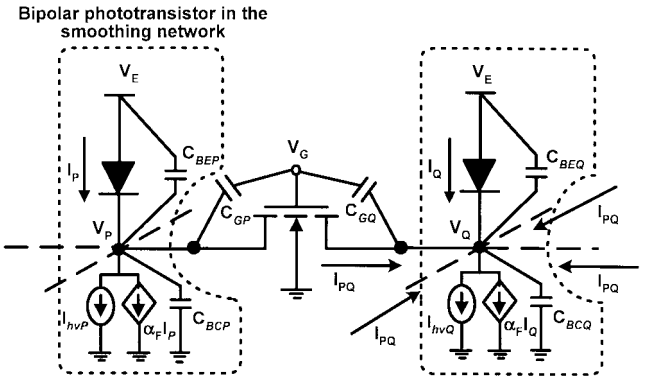


Fig. 3. The large-signal equivalent circuit of the BJT smoothing network in Fig. 1 with device capacitances.

base region, whereas the holes are swept into the collector. The electrons swept into the base region form a transversely flowing photocurrent in the BJT smoothing network. This gives rise to the forward bias of each base–emitter junction and the current on each emitter. Due to the nMOSFET channel resistance, there are voltage drops in the base region of the BJT smoothing network when the photoinduced electron currents flow. This effect makes the forward bias voltages of base–emitter junctions different from one another and, thus, the magnitudes of emitter currents in the BJT smoothing network become a *weighted* distribution function of distance. The BJT smoothing network, therefore, can perform the required spatial smoothing.

The excitatory synapse between the photoreceptor and horizontal cell in the retina is implemented by letting photons simultaneously stimulate the floating bases of both BJT's at each pixel. According to the analog model [4] of the retina, the response of the bipolar cell in the retina is realized by subtracting the emitter current of the BJT in the smoothing network from that of the isolated BJT at the same pixel. Thus, the output current of the silicon retina in Fig. 1 is $I_{\rm EI} - I_{\rm ES}$.

A. Static Characteristics

To model the static characteristics of the BJT smoothing network in Fig. 1, where the bipolar phototransistors are operated in the active region, the Ebers–Moll equivalent circuit of the BJT is used. The resultant large-signal equivalent circuit of the BJT smoothing network is shown in Fig. 3, where the diode D_P (D_Q) represents the emitter–base junction of the BJT, I_P (I_Q) represents its emitter current, α_F is the common-base forward short-circuit current gain, $I_{h\nu}$ represents the photocurrent induced by photons, $C_{\rm BE}$ $(C_{\rm BC})$ is the base–emitter (collector) capacitance of the BJT, C_G is the gate–source (drain) capacitance of the nMOSFET, and V_G (V_P, V_Q) is the gate (drain, source)–substrate voltage of the nMOSFET. If the nMOSFET in Fig. 3 is operated in the subtreshold region, the current I_{PQ} flowing through the nMOSFET is the diffusion current. I_{PQ} can be expressed as [26]

$$I_{PQ} = \frac{W}{L} I_{D0} \exp\left(\frac{V_G}{nV_T}\right)\left[\exp\left(-\frac{V_Q}{V_T}\right) - \exp\left(-\frac{V_P}{V_T}\right)\right] \quad (1)$$

where W/L is the channel width-to-length ratio of the nMOSFET, I_{D0} and n are process-dependant parameters, and V_T is the thermal voltage. The emitter currents I_P and I_Q flowing through D_P and D_Q in Fig. 3, respectively, can be expressed as

$$I_P = I_{E0}\exp\left[\frac{(V_E - V_P)}{V_T}\right] \tag{2}$$

$$I_Q = I_{E0}\exp\left[\frac{(V_E - V_Q)}{V_T}\right] \tag{3}$$

where I_{E0} is the emitter–base reverse saturation current of the BJT and V_E is the emitter voltage. Substituting (2) and (3) into (1) to cancel the terms of V_P and V_Q, we have

$$I_{PQ} = \frac{W}{L}\frac{I_{D0}}{I_{\rm E0}}\exp\left[\frac{\frac{1}{n}V_G - V_E}{V_T}\right](I_Q - I_P). \tag{4}$$

It can be seen from (4) that I_{PQ} is linearly proportional to $(I_Q - I_P)$ with a constant coefficient determined by V_G and V_E.

From the above analyses, it can be seen that the linear resistive network used to model the horizontal cells can be implemented by the proposed compact BJT smoothing network with subthreshold operated nMOSFET's. This is because the emitter–base junction of the BJT provides the nonlinear conductance to cancel the nonlinear conductance of the nMOSFET so that a linear resistive network is formed. This unique combination of the BJT and MOSFET makes the proposed BJT smoothing network simpler than those proposed in [7]–[9].

When $V_G - V_Q$ of the nMOSFET's in Fig. 3 is greater than the threshold voltage, the current flowing through the nMOSFET is the drift current and the improved BJT smoothing network acts as a nonlinear network. It performs the spatially smoothing function through the base resistance bias effect of the BJT's [20]. As derived in [20], the emitter current $I_E(n)$ of the smoothing BJT at the nth pixel in the one-dimensional (1-D) smoothing network under the single-point stimulus can be expressed as

$$\frac{I_E(n)}{I_E(0)} = \frac{\cos^2(z)}{\cos^2\left[z\left(1 - \frac{n}{N}\right)\right]} \tag{5}$$

$$z\tan z = \frac{RN}{2V_T}I_{h\nu}(0) \tag{6}$$

where R is the sum of base resistance and effective channel resistance of the nMOSFET among the active bases of BJT's, N is the total BJT number in the 1-D network, $I_E(0)$ is the output emitter current at the stimulated pixel, and $I_{h\nu}(0)$ is the incident photocurrent. As seen from (5) and (6), the emitter current ratio in (5) and the smoothing function are adjustable if R is adjustable. Since the channel resistance of the nMOSFET is dominant in R, the inserted nMOSFET can be used to adjust R through V_G in order to obtain different smoothing ranges.

Since the base potential difference between two adjacent BJT's in the BJT smoothing network is quite small, the inserted nMOSFET is operated in the linear region when V_G is large. Its channel resistance $R_{\rm DS}$ can be expressed as

$$R_{\rm DS} = \left[\frac{W}{L}\mu_n C_{\rm OX}(V_G - V_E + V_{\rm EB} - V_{\rm th})\right]^{-1} \tag{7}$$

where W/L is the geometric ratio of the nMOSFET, μ_n is the effective electron mobility, $C_{\rm ox}$ is the gate oxide capacitance per unit area, and $V_{\rm th}$ is the threshold voltage under the reverse substrate bias $V_E - V_{\rm EB}$. As may be seen from (7), $R_{\rm DS}$ is tunable by V_G. Thus, the smoothing characteristics of the BJT smoothing network can be adjusted by V_G [20].

It can be seen from the above analyses that the proposed BJT smoothing network can meet the requirement of adjustable image smoothing from local to global, as indicated in [21]–[25]. Moreover, the proposed BJT smoothing network can perform wide-range smoothing functions with small chip area.

When the incident light intensity is increased, the emitter–base junction voltage $V_{\rm EB}$ of the BJT in the proposed BJT smoothing network is increased. If the MOSFET is in the subthreshold region, the effective channel resistance is decreased with the increasing light intensity. However, the effect of decreasing channel resistance can be completely compensated by the increasing base–emitter junction conductance. Thus, I_{PQ} in (4) remains unchanged, and so does the smoothing characteristics.

If the nMOSFET in the smoothing network is operated in the linear region, $R_{\rm DS}$ in (7) is decreased with light intensity increasing. The reduced $R_{\rm DS}$ in the proposed BJT smoothing network leads to more global smoothing and the low-contrast image becomes less visible. This problem also arises in the MOSFET resistive smoothing networks [7]–[9]. However, in the proposed BJT smoothing network, the above-mentioned effect can be compensated.

In the BJT smoothing network of [16] and [17] with an invariant intercell resistance, the smoothing is adaptive. Under brighter background or higher contrast, the BJT smoothing network can be automatically adjusted to achieve a more local smoothing range [20]. This unique performance, which is due to the nonlinear base resistance bias effect, also exists in the proposed BJT smoothing network. When the intensity of light incident on the proposed BJT smoothing network with the nMOSFET's in the linear region is increased, the increase of the smoothing range due to the decreased $R_{\rm DS}$ can be compensated by the reduced smoothing range due to the base resistance bias effect. The resultant smooth area is still decreased due to the stronger base resistance bias effect.

B. Dynamic Characteristics

To characterize the temporally average function of the proposed BJT smoothing network, its large-signal equivalent circuit with device capacitances, as shown in Fig. 3, is considered. This circuit structure is similar to the organization of the horizontal cells in the vertebrate retina, where the node capacitance $C_{\rm BE} + C_{\rm BC} + 4C_G$ is equivalent to the membrane capacitance of horizontal cells, whereas the channel resistance $R_{\rm DS}$ of the nMOSFET is equivalent to the resistance of the gap junction between two horizontal cells.

When a flashlight is incident upon the silicon retina, it takes certain delay time to build up the emitter currents of both the isolated BJT and smoothing BJT due to BJT intrinsic turn-on delay and *RC* components at the base node. In the proposed BJT smoothing network, the delay time t_S is dominated by the *RC* effect in the equivalent circuit of Fig. 3. Assume that under light illumination, the base node voltage V_Q at the incident pixel is decreased from V_{QS} to $V_{QS} - \Delta V_{QS}$. The delay time t_S can be approximately expressed as

$$t_S \approx \frac{(C_{\mathrm{BE}Q} + C_{\mathrm{BC}Q} + 4C_{GQ})\Delta V_{QS}}{I_{h\nu Q} + \alpha_F I_Q - 4I_{PQ} - I_Q} \tag{8}$$

where both capacitances and currents are nonlinear function of node voltages and $4I_{PQ}$ is the total current flowing into the base node from the four neighboring nodes, as shown in Fig. 3. For the dark pixel in the smoothing network, ΔV_{QS} is smaller and $I_{h\nu Q} = 0$. Thus, its t_S is nearly the same as that at the incident pixel.

Similarly, the delay time t_i to build up the emitter current of the isolated BJT incident by light can be approximately expressed as

$$t_i \approx \frac{(C_{\mathrm{BE}} + C_{\mathrm{BC}})\Delta V_i}{I_{h\nu} + \alpha_F I_{Ei} - I_{Ei}} \tag{9}$$

where I_{Ei} is the transient emitter current, ΔV_i is the change of base node voltage, and both capacitances and currents are nonlinear functions of node voltages. Comparing (9) to (8), it can be found that the isolated BJT has a smaller capacitance and a larger current. Thus, t_i is much smaller than t_S. Therefore, the output current $I_{\mathrm{EI}} - I_{\mathrm{ES}}$ of the BJT-based silicon retina has a significant positive pulse when light is incident. Both peak value and pulsewidth are dependent on the size of flashlight. When the size of flashlight is larger, the current I_{PQ} in (8) is smaller due to the spatial smoothing function of the smoothing network. Thus, t_S is smaller, leading to a smaller pulsewidth.

When the light is turned off, the base node voltage is increased to the value in the off state. It is found that the charging current is mainly provided by the BJT itself. Thus, the turn-off times of both smoothing BJT and isolated BJT are nearly the same. Since the base node of the BJT in the BJT smoothing network has an extra capacitance $4C_{GQ}$ as in (8), the turn-off time is slightly larger. Thus, a smaller negative pulse is resulted when the flashlight is turned off.

III. The 2-D Architecture of Silicon Retina

In the design of the FPA of the proposed BJT-based silicon retina, compact row/column selection circuits are required to achieve small pixel area. Fig. 4 shows the basic cell structure of the FPA of BJT-based silicon retina. Both isolated and smoothing BJT's at each pixel have extra emitters directly connected to the row line. Two pMOS devices are connected in series with the active emitters of BJT's to serve as the row switches *SW1* and *SW2* controlled by the row line. Through the switches, the emitter currents can be sent to smoothing and isolated column lines biased at V_E. In each cell, four nMOSFET's are connected from the smoothing BJT to the four

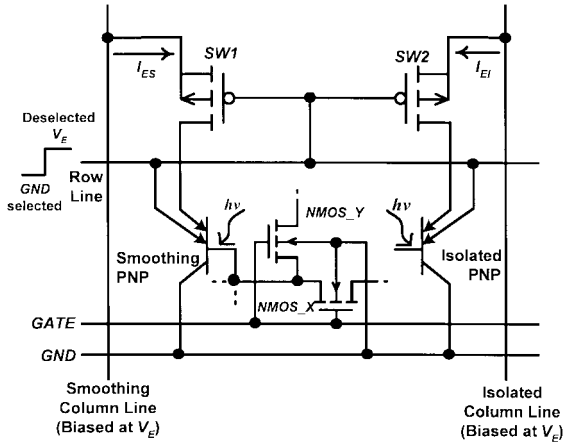


Fig. 4. The basic cell circuit of the FPA of the proposed 2-D BJT-based silicon retina.

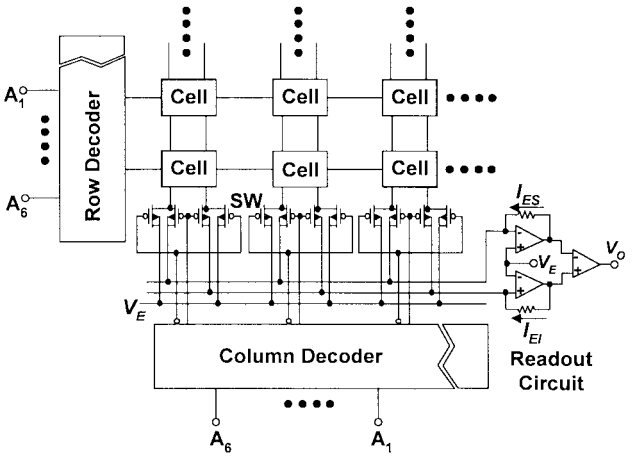


Fig. 5. The complete architecture of the FPA chip of the proposed 2-D BJT-based silicon retina.

neighbors to form the proposed 2-D BJT smoothing network. Equivalently, each cell has two nMOSFET's, as shown in Fig. 4. All the gates of nMOSFET's are connected to the common gate line with the adjustable voltage V_G.

When the row line is selected through the row decoder, its voltage is set at *GND*. The extra emitters act as collectors of pnp BJT's and *SW1* and *SW2* are closed. Thus, the two emitter currents I_{EI} and I_{ES} of isolated and smoothing pnp BJT's at the selected pixel can be sent to the isolated and smoothing column lines, respectively. When the row line is deselected, its voltage is raised to the emitter voltage V_E. In this case, *SW1* and *SW2* are open and the normal emitters of pnp BJT's are disconnected from the column lines and become floating. However, the extra emitters connected to the row selection line are connected to V_E. With all the deselected emitters of BJT's connected to V_E, the BJT's in the smoothing network can be kept in the normal state so that the normal smoothing operation can be performed.

The complete FPA architecture of the proposed BJT-based silicon retina is shown in Fig. 5. As may be seen from Fig. 5, each column line has two pMOS devices as the column switches controlled by the column decoder. When the column

TABLE I
THE SUMMARY ON THE CHARACTERISTICS OF THE FABRICATED FPA CHIP OF BJT-BASED SILICON RETINA

Technology	0.5μm N-well CMOS Double Poly Double Metal
Resolution	64 × 64
Sampling geometry	Rectangular
Pixel size	45μm × 45μm
Size of the bipolar phototransistors	3.3μm × 2.2μm (emitter), 15μm × 34μm (base)
W/L of the inserted nMOSFET among smoothing BJTs	3μm/6μm
Fill factor (size of the light window)	0.49 (29.5μm × 34μm)
Chip size	4mm × 4mm
Power supply	3V, 5V
Total quiescent power dissipation	45mW
Active power dissipation of the sensor array in the illuminated state	3mW ~ 30mW (Depending on image light intensity)
Current gain of BJTs	4.8
Settling time of the BJT smoothing network	1ms
Readout time of one pixel	16μs
Frame rate for column parallel readout	9.6 kHz

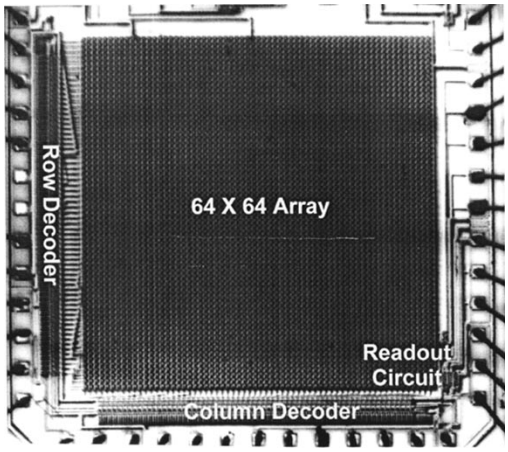


Fig. 6. The chip photograph of the fabricated 64 × 64 FPA of BJT-based silicon retina.

is selected, one pair of switches are closed to connect both isolated and smoothing column lines to the readout circuit. When the column is deselected, the other pair of switches is closed to connect both column lines to V_E. Thus, all emitters in the deselected columns can be biased at V_E.

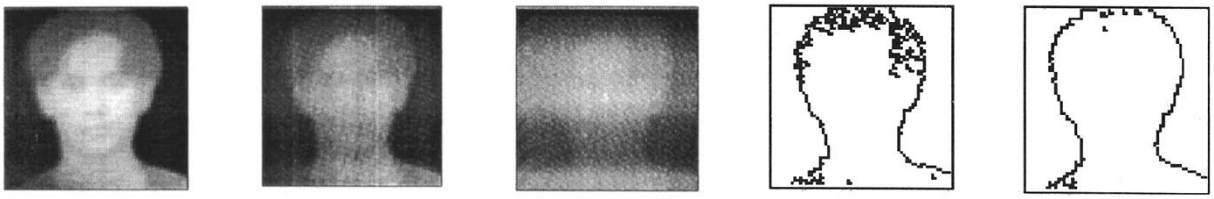
As shown in Fig. 5, the readout circuit is used at the output to sense both emitter currents $I_{\rm EI}$ and $I_{\rm ES}$ and convert them into voltages. The subtraction of the two voltages is then performed to obtain the output voltage V_o, which represents the response of the bipolar cell in the retina.

IV. EXPERIMENTAL RESULTS

An experimental chip of the proposed BJT-based silicon retina is designed and fabricated by using 0.5-μm n-well double-poly double-metal CMOS technology. Fig. 6 shows the chip photograph of the fabricated 64 × 64 FPA of the BJT-based silicon retina. In the quiescent state without image inputs, the power dissipation of the sensor array in the silicon retina is very small, being that of 64 × 64 open-base BJT's. Thus, the total quiescent power dissipation is determined by the peripheral circuit, which is about 45 mW. In the illuminated state, the power dissipation of the sensor array is caused by the photocurrents of the BJT's, which depends on the image light intensity. The typical total active power dissipation of the silicon retina FPA in the illuminated state is about 3–30 mW. The characteristics of the fabricated FPA chip of BJT-based silicon retina are summarized in Table I.

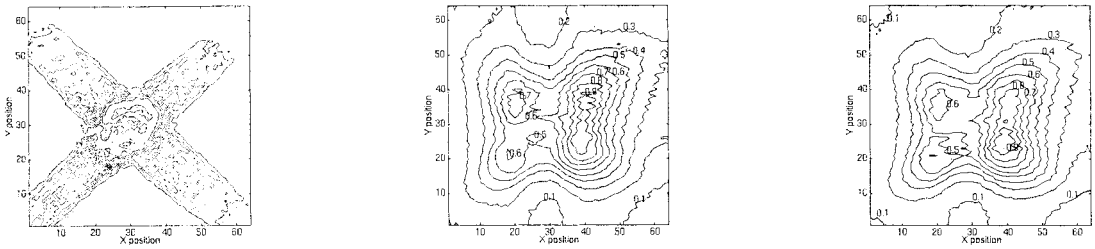
To verify the tunable smoothing function of the proposed BJT smoothing network, an image is projected on the experimental chip with the gate bias V_G of nMOSFET's tuned at different values. Fig. 7(a) shows the measured output responses of the isolated BJT's. These responses represent those of the photoreceptors in the retina. Fig. 7(b) and (c) shows the measured output responses of the BJT's in the BJT smoothing network with V_G at 3.75 and 4.0 V, respectively. These responses represent those of the horizontal cells in the retina. Fig. 7(d) and (e) shows the mathematically found zero crossing positions of the outputs of the BJT-based silicon retina. The zero-crossing points of the measured output signals of the BJT-based silicon retina can be used to identify the edges of objects [24], [25], and [27]. As shown in Fig. 7(d) and (e), when the smooth area is smaller, the smaller variation of light intensity can be identified. In other words, the edges with smaller contrast can be identified.

Fig. 8 shows the measurement results on the unique adaptive characteristics of the proposed BJT-silicon retina, as mentioned in Section II-A. It can be seen that the smooth area of the BJT smoothing network under brighter background, as shown in Fig. 8(c), is smaller than that under darker background, as shown in Fig. 8(b). Moreover, the effect of the



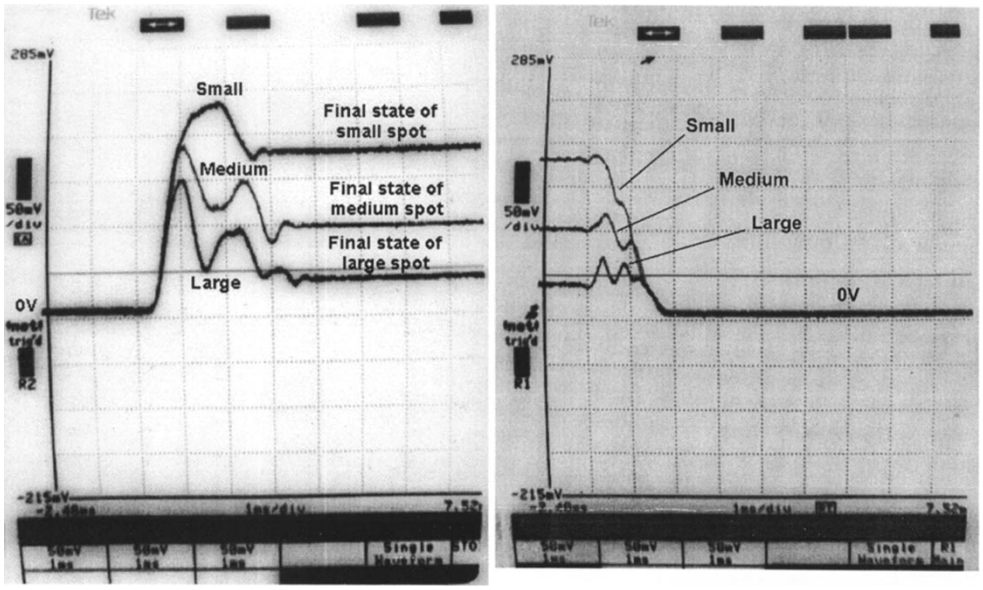
(a) (b) (c) (d) (e)

Fig. 7. The measured output responses of (a) isolated BJT array, (b) BJT smoothing network with $V_G = 3.75$ V, and (c) BJT smoothing network with $V_G = 4.0$ V in the fabricated FPA chip of BJT-based silicon retina exposed to an image. The mathematically found zero-crossing positions of the measured output responses of the BJT-based silicon retina are shown in (d) for (b), and (e) for (c). In (a), (b), and (c), the 256 gray levels are used to divide the current range of (a) 0–0.2 μA, (b) 0–0.165 μA, and (c) 0–0.12 μA, respectively.



(a) (b) (c)

Fig. 8. The normalized contour plots of the measurement emitter currents of the BJT smoothing network for an (a) original image under (b) darker background and (c) brighter background, where the contrast of input pattern is kept the same and the gate bias of nMOSFET's is 3.9 V.



(a) (b)

Fig. 9. The measured output (a) turn-on and (b) turn-off temporal responses of a single pixel in the improved 2-D BJT-based silicon retina under different incident flashlight patterns with the same intensity and different sizes.

decreasing channel resistance of nMOSFET's on the increase of smooth area does not appear in the measurement results, as predicted in Section II-A.

Fig. 9(a) and (b) shows the measured output temporal responses of a single pixel in the fabricated FPA chip of the BJT-based silicon retina under three flashlight spot patterns with nearly the same intensity, but different spot diameters. It can be seen in Fig. 9(a) that the positive pulse is generated when the flashlight is incident. The pulse has higher peak for a smaller flash spot. This is consistent with the analyses in Section II-B.

When the light is turned off, the measured output temporal responses of the fabricated silicon retina decays to the off state, as shown in Fig. 9(b). The small negative pulse is not observed because the large off transition time of the flashlight allows both isolated and smoothing BJT turned off simultaneously. The peaks in Fig. 9(b) are induced by the closing time of the mechanical shutter used in this measurement.

Fig. 10 shows the measured output responses of a single pixel in the fabricated FPA chip of the BJT-based silicon retina with a moving light bar projected upon the chip. During the periods of $T1$ and $T2$, indicated in Fig. 10, the light bar is

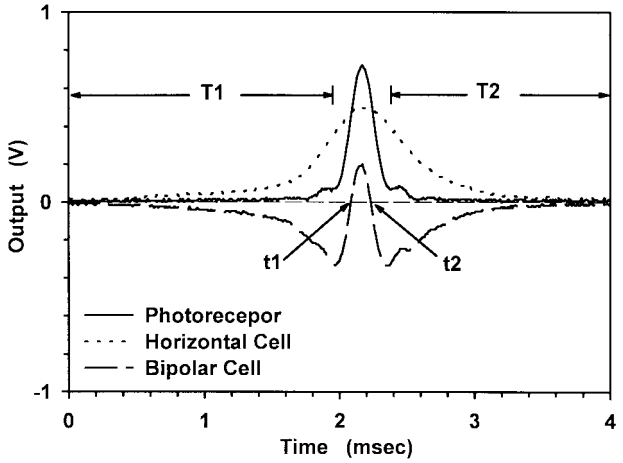


Fig. 10. The measured output responses of a single pixel in the 2-D BJT-based silicon retina under a moving light bar incident upon the chip.

not incident on the readout pixel. Therefore, there are very small output responses in the isolated BJT due to the diffracted light. However, the response of the BJT in the smoothing network is gradually increased as the light bar is approaching and decreased as the light bar is leaving. This is caused by the spatial smoothing function of the BJT smoothing network. When the light bar is projected upon the readout pixel, the isolated BJT has a larger response than the smoothing BJT. The difference of these two responses, as generated by the silicon retina shown in Fig. 10, involve negative and positive pulses as the light bar is approaching and positive and negative pulses as the light bar is leaving. The zero-crossing points occurs at $t1$ and $t2$. These zero-crossing characteristics caused by the passing of the edge of object can be applied to the detection of velocity and direction of moving objects [28].

In the FPA chip of the BJT-based silicon retina, the current gain β of BJT's is not completely matched due to process variations. One of the dominant factors for β mismatch is the base width. Since the parasitic p-n-p BJT's in n-well CMOS process has a wide base width, this leads to a low β of 4.8 and a low β mismatch. The measured global β variations are 6% on the same wafer, 4% in the same chip, and 0.1% at the same pixel. In the FPA of BJT-based silicon retina, the current difference of two bipolar phototransistors are taken as the output signal. Using the output current difference to perform edge detection or moving object detection, only the pixels near the edge are involved. Under good local matching error of 0.1%, it is found that the detection capability is not affected by this small β variations. Moreover, under uniform light illumination, the 4% β variation across the chip in the BJT smoothing network can be smoothed so that the resultant zero-crossing error signals are quite small. They can be cleared out by zero-crossing detectors [29]. Thus, the β variation has negligible effects on the performance of the proposed BJT-based silicon retina.

V. Conclusion

A CMOS 64 × 64 FPA of BJT-based silicon retina with simple structure and tunable smoothing characteristics has been designed, analyzed, and fabricated by using 0.5-μm n-well double-poly double-metal CMOS technology. In the proposed BJT-based silicon retina structure, nMOSFET's are merged among the BJT's in the BJT smoothing network to make the smooth area tunable through the adjustable channel resistance controlled by the gate voltage. Moreover, the multiemitter structure is used to simplify the row selection circuit. Both simulation results and experimental results of static and dynamic performance of the proposed structure have been presented. Further research will be conducted in the applications of the proposed BJT-based silicon retina to the detection of velocity and direction of moving objects [28].

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