A 2-V, 1.8-GHz BJT Phase-Locked Loop

Wei-Zen Chen and Jieh-Tsorng Wu, *Member, IEEE*

***Abstract*— This paper describes the design of a bipolar junction transistor phase-locked loop (PLL) for $\Sigma\Delta$ fractional-N frequency-synthesis applications. Implemented in a 0.8-μm BiCMOS technology, the PLL can operate up to 1.8 GHz while consuming 225 mW of power from a single -2-V supply. The entire LC-tuned negative-resistance variable-frequency oscillator is integrated on the same chip. A differential low-voltage current-mode logic circuit configuration is used in most of the PLL's functional blocks to minimize phase jitter and achieve low-voltage operation. The multimodulus frequency divider is designed to support multibit digital modulation. The new phase and frequency detector and loop filter contain only npn transistors and resistors and thus achieve excellent resolution in phase comparison. When phase locked to a 53.4-MHz reference clock, the measured phase noise of the 1.6-GHz output is -91 dBc/Hz at 10-kHz offset. The frequency switching time from 1.677 to 1.797 GHz is 150 μs. Die size is 4300 × 4000 μm^2, including the passive loop filter.**

***Index Terms*— Fractional-N, frequency synthesis, low-voltage current-mode logic (LVCML), phase-locked loop.**

I. Introduction

In radio-frequency wireless transceivers, frequency synthesizers based on the phase-locked loop (PLL) architectures are often used as local oscillators for up and down frequency conversion. PLL's are suitable for monolithic integration and thus can be of small size, of low cost, and power thrifty. Basic functional blocks of PLL's for frequency-synthesis applications include a phase detector, loop filter, variable-frequency oscillator (VFO), and frequency divider. By varying the divide ratio of the frequency divider, the PLL can synthesize a new frequency based upon the reference input while retaining the stability, accuracy, and spectral purity of the original reference.

Major design considerations are channel frequency spacing, frequency switching time, and phase noise. A small frequency spacing dictates the use of a loop filter with a narrow bandwidth, resulting in slow frequency switching time. Since the VFO's phase noise at frequencies outside the loop bandwidth cannot be suppressed by the loop's feedback mechanism, a PLL with a narrow loop bandwidth also requires its VFO to have low free-running phase noise. In addition, the loop filter must exhibit little noise and have good immunity against outside disturbance.

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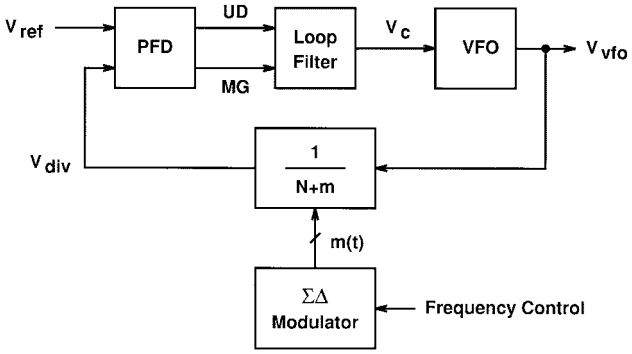

Fig. 1. A $\Sigma\Delta$ fractional-N phase-locked loop.

The severe tradeoff between the channel frequency spacing and frequency switching time can be mitigated by using $\Sigma\Delta$ fractional-N PLL's [1]–[4]. As shown in Fig. 1, the digital $\Sigma\Delta$ modulator generates a stream of integers $m(t)$ that can interpolate a fractional number corresponding to the frequency control input. Most of the quantization noise arising from the interpolation can be deployed outside the frequency band of interest so that it can be removed by the PLL's loop filter. The divide ratio of the multimodulus frequency divider (MMFD) is controlled by $m(t)$, and the ratio can be expressed as $N+\overline{m(t)}$. The high resolution of the averaged divide ratio $N+\overline{m(t)}$ permits the use of a higher input frequency and wider loop bandwidth while maintaining channel frequency spacing.

Fully integrated radio-frequency PLL's in CMOS technology have been reported in recent years [7], [8]. Since large voltage swing is required for many of the CMOS digital circuits to operate, it can be difficult to isolate the PLL's sensitive functional blocks from being polluted by the coupled noise. On the other hand, the bipolar junction transistor (BJT) current-mode logic has better input sensitivity, requires only a small voltage swing, and generates little noise.

This paper describes the design of a fully integrated, low-voltage BJT PLL for $\Sigma\Delta$ fractional-N frequency-synthesis applications [5]. The architecture of the PLL is shown in Fig. 1. All functional blocks except the digital $\Sigma\Delta$ modulator have been integrated in a single chip. The PLL contains an MMFD that supports multibit modulation [1], [4]. The frequency tuning of the VFO is accomplished by using a variable-impedance converter [9], [10], so that low-voltage operation as well as monolithic integration become possible. The PLL has a relatively wide loop bandwidth to enable agile frequency hopping. In this case, the phase jitter in the MMFD and the phase and frequency detector (PFD) must be minimized. Fully differential low-voltage current-mode circuit configurations are applied to most of the PLL's circuit blocks.

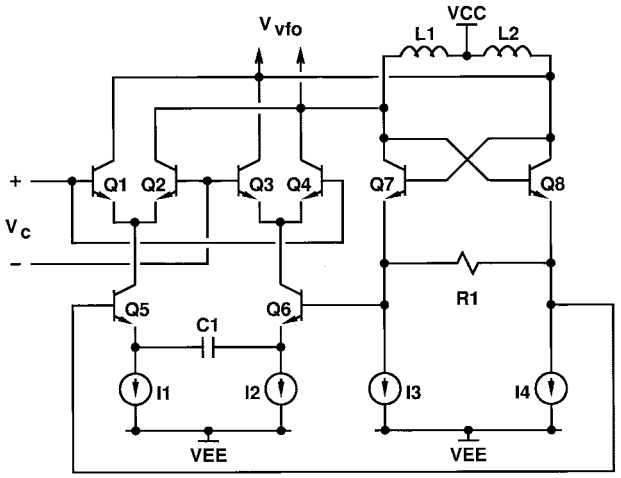

Fig. 2. VFO circuit schematics.

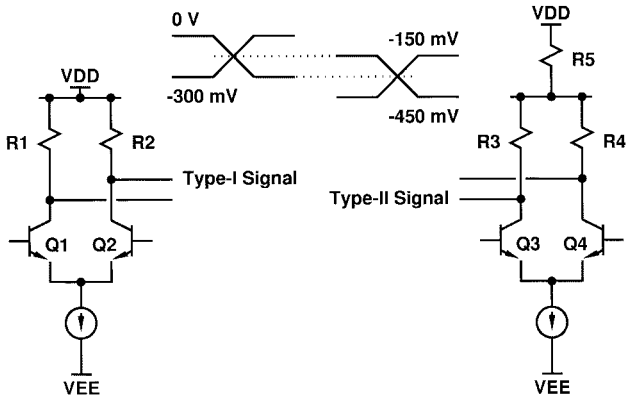

Fig. 3. LVCML circuit schematic.

The bipolar transistors are well suited for low-jitter current-mode operation due to their high transconductance and low flicker noise. Each circuit block in the PLL is designed with objectives of high speed and low noise to obtain good phase-noise performance. The PFD and the loop filter are designed in such a way that only npn transistors and resistors are used to achieve high resolution in phase comparison. In addition, the pole and the zero of the loop filter are generated separately so that the integration capacitor can be reduced.

This paper is organized as follows. Section II is a brief overview of the VFO circuit architecture and its operation principles. Section III discusses a fully differential low-voltage current-mode logic whose circuit configuration is used in MMFD's, PFD's, and loop filters. Section IV describes the architecture and detailed schematic of the MMFD. Section V describes the design of the PFD and the loop filter. Experimental results are presented in Section VI. Last, conclusions are given in Section VII.

II. Variable-Frequency Oscillator

The VFO circuit schematic is shown in Fig. 2 [9], [10]. This circuit is based on the principle of LC-tuned negative-resistance oscillators. Frequency tuning of the VFO is accomplished by using a variable-impedance converter (VIC) to simulate the function of a varactor. The VIC varactor consists of transistors Q1–Q6 and capacitor C1. The Q5–Q6 emitter-coupled pair degenerated by the C1 capacitor produces a phase-shifted differential collector current in response to the $V_{\rm vfo}$ variation. This differential current then passes through the Q1–Q4 current switch and becomes the capacitive loading of the differential $V_{\rm vfo}$ nodes. The differential voltage V_c determines the equivalent capacitance of the VIC varactor and thus controls the oscillation frequency of the VFO.

Compared with the pn-junction varactors' tuning schemes [11], [12], this VIC tuning technique is more suitable for low-voltage operation, and at the same time can provide a wide tuning range to cover both the process and temperature variations. Unlike the pn-junction varactors, whose control inputs are single ended and susceptible to noise coupling, the control input V_c of the VIC is fully differential and can reject common-mode noise. The frequency-dependent phase shift along the VIC signal path can affect the equivalent quality factor of the VFO's resonator [9]. When $V_c > 0$, the input admittance of the VIC exhibits a negative real part, which can increase the quality factor of the resonator. The capacitive tuning range of the VIC could be widened at the expense of higher power consumption [9]. The active devices in the VIC introduce additional noise sources, thus degrading the free-running phase noise of the VFO. However, the phase noise near the carrier frequency can be suppressed by the PLL if the loop gain and bandwidth are enough.

Transistors Q7–Q8 and resistor R1 are configured as a negative impedance converter, providing the negative resistance necessary to sustain oscillation. They also function as the voltage level shifter for the VIC. The oscillating amplitude of $V_{\rm vfo}$ is eventually clamped by the collector junctions of Q7 and Q8. The redundant energy generated by the negative impedance converter is absorbed by the extra energy loss due to forward biasing of the collector junctions.

The minimum supply voltage for the VFO is $V_{\rm BE(on)}$ of Q5–Q6 plus $V_{\rm BE(on)}$ of Q7–Q8 plus $V_{\rm BC(on)}/2$ of Q7–Q8, which is approximately 2 V at room temperature. It has been experimentally demonstrated that the VFO can still operate even in the low-voltage cases in which the two current sources in the VIC, I1 and I2, are temporarily forced into the operation regions where the output currents are no longer constant.

III. Low-Voltage BJT Current-Mode Logic

Both the PFD and the frequency divider of the PLL are realized using the low-voltage BJT current-mode logic (LVCML) shown in Fig. 3 [13].

The Type-I and Type-II signals have an identical differential voltage swing of 300 mV and a common-mode voltage difference of one-half of the differential voltage swing. A D-latch example using the LVCML is shown in Fig. 4. The CK is a Type-I signal, while both D input and Q output are Type-II signals. The input data are latched on the rising edge of the CK signal.

The LVCML has poor output driving capability because no effective output buffer can be used. This drawback causes no difficulty in this PLL application, however, since most circuit blocks have low fanouts.

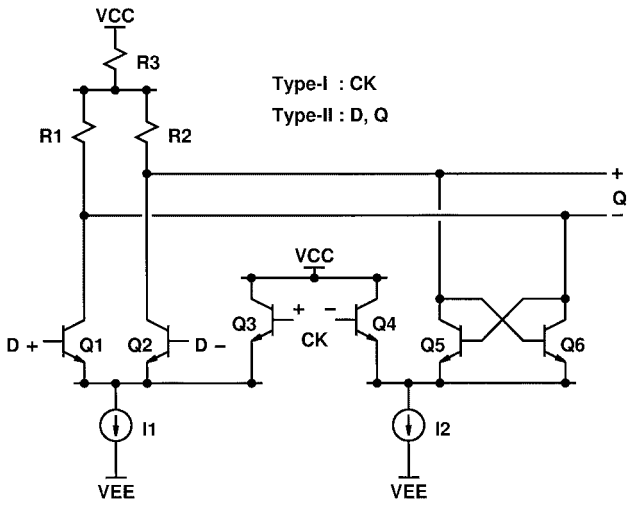

Fig. 4. An LVCML D-latch circuit schematic.

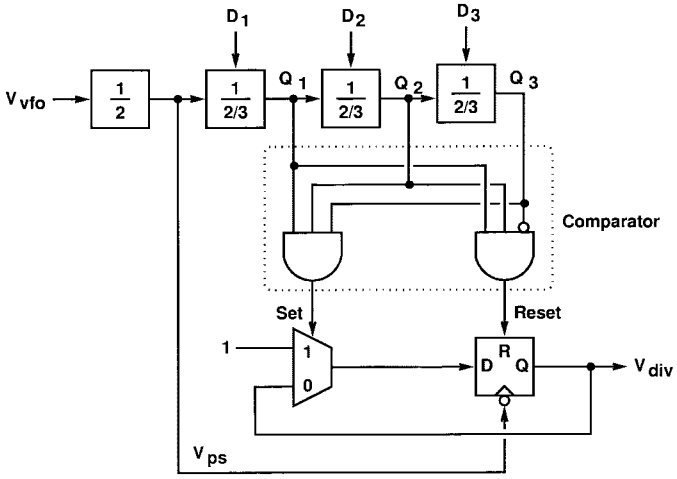

Fig. 5. MMFD block diagram.

IV. Multimodulus Frequency Divider

Fig. 5 shows the block diagram of the MMFD, which consists of an asynchronous counter and a resynchronizer. The asynchronous counter is a cascade of a divide-by-two prescaler followed by three stages of divide-by-two/three dividers. To reduce power consumption, the currents in circuit blocks that can operate at slower speed are scaled down. The phase jitter accumulated in the asynchronous counter is eliminated by the resynchronizer, which consists of a comparator, a multiplexer, and a resettable flip-flop. After resynchronization, the phase jitter in $V_{\rm div}$ is affected by the prescaler and the resettable flip-flop only.

The operation of the resynchronizer is explained as follows. The set signal is activated when the divider's outputs $Q_1Q_2Q_3$ become 111. The multiplexer selects the "1" input, and the output $V_{\rm div}$ rises to one at the falling edge of $V_{\rm ps}$. The output $V_{\rm div}$ will remain one until the flip-flop is reset from the asynchronous reset input. The reset signal is activated when $Q_1Q_2Q_3$ becomes 110. Once $V_{\rm div}$ becomes zero, it will remain zero until $Q_1Q_2Q_3$ is 111 again. The PFD takes only the rising edge of the $V_{\rm div}$ for phase comparison.

A more detailed schematic of the divide-by-two/three dividers is shown in Fig. 6. Each divider stage consists of a divide-by-two A flip-flop, a phase-shift B flip-flop, and a strobe C flip-flop [14]. The *Out* signal is used to strobe C flip-flops, such that the modulus-control inputs $D_1D_2D_3$ are loaded simultaneously at the end of each divide cycle. For each divider stage, if the modulus-control input D_i is low, the phase-shift B flip-flop is disabled, and the A flip-flop functions as a straight divide-by-two divider. When the input D_i is high, the A flip-flop output retains one extra clock cycle by the B flip-flop. The extra cycle (swallowing a single clock period) makes the A flip-flop function as a divide-by-three divider. The activated output of the B flip-flop is then used to reset the C flip-flop, such that the A flip-flop perform the divide-by-three function only once and return to the divide-by-two mode for other clock cycles. Therefore, the overall divide ratio of the MMFD can be expressed as

$$N = D_1 \cdot 2^1 + D_2 \cdot 2^2 + D_3 \cdot 2^3 + 2^4. \tag{1}$$

The divide ratio N can be varied from 16 to 30 with a minimum increment of two.

V. PFD and Loop Filter

The PFD circuit schematic is shown in Fig. 7. The two D-type flip-flops and the AND gate form a classical sequential PFD that generate the UP and DN signals. Instead of using the UP and DN signals to drive the following loop filter directly, an XOR and a delay are added to generate the UD and MG signals. The delay cell in the UD path is used to match the delay of the XOR gate. The UD signal represents the polarity of the phase difference between the two inputs, while the MG signal represents the magnitude of the phase difference.

The loop filter consists of a pole generator and a zero generator, The schematic of the pole generator is shown in Fig. 8, which basically is an integrator. To drive this circuit, the MG input needs to be a type-I signal, and the UD input a type-II signal. When the MG input is high, the I_2 current is bypassed to $V_{\rm CC}$ and the I_1 current is integrated on the capacitor C_f to generate the V_f differential output. The polarity of integration depends on the UD input. When the MG input is low, the I_1 current is bypassed to $V_{\rm CC}$ and the I_2 current is equally divided and enters the V_f differential nodes separately. If $I_1 = I_2$, then the common-mode voltage of V_f can remain unchanged regardless of the states of the MG and UD inputs. The Q7–Q8 cross-coupled pair degenerated by the resistor R4 is a negative-impedance converter (NIC) that generates a negative resistor to cancel the resistive loading effects of R1 and R2. Any mismatch between the negative resistor and R1 + R2 can deviate the pole from $s = 0$.

The schematic of the zero generator and a predistorter is shown in Fig. 9. The predistorter is a low-voltage translinear circuit that can be used to linearize the transfer characteristic of the VFO [9]. The differential signal V_f from the pole generator causes a linear change in the differential collector currents of the Q9–Q10 pair, I_{C9}–I_{C10}. Assuming that diodes D1 and D2 are designed to be always forwarded biased, it can be shown that the VFO's oscillation frequency is linearly related to this

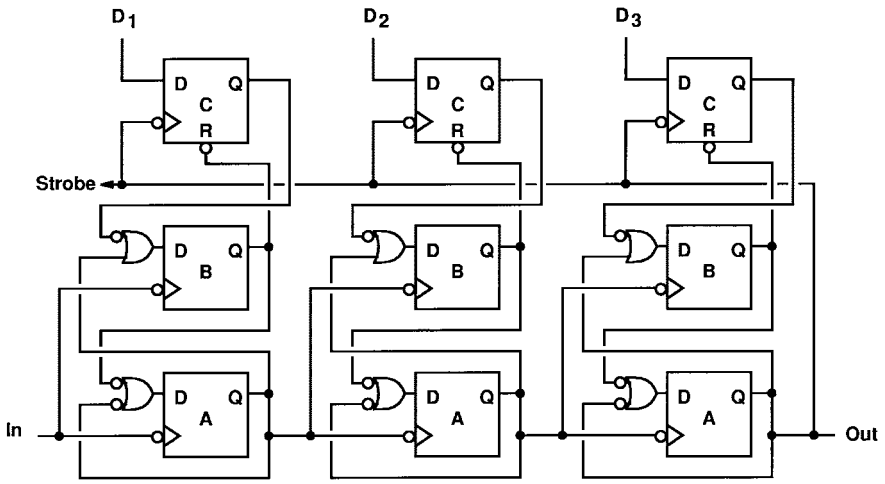

Fig. 6. Divide-by-two/three frequency divider block diagram.

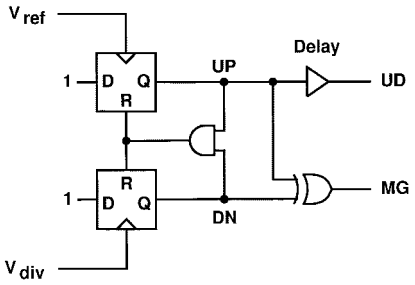

Fig. 7. PFD schematic.

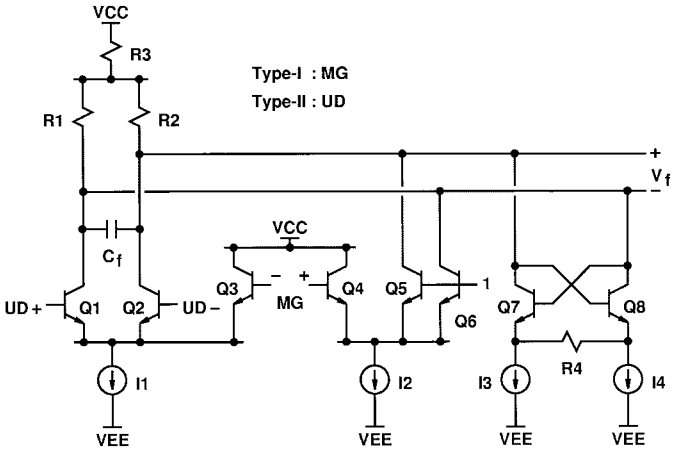

Fig. 8. Pole-generator circuit schematic.

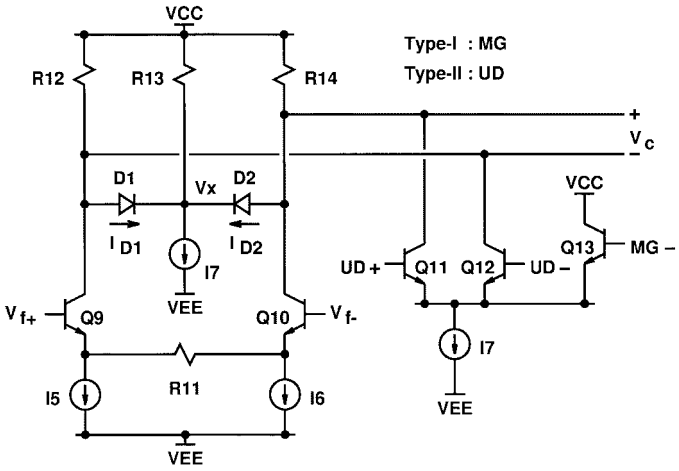

Fig. 9. Zero-generator circuit schematic.

differential current if the V_c output drives the VFO directly [9]. The zero of the loop filter can be easily generated by attaching the Q11–Q13 current switch to the predistorter, as shown in Fig. 9. The current switch is driven by a type-I MG signal and a type-II UD signal. When MG is high, the differential current from the Q11–Q12 pair is added to the V_c output nodes.

A linear model for the PLL is shown in Fig. 10. In the loop filter's pole generator, the phase difference at the PFD output θ_e is converted into a charge-pump current $I_1/2$, where I_1 is the output current of the current source I1 shown in Fig. 8. With the help of the translinear predistorter, the voltage on the C_f integration capacitor, V_f, controls the VFO's oscillating frequency with a linear conversion gain of K_c. The conversion gain is defined with a unit of hertz/volts. The resistor R_m represents the mismatch between the NIC's negative resistor and R1 + R2 in the pole generator. In Fig. 10, the zero generator is modeled with a V_z voltage generated by a charge-pump current I_7 and a resistor R_{11}, where I_7 is the output current of the current source I7 shown in Fig. 9 and R_{11} is the degeneration resistor in the predistorter. The natural frequency of this second-order loop, ω_n, can then be expressed as

$$\omega_n = \sqrt{\frac{K_c}{N} \times \frac{1}{2} \frac{I_1}{C_f} \left(1 + 2\frac{I_7 R_{11}}{I_1 R_m}\right)}. \tag{2}$$

The damping factor of the loop, ζ, is

$$\zeta = \frac{1}{2\omega_n} \times \frac{1}{C_f R_m} + \frac{1}{2N} \times \frac{K_c I_7 R_{11}}{\omega_n}. \tag{3}$$

In nominal cases, we have $I_7 R_{11} \ll I_1 R_m$ and $1/(C_f R_m) \ll \omega_n$; then the ω_n depends only on the conversion gain K_c divided by N and the charge-pump current I_1 divided by the integration capacitance C_f. Once the value of ω_n is determined, the damping factor ζ can be independently selected by choosing a proper value $I_7 R_{11}$. One advantage of this

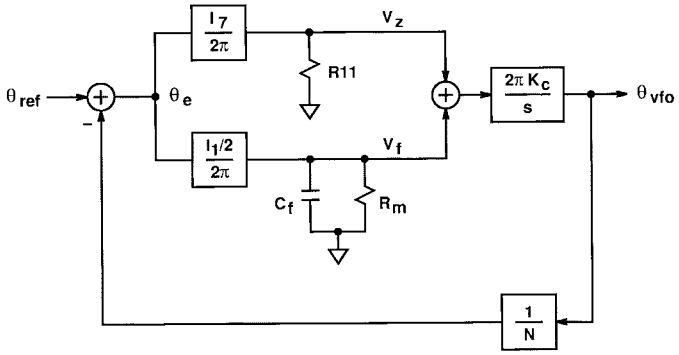

Fig. 10. PLL linear model.

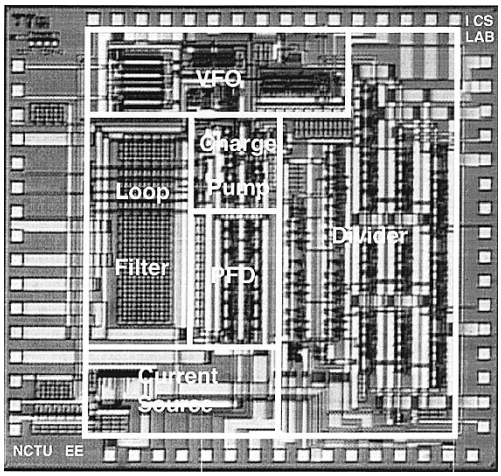

Fig. 11. Chip micrograph of the PLL.

architecture is that it permits the use of smaller C_f. This is because the charge-pump current I_1 can be reduced without affecting the damping factor if ω_n remains unchanged. Since the mismatch resistor R_m moves the loop filter's pole from dc to $1/R_mC_f$, resulting in a finite dc loop gain and reducing the effectiveness of phase-noise suppression near the carrier frequency, it is desirable to have a large value of R_mC_f.

VI. Experimental Results

An experimental PLL chip has been fabricated using a 0.8-μm, 12-GHz f_T BiCMOS technology. The chip micrograph of the PLL is shown in Fig. 11. The chip size is 4300 $\times$ 4000 μm^2. The L1 and L2 inductors in the VFO are realized using bonding wires so that they can be varied to operate at different frequency ranges. For the following measurements, the inductances for both L1 and L2 are approximately 5 nH. The integration capacitor C_f in the charge pump is implemented using the poly-to-poly capacitor. It has a capacitance of 700 pF. The chip is attached directly to a testing circuit board without using any package. Operating from a single 2-V supply, the total power consumption is 225 mW, of which 30 mW is used by the VFO, 40 mW by the output buffer for driving a 50-Ω load, and 100 mW by the MMFD. The PLL can deliver 0-dBm output power to a 50-Ω differential load.

The VFO's frequency tuning range is measured from 1.55 to 2.02 GHz [9]. It has a conversion gain of $K_c = 390$ MHz/V.

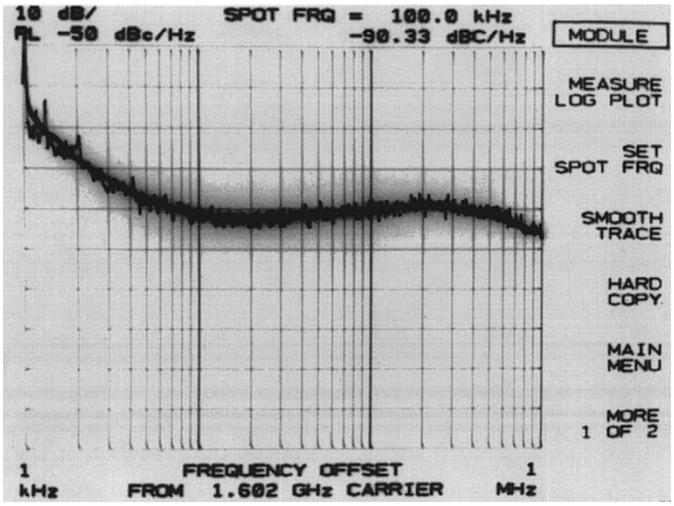

Fig. 12. Measured VFO output phase noise at 1.6 GHz.

However, the maximum operating frequency of the MMFD is only 1.8 GHz. From (2) and (3), with $N = 30$, $I_1 = 0.8$ mA, $C_f = 700$ pF, $I_7 = 0.2$ mA, and $R_{11} = 1$ kΩ, the PLL has a natural frequency $f_n = \omega_n/2\pi = 450$ kHz and a damping factor $\zeta = 0.5$. When the PLL is phase locked to a 53.4-MHz external reference, the measured phase noise of the 1.6-GHz output is shown in Fig. 12. The phase noise is $-$90.3 dBc/Hz at 10-kHz offset. The in-band phase noise is relatively flat between 10 and 400 kHz offset. The relatively high phase noise may be attributed to the noise in the loop filter and ill-designed input buffer for the PFD inputs.

The PLL frequency switching time has also been measured. Using a 59.9-MHz reference and alternating the divide ratio of the frequency divider between 28 and 30, the PLL output frequency can be switched 120 MHz between 1.677 and 1.797 GHz. The measured 10–90% rise/fall time is 10 μs; and the settling time within 100 Hz of final frequency is 150 μs.

VII. Conclusions

This paper describes the design of a fully integrated, low-voltage BJT phase-locked loop for $\Sigma\Delta$ fractional-N frequency-synthesis applications. To achieve fast frequency switching time, the PLL has a relatively wide bandwidth. Therefore, the jitter in the frequency divider and phase-frequency detector must be minimized.

To support monolithic integration, the frequency tuning of the VFO is accomplished by using a variable-impedance converter circuit to emulate the varactor function. The new VFO can achieve a wide frequency tuning range under a supply voltage below 2 V and is immune to common-mode noise due to its fully differential frequency-control input.

The circuit configuration of the low-voltage current-mode logic has been applied to a frequency divider and phase-frequency detector, as well as to a loop filter. To support multibit digital control input, the multimodulus frequency divider uses an architecture that swallows a clock only once in each divide cycle and reload the inputs only at the end of each divide cycle. The use of the resynchronization technique allowed the MMFD to have a jitter performance comparable

to that of a synchronous counter, while its power consumption was similar to that of an asynchronous counter.

The PFD and the loop filter are also implemented in current-mode circuit configuration, and use only npn transistors and resistors. Therefore, excellent resolution in phase comparison can be achieved. Without using the complementary devices, the PLL's dc loop gain can be enhanced with a negative-impedance converter. By separating the pole and zero generation in the loop filter design, the natural frequency and damping factor of the PLL can be optimized separately, resulting in a smaller integration capacitor for pole generation.

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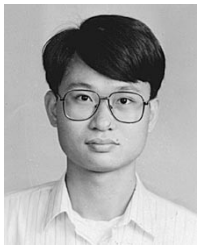

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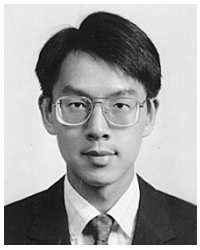

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