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The Leakage Current Effect of Thin Gate Oxides (2.4-2.7 nm) with In Situ Native Oxide Desorption

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An intrinsic defect may exist in thin gate oxides. Such a defect can increase the leakage current in a manner similar to stress-induced leakage current. In this paper, we have shown that the effect of this intrinsic defect can be greatly reduced by in situ removal of the native oxide followed by growing a high-quality thermal oxide. By using such in situ cleaning, ultrathin oxides can be prepared with atomically smooth interfaces, good thickness uniformity, and reduced leakage currents.
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The gate dielectric has become one of the most difficult challenges for future device scaling.[1-7] As metal-oxide semiconductor field effect transister (MOSFET) oxide thickness is reduced, oxide integrity becomes an important issue due to increased direct-tunneling current density and applied electric field. Both intrinsic traps[1] and soft breakdown[2] are observed that increase leakage current in ultrathin oxides and limit reliability, respectively. Although the detailed mechanisms to cause these degraded performances are still not well understood, the presence of native oxide has been reported to cause an oxide reliability problem, and an ultradry process is developed to reduce the native oxide.[8] Unfortunately, native oxide is unavoidable in conventional furnace oxidation due to oxygen and moisture in the air, and this problem becomes more serious as the oxide thickness is scaled down and the ratio of native oxide to total oxide becomes large. Recently, we developed a H_2 bake process to remove native oxide in situ, prior to thermal oxidation, and achieved atomically smooth oxide and Si interface and mobility enhancement over a large applied area.[9] In this paper we discuss the effect of native oxide on leakage current. We have found that the presence of residual native oxide can strongly increase the leakage current at low electric field. In addition, this leakage current is also strongly dependent on the various native oxide formation processes. Native oxide formed in deionized water and 80°C hydrogen peroxide (H_2O_2) shows a higher leakage current at low electric field than that left in air.

Experimental

Figure 1 schematically illustrates our leak-tight, low-pressure oxidation system. The leak-tight oxidation furnace is a modified conventional oxidation furnace with an added mechanical pump and a tightly sealed door. A throttle valve is used to control the pressure of the furnace. Because there is no load lock in this oxidation furnace, care must be taken to avoid premature low-temperature oxidation before the desired thermal oxidation. In order to avoid ambient gas leakage into the reactor, joints and all parts are carefully sealed and leak-checked using He gas. To minimize the air and moisture in the reactor during loading, the system is operated at 350°C to continuously outgas and a high-flow-rate nitrogen (N_2) purge is also applied. After wafer loading, the reactor is subsequently pumped to its lowest pressure and purged with hydrogen (H_2) or N_2. A high flow rate of H_2 or N_2 is applied during temperature ramp-up in order to maintain ultradry conditions inside the reactor.

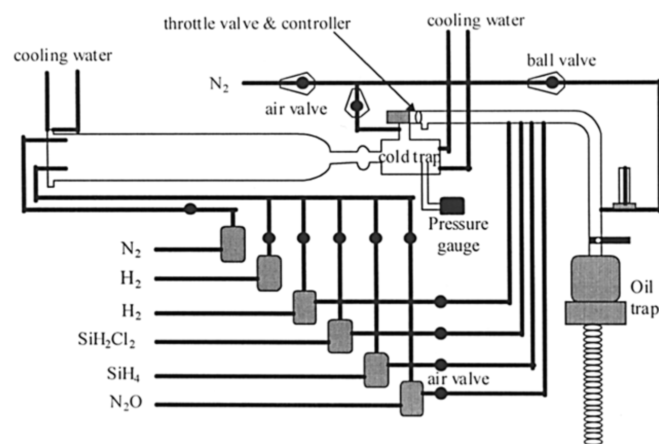

Figure 1. Schematic diagram of the low-pressure oxidation furnace.

Four-inch p-type (100) wafers are used in this study and are cleaned by modified RCA clean, followed by HF dipping and spin-dry. To study the various process dependencies of native oxide formation, we grew native oxides in air for 20 min, 17 MΩ cm deionized water for 10 min, and 80°C H_2O_2 for 8 min before oxidation. The measured native oxide thicknesses of these wafers were 0.6-0.8 nm. To avoid any process-related variation, all three wafers with different native oxides were processed simultaneously. After loading these wafers, a N_2 ambient was maintained at a pressure of 2 Torr during heating. Subsequently, thermal oxides were grown by N_2O at either 850 or 900°C and the thicknesses were measured by ellipsometry. Because of the self-limiting growth mechanism, N_2O-grown oxynitride can achieve the same thickness with different-process-formed native oxides. To study the relationship of native oxide on leakage current, we have also grown the thermal oxide with and without the presence of residual native oxide. The native oxide can be desorbed in situ with a 900°C H_2 bake for 30 min. The native-oxide-free surface is confirmed in a separate experiment on Si epitaxy.[10,11] Then poly-Si is deposited on the oxide and doped by phosphorous from $POCl_3$ followed by Al evaporation, patterning, etching, and sintering. We have used high-resolution transmission electron microscopy (HRTEM) to investigate the interface roughness, atomic force microscopy (AFM) to measure surface roughness, and the electrical J-V characteristics were measured by a curve tracer.

Results and Discussion

We characterized the oxide by cross-sectional TEM. As shown in Fig. 2a, atomically smooth interfaces between oxide and bulk-Si were obtained for the ultrathin 2.7 nm oxide grown by low-pressure oxidation with in situ native oxide desorbed. This smooth interface is comparable to our previously published data at a higher H_2-baked temperature of 950–1000°C.[9] In order to show this very smooth interface over a large distance, we also observed the interface over a wide range. As shown in Fig. 2b, good interface smoothness can last over 100 nm, indicating the importance of the native oxide removal step.

We have further characterized the surface smoothness of the oxide by AFM. The advantage of AFM is the capability to measure a large area. Figure 3a-c shows the AFM pictures of the 2.7 nm oxides grown by a conventional method without H_2 prebake, by the

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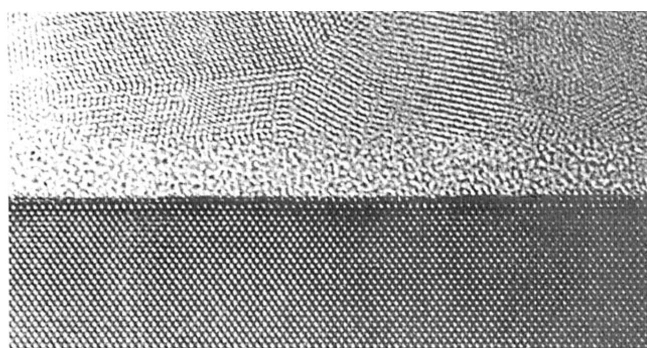
850 and 900°C H_2 prebake, respectively. A measured root-mean-square (rms) roughness of the oxide grown conventionally is 0.20 nm, the typical value reported in the literature. In contrast, a much smoother surface of the same 2.7 nm oxide is obtained after H_2 prebake at 850 or 900°C, and rms roughnesses of 0.07 and 0.03 nm, respectively, are measured. The improved smoothness with increasing prebake temperature may be due to the more efficienct native oxide removal. It is important to notice that the measured smooth surface by AFM is also consistent with the atomically smooth interface observed by cross-sectional TEM shown in Fig. 2.

We also studied the electrical characteristics of the thin oxides with various native oxide formation processes. Figure 4 shows the effect of native oxide on J-V characteristics of MOS diodes with a 2.4 nm gate oxide. The diodes are 500 × 500 μm in area. From the J-V characteristics, oxides grown in wafers that are covered with a chemical oxide formed in H_2O_2 shows the highest leakage current in the low-voltage region ($V < 0.5$ V). Excessive leakage current is also observed in this voltage region, while native oxide was formed in deionized water. Because these three wafers with different native oxides were processed identically and simultaneously oxidized by N_2O, any process-induced variation can be minimized. Furthermore, the self-limiting growth mechanism for oxynitride grown by N_2O also gives the same measured thickness within experimental errors. Therefore, this excess leakage current is from the different native oxide formation methods. The near-identical current densities at voltages above 0.5 V are due to the direct-tunneling process that dominates the electron transport at higher electric field. The same current densities at higher voltages also suggests the same oxide thickness among the three different samples.

We also measured surface roughness of the 2.4 nm oxides with different native oxide formation processes. As shown in Table I, the oxides grown in wafers covered with a chemical oxide formed in H_2O_2 showed the smoothest surface after oxidation. Therefore, the excess leakage current measured in this sample is not due to interface roughness and may come from the oxide itself. Because excess leakage current in thin oxide is also observed by Liu et al.,[1] similar trap-induced leakage currents may be responsible for the large leakage currents of oxide with H_2O_2 pretreatment. Although part of the weak SiOH bonding in chemical oxide can be converted into normal SiO_2 during thermal oxidation, this process may be limited by the short oxidation time and the thinness of the oxides. The insufficient conversion of poor-quality native oxide may explain the excess leakage current of oxide with H_2O_2 pretreatment and the reported intrinsic defect-induced excess leakage current.[1]

We also investigated the presence of residual native oxide on leakage current. Figure 5 presents J-V characteristics of oxides



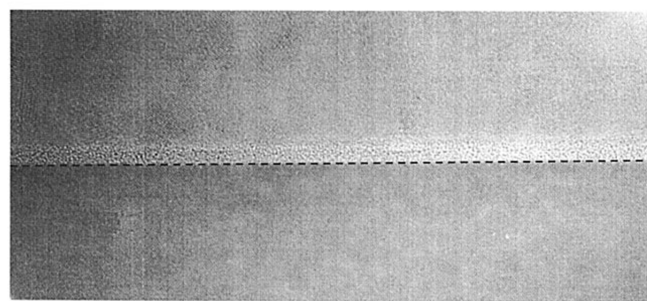
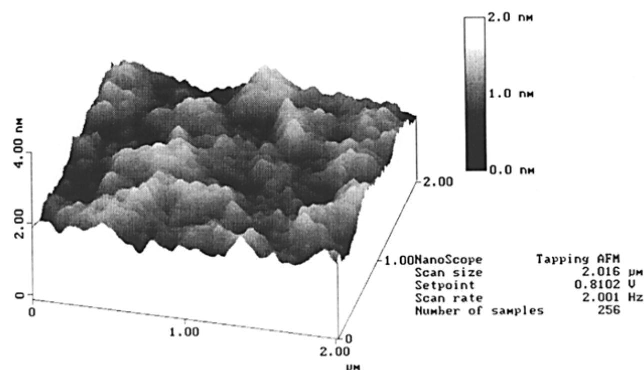
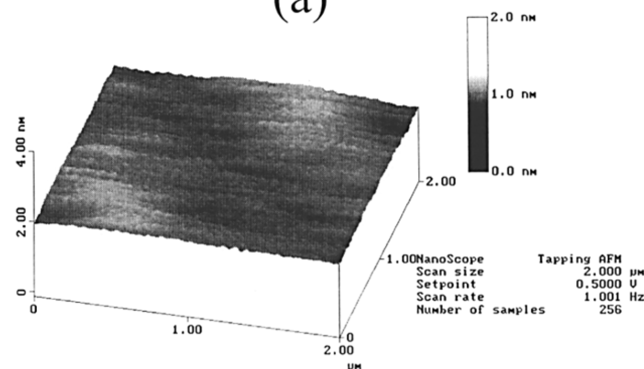


Figure 2. (a) Cross-sectionl TEM view of the 2.7 nm oxide to show atomically smooth interface between oxide and bulk Si. (b) Such a smooth interface can last over a wide range.





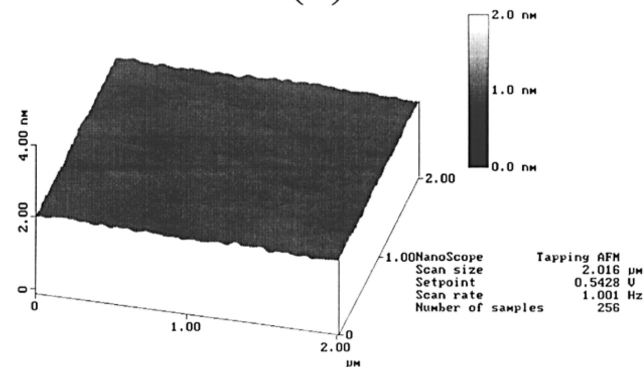


Figure 3. AFM pictures of the 2.7 nm oxide grown by (a) a conventional method without H_2 prebake, (b) an 850°C H_2 prebake, and (c) a 900°C H_2 prebake.

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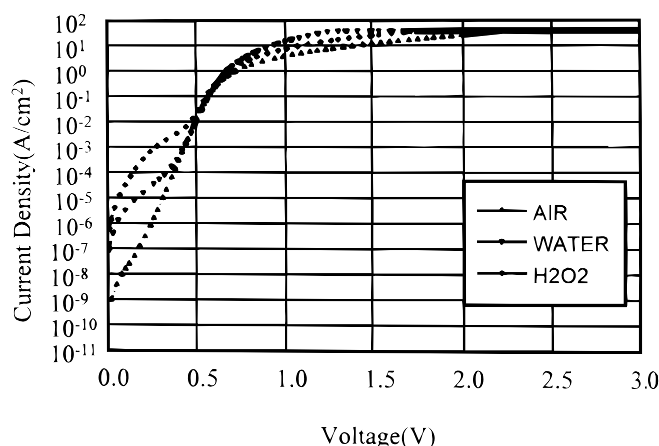

Figure 4. J-V characteristics of 2.4 nm oxides with various native oxide forming processes.

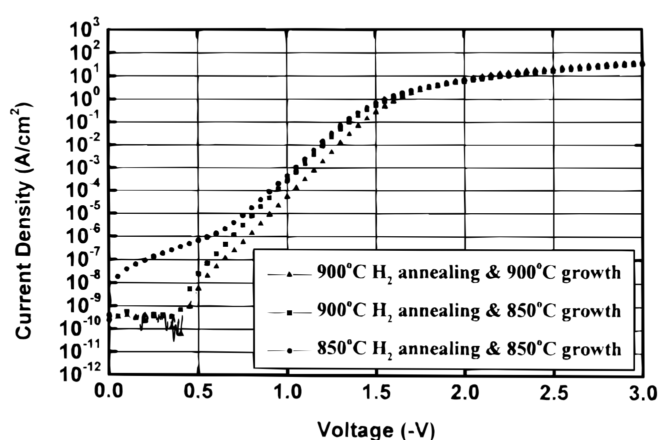

Figure 5. J-V characteristics of grown oxides H_2-baked at different temperatures.

grown at different temperatures and different H_2-bake temperatures. As shown in this figure, the leakage current is strongly temperature-dependent. Oxides with a 900°C H_2 bake showed much improved leakage current in the low-voltage region ($V < 0.7$ V) than those baked at 850°C. At the same 900°C H_2 bake, further increase in growth temperature from 850 to 900°C shows little improvement if considering a 0.1–0.2 nm thickness difference. Therefore, this 900°C H_2 bake is the key factor to achieving low leakage current. This conclusion is also consistent with the improved surface roughness in Fig. 3b and c and the observed atomically smooth interface by cross-sectional TEM in Fig. 2a. Therefore, the in situ native oxide desorption process is essential to achieve low leakage current and good surface and interface smoothness.

Conclusions

We have developed a process to grow the ultrathin oxide with good thickness uniformity and interface smoothness. Removing native oxide in situ prior to thermal oxidation is the key step to achieving atomically smooth interfaces and low gate leakage currents.

Table I. Surface roughness of different native oxide formation processes.

RMS (Å)	Air	H_2O	H_2O_2
Before oxidation	0.7	1.2	0.7
After oxidation	2.0	1.9	1.1

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