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Application of Selective Liquid-Phase Deposition to Fabricate Contact Holes Without Plasma Damage

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This work develops an alternative method, selective liquid-phase deposition (S-LPD), to fabricate contact holes instead of reactive ion etching. In preliminary experiments, deep n^+/p junction diodes with contact holes prepared by S-LPD exhibit much less reverse current, unity ideality factor, larger forward current, lower contact resistance, and higher thermal stability than those prepared by reactive ion etching. Further superiority of plasma damage-free near-surface regions is also investigated using Schottky and ultra-shallow junction diodes. Experimental results indicate that S-LPD can be applied to the submicron contact-hole process. The data after reverse bias temperature stress reveals the satisfactory reliability of S-LPD contact holes. This work demonstrates that the S-LPD technology is a highly promising means of replacing reactive ion etching processes to form submicron contact holes as reliably as those by wet-etching.
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Owing to its anisotropic etching ability, reactive ion etching (RIE) is extensively used to etch silicon oxide to form contact holes or interconnect vias. However, because of inevitable energetic ions and fluoride radicals in the plasma ambient, RIE causes damage, defects, polymer residue, and radical contamination[1-5] on etched surfaces, and induces oxide traps in the SiO_2 or interface states at the SiO_2/Si interface.[6-8] Therefore, the reverse current, contact resistance, and oxide leakage of devices are inevitably enlarged due to the undesirable effects described previously.[5,9,10,11] Currently, the issue of RIE selectivity has become increasingly critical in ultra-shallow junctions because overetch is less tolerated. To alleviate these problems on RIE-etched silicon surfaces, several modified and complex dry-etching techniques, e.g., magnetically enhanced reactive ion etching (MERIE),[2,12] and electron cyclotron resonance (ECR) plasma etching,[10,13] have been developed. Many different etchant sources, e.g., CF_4, CH_xF_{4-x}, NF_3, SF_6, SiF_4, BCl_3, and HBr etc., have also been developed to increase etching selectivity or reduce the effects of impurities and defects on the etched surface.[14] Several severe postcleaning and post-treatment methods after RIE have also been developed to remove damage or polymer residues.[5,15-17] Although these post-treatment techniques have been improved once again and the RIE apparatuses have gradually become extremely expensive, RIE cannot be compared with conventional wet-etching in the integrity of the etched surface.[9,10,16] In addition, to improve the overetch problem, many techniques, e.g., laser interferometry, optical emission spectroscopy (OES), invasive Langmuir probes, and radio-frequency power monitoring, have been developed as an end-point detector.[18-20] Despite additional equipment and high cost, each proposed technique has drawbacks and limitations.

To avert these problems, an alternative method without RIE etching must be developed. Our previous studies have investigated liquid-phase deposition (LPD) technology,[21-24] and applied it to the gate insulator of thin-film transistors (TFTs).[25,26] Many physical and chemical characteristics, such as Auger electron spectroscopy (AES) analysis,[21,22] Fourier transform infrared (FTIR) spectra,[22,24] X-ray photoelectron spectroscopy (XPS) measurement,[24] extraction of interface trap,[25] film stress measurement,[23] stress hysteresis,[23] etc., for LPD dielectric films have been surveyed and analyzed in our proposed papers.[21-25] The LPD technique has also been applied to form the interlayer dielectric (ILD) in multilevel tungsten interconnect structures.[28] These studies confirm that LPD oxide possesses excellent electrical properties, low dielectric constant (k)[22] and low stress.[23] Due to low stress, LPD oxide exhibits fewer trap states than plasma-enhanced chemical vapor deposited (PECVD) oxide at the oxide/Si interface.[23,25,27] This reveals there is a better interface state between silicon and LPD oxide than conventional PECVD oxide. Especially, LPD oxide can be selectively deposited against photoresist if the deposition condition is adequately controlled.[29,30] This implies the feasibility of applying selective LPD (S-LPD) to create contact holes or vias. In addition, the cost of LPD apparatus is quite low, because no vacuum facilities and no corresponding etching monitors are necessary. In this work, we first apply S-LPD to form contact holes for n^+/p diodes, Schottky diodes, and Kelvin resistors and thereby study the superiority of utilizing plasma-free S-LPD over the conventional RIE. It is expected that in addition to forming contact holes with submicron meter scale as RIE, S-LPD can also obtain device performance comparable to wet etching.

Experimental

The process and mechanism of S-LPD have been described in our previous literatures.[29-31] Figure 1a indicates that the process window of S-LPD is a function of silicic acid $Si(OH)_4$ concentration and deposition temperature. In this work, we mainly perform the S-LPD under a condition at $Si(OH)_4$ concentration of 7.3×10^{-3} mol/L and 23°C. The SEM photograph in Fig. 1b shows the LPD oxide is selectively deposited against photoresist. It preliminarily reveals the absence of particles and indicates the feasibility of forming half-micrometer contact holes with a high aspect ratio.

The devices, including n^+/p diodes, Schottky diodes, and Kelvin resistors, were fabricated with their contact holes prepared using S-LPD and RIE, respectively. The p-type (100) wafers with 15-25 Ω cm bulk resistivity were adopted in the n^+/p diodes and Kelvin resistor fabrication. Following the formation of channel stopper and field oxide, phosphorus with a dose of 5×10^{15} cm^{-2} and energy of 40 keV was implanted to make n^+/p junction, and then the 30 min annealing at N_2 900°C was performed for dopant activation. As shown in the left portion of Fig. 2, for S-LPD samples the photoresist on the area defined as the site of contact hole was kept intact. Next, the LPD oxide was selectively grown on the region without photoresist by using S-LPD. After removing the photoresist, the contact holes were automatically formed. For RIE samples, as shown in the right portion of Fig. 2, LPD oxide was globally deposited to cap the n^+/p diodes. Then the contact holes were defined through lithography and etched using RIE. To increase the etching selectivity of SiO_2/Si[14] and reduce chamber particles,[32] the RIE was performed under the following conditions: a CHF_3/O_2, ratio of 20/5 sccm, 50 mTorr pressure , and 100 W rf power. Before metallization, the contact holes of both S-LPD and RIE were cleaned sequentially with H_2SO_4/H_2O_2, NH_4OH/H_2O_2, HCl/H_2O_2, and diluted HF solution (standard RCA cleaning). In addition to Al/Si contact, for some samples, 20 nm thick titanium was used between Al and Si to serve as a titanium silicide barrier to reduce spiking. The purpose of using a

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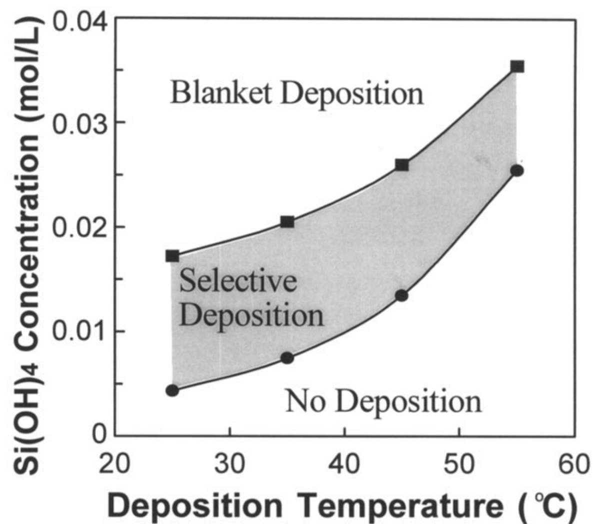
single Ti barrier is due to low resistance with respect to using TiN/Ti barrier or Al:Si(1-2%) alloy. Especially for Al:Si/n^+-Si contact, an undesirable increase in contact resistance arises from silicon precipitates which occur preferentially around the contact hole edges.[33] After metallization, some n^+/p junction diodes were sintered at 400°C for 30 min in N_2. The temperatures of all processes after S-LPD are below 500°C, the outgassing temperature of fluorine in LPD dielectric,[22] so there is no effect due to fluorine outgassing. In addition to n^+/p diodes, the Kelvin resistors were also fabricated under an identical conditions. For Schottky diodes, the fabrication procedures closely resembled those of n^+/p diodes except for use of 1-5 Ω cm, n-type (100) wafers and the fact that no ion-implantation was necessary.

Subsequently, we further applied S-LPD to the ultrashallow n^+/p junction diodes. All processes closely resembled those mentioned previously except (*i*) the n^+ region was prepared with 5 keV, As^+, 2×10^{15} cm^{-2}, and then annealed with rapid thermal annealing (RTA) in the N_2 ambient. (*ii*) For the RIE sample, the partial-RIE (P-RIE) was employed to etch contact holes. The P-RIE refers to a situation in which most of the capping oxide thickness was etched with RIE and then the remaining oxide of about 20-30 nm was wet-etched by buffer HF solution. This modification attempts to reduce the RIE overetch, because etching rate nonuniformity easily leads to overetch-through in ultrashallow junctions. (*iii*) To resemble the common RIE process, P-RIE samples were prepared by using plasma-enhanced chemical vapor deposited tetraethylorthosilicate (PE-TEOS) oxide as a capping layer. The PE-TEOS oxide was deposited in the TEOS/O_2 ratio of 10/200 sccm, 300 mTorr pressure, and 200 W power. (*iv*) Titanium thickness of all ultrashallow n^+/p diodes was reduced to 12 nm.



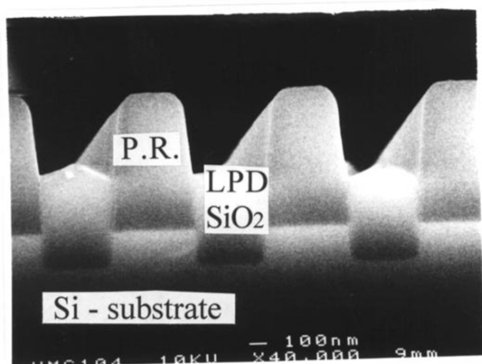


Figure 1. (a) Process window and (b) SEM photograph for S-LPD.

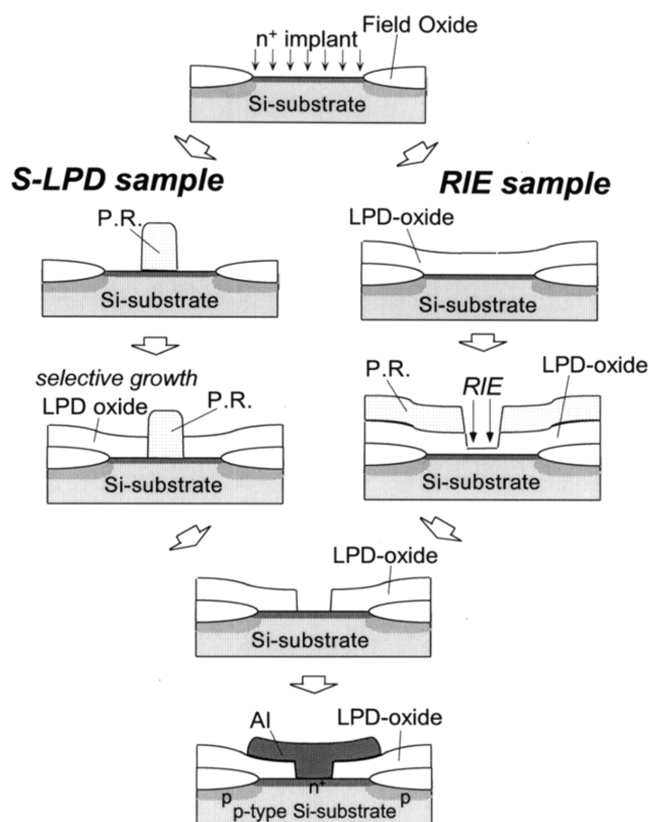


Figure 2. Process-flow diagram of n^+/p junction diodes with contact hole fabricated by S-LPD (left) or conventional RIE (right).

Results and Discussion

n^+/p junction diode.—Figure 3 shows the typical current-voltage (I-V) characteristics of n^+/p diodes with contact holes prepared by S-LPD and RIE before and after sintering, respectively. The metal contact of Al/n^+-Si is 60 × 60 μm, while the junction area is 100 × 100 μm. According to this figure, before sintering the reverse current of S-LPD samples is one order less than that of RIE. As for the forward bias, the ideality factor, η, of 1.13 in S-LPD samples is also superior to that of 1.57 in RIE samples. This indicates that relatively few generation-recombination (G-R) centers are in the depletion region of S-LPD diodes such that η approaches 1. Table I summarizes several key characteristic parameters. The reverse current ratio of 400 × 400 μm diodes to 100 × 100 μm diodes (I_{400}/I_{100}) is 3.27 for the S-LPD sample, while it is 5.15 for the RIE sample. The I_{400}/I_{100} ratio of 5.15 exceeds the geometry ratio of the junction perimeter, i.e., 1600/400 μm = 4. From the fitting with the equation $I_R = J_{RA} \times L^2 + J_{RP} \times (4L)$, where J_{RA} and J_{RP} are the partial current densities due to junction area leakage and junction periphery leakage, respectively, the factor of $I_{400}/I_{100} > 4$ indicates that the effect of J_{RA} is rather significant for the RIE sample. The RIE method easily causes lattice defects and bonding defects, which function as deep-level traps[1,34] and donor-like charge states,[35] respectively. For the contact etched by CHF_3, it has been detected by deep-level transient spectroscopy (DLTS) that a dominant trap arises from H(0.40) Si defects and locates at about 0.65 eV above the valence band.[1] These states and traps serve as G-R centers and significantly enlarge the reverse current. In addition, fluorine-contained ion bombardment and permeation also cause soft breakdown.[36] These factors account for why the reverse current is rather high for

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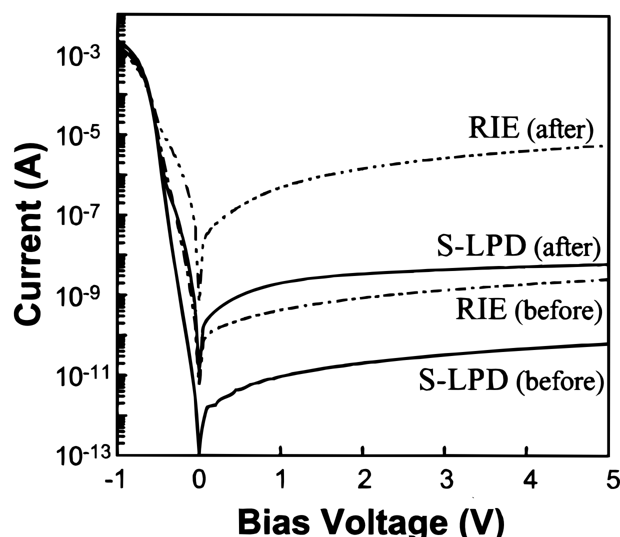

Figure 3. Comparison of I-V characteristics between n^+/p diodes with S-LPD and RIE contact (Al/Si) holes.

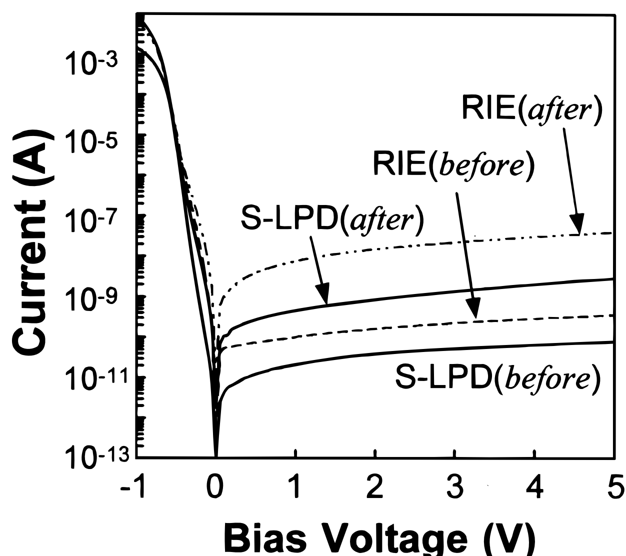

Figure 4. Comparison of I-V characteristics between n^+/p diodes with S-LPD and RIE contact (Al/Ti/Si) holes before and after sintering.

RIE samples. After sintering, the reverse current of RIE samples increases drastically. This large leakage magnitude after sintering indicates a spiking enhanced by RIE damage. It has been proposed that RIE can damage the etched surface to become as rough as 30 nm and makes the spiking effect easily occur during sintering treatment.[5] In contrast, S-LPD can avoid a large reverse current owing to no plasma-induced defects and no energetic ion bombardment damages during contact hole formation.

Figure 4 shows the performance of S-LPD and RIE diodes with Al/Ti/Si contact, respectively. Before sintering, the I-V characteristics of S-LPD samples are still superior to those of RIE samples. After sintering, both the reverse currents increase, while RIE samples increase more significantly than S-LPD samples. This can be attributed to many defects and contamination induced by RIE diffusing from contact-hole surfaces into the junction depletion region during sintering. In particular, the metallic contamination sputtered from the RIE chamber wall enlarges reverse current after sintering.[37] Having no such drawbacks, the S-LPD samples exhibit relatively good thermal stability. Figure 5 shows the accumulative distribution for the reverse currents of all measured diodes. For S-LPD samples, the reverse currents distribute in a more confined region; however, for RIE samples, they separate from nanoampere to microampere magnitude. This finding indicates another superiority that S-LPD has no nonuniformity problem of RIE etching rate.[38] So far, applying S-LPD can avoid the problem of defects, contamination, rough-etched surfaces, and etching rate nonuniformity caused by RIE. These results preliminarily prove the superiority of S-LPD replacing RIE to form contact holes.

Ohmic contact resistance.—According to Fig. 3 and 4, the forward current of S-LPD samples is larger than that of RIE samples at forward bias −1.0 V, whether a titanium barrier is used or not. This implies that applying S-LPD can effectively reduce forward series resistance. Because all processes are the same except the contact-hole formation, it is believed that for RIE samples, the additional resistance must result from contact resistance. To investigate contact resistance, we further fabricated four-terminal Kelvin D-resistors,[39] as illustrated in the Fig. 6 inset. The n^+ doping region of sheet resistance 25.5 Ω/□ was adopted for all resistors. The Kelvin contact

Table I. Comparison for key characteristic parameters of diodes and ohmic contacts between S-LPD and RIE contact holes.

	S-LPD	RIE
n^+/p diode		
Ideality factor η (Al/Si) (−0.4 to −0.5 V)[a]	1.13	1.57
Dimension current ratio I_{400}/I_{100} (5.0 V) [a]	3.27	5.15
Ideality factor η (Al/Ti/Si) (−0.4 to −0.5 V)	1.17	1.64
Ohmic		
Contact resistivity ρ_{ce} (Ω cm^2) [b]	2.5×10^{-6}	$\sim 12 \times 10^{-6}$
Schottky diode		
Schottky η_{sc} (0.1-0.3 V)	1.11	>3.0
Schottky barrier height (eV)	0.83	0.60
Ultrashallow n^+/p diode		
Ideality factor η (−0.4 to −0.5 V)	1.03	1.13[c]

[a] Diodes with Al/Si contact considered before sintering.
[b] Sheet resistance, R_s, 25.5 Ω/□.
[c] P-RIE was adopted.

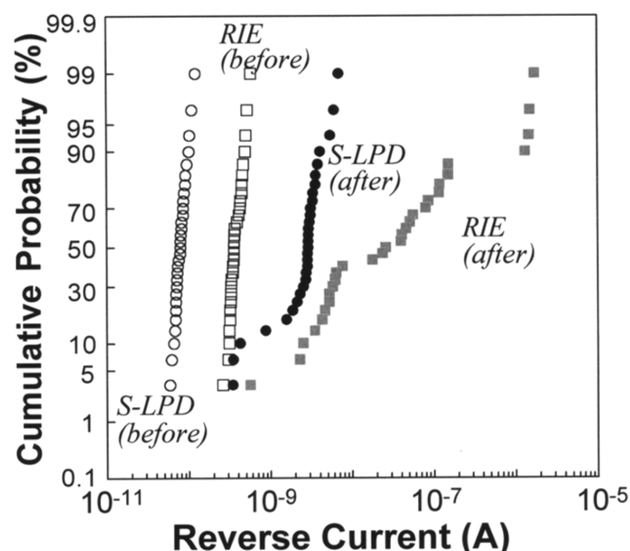

Figure 5. Cumulative distribution for reverse currents, at reverse bias 5.0 V, of all measured S-LPD and RIE n^+/p diodes before and after sintering.

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resistance, R_C, is defined by the voltage 2 to 4 over the fed current 1-3, i.e., the curve slope of V_{24}-I_{13} plot. Figure 6 depicts the typical R_C characteristics of the resistor with the contact size $L \times L = 10 \times 10$ μm and the collar width $d = 10$ μm at the fed current ranging from −4 to 4 mA. The S-LPD contact shows a linear I-V relationship and exhibits a smaller R_C than the RIE contact. Meanwhile, the RIE contact shows a nonlinear I-V relationship and therefore exhibits a nonconstant and larger R_C value, especially at the small fed current. This occurrence is because in the RIE process, the polymer and photoresist residues are difficult to be cleaned owing to the energetic plasma bombardment.[5] In addition, the large R_C can also be attributed to the decreased mobility in the etched surface.[40] Interestingly, the impurities and residues impinged by RIE scatter the drift electrons and holes, thereby reducing the effective mobility. Owing to the scattering, the drift carriers are scattered rather seriously if they move at a low velocity. This is the reason the R_C of RIE contact becomes large, particularly in small fed current, and exhibits nonlinear I-V characteristics. For S-LPD contact, it is relatively easy to clean the photoresist residues because of no energetic bombardment. Therefore, the I-V characteristics show linearity with low slope and exhibit the superiority of being plasma-damage free.

Figure 7 depicts the relationship between contact resistance, R_C, and different contact-hole sizes for the S-LPD and RIE samples. According to this figure, the S-LPD contacts always exhibit a lower contact resistance than the RIE ones for all contact-hole sizes. In addition, compared to RIE contacts, the R_C reduction has a tendency of becoming more apparent in small contact-hole sizes. On the other hand, the R_C values vs. the contact-hole sizes exhibit a linear trend with about −1 slope, regardless of whether for S-LPD or RIE samples. This indicates that our Kelvin resistors can eliminate most of the parasitic resistance and thus can be used to extract specific contact resistivity, ρ_{Ce}, and make ρ_{Ce} close to the actual contact resistivity ρ_C.[39] To extract the ρ_{Ce}, we incorporate the measured R_C values with different L/d ratio into the simulated universal curves of Kelvin D-resistors. As shown in Fig. 8, for resistors with different L/d ratios, the R_C/R_S values of S-LPD samples are much smaller than those of RIE samples. Following the extraction procedures of ρ_{Ce},[41] the specific Al/Si contact resistivity, ρ_{Ce}, as listed in Table I, is about 2.5×10^{-6} Ω cm^2 for the S-LPD contacts; however, it is about 12-13 $\times 10^{-6}$ Ω cm^2 for the RIE contacts. Because the contact resistivity is very sensitive to the cleanness and integrity at the metal/Si interface, the specific ρ_{Ce} of RIE must be larger than that of S-LPD.

Schottky diodes and ultrashallow n^+/p junction diodes.—Now that the S-LPD method has been preliminarily shown feasible to replace RIE in contact-hole formation, especially in damage-free and contamination-free processes to further prove its excellence without plasma, the performance in near-surface regions is next investigated thru Schottky and ultrashallow junction diodes.

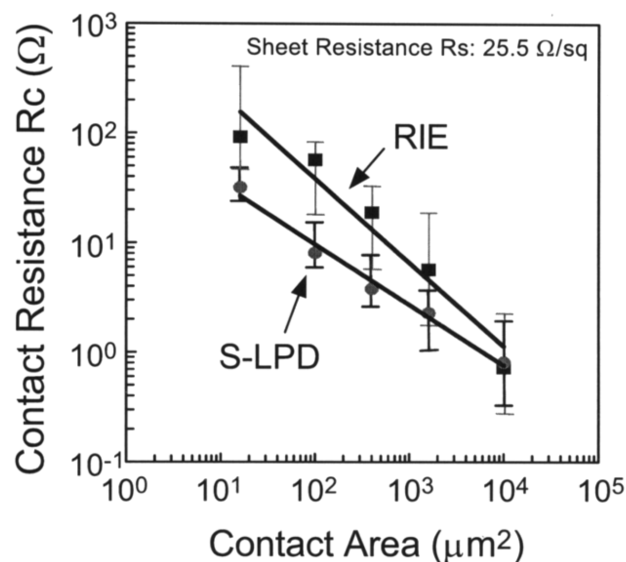

Figure 7. Comparison of contact resistance, R_C, between S-LPD and RIE contact holes for different contact sizes.

Schottky diodes.—Figure 9 depicts the performance of S-LPD and RIE Schottky diodes with Al/n-Si (1-5 Ω cm) contact before/after N_2 400°C sintering, and Table I also summarizes their key characteristic parameters. Before sintering, the RIE sample nearly loses the rectifying characteristics of a Schottky diode under reverse bias, while the S-LPD sample exhibits satisfactory Schottky characteristics. However, after sintering, the S-LPD sample still exhibits about four orders smaller than that of RIE sample in reverse current. Meanwhile, the ideality factor 1.11 of the former is lower than 4.05 of the latter. The worse ideality of RIE samples is attributed to the large surface recombination velocity.[42] According to the curves of $\ln\{I/[1 - \exp(-qV/kT)]\}$ vs. forward-bias voltage, the potential barrier is 0.83 eV for the S-LPD Schottky diodes and 0.60 eV for the RIE ones, respectively. As generally contended, the donor-like bonding defects and the polymer residues make the depletion region

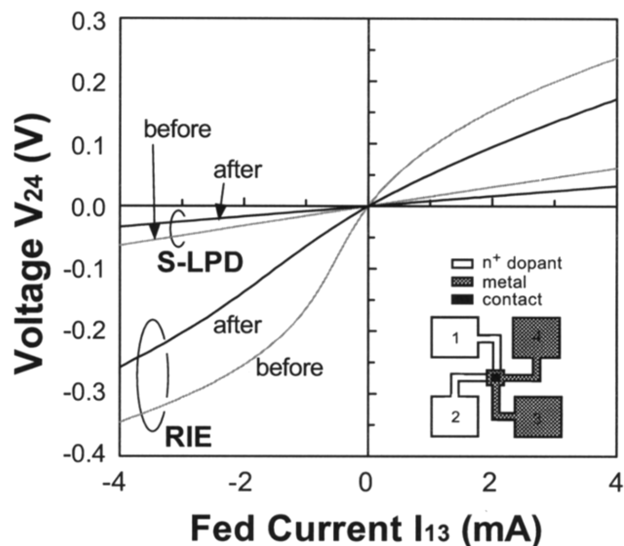

Figure 6. V-I plot of Kelvin D-resistors with S-LPD and RIE contact holes, respectively.

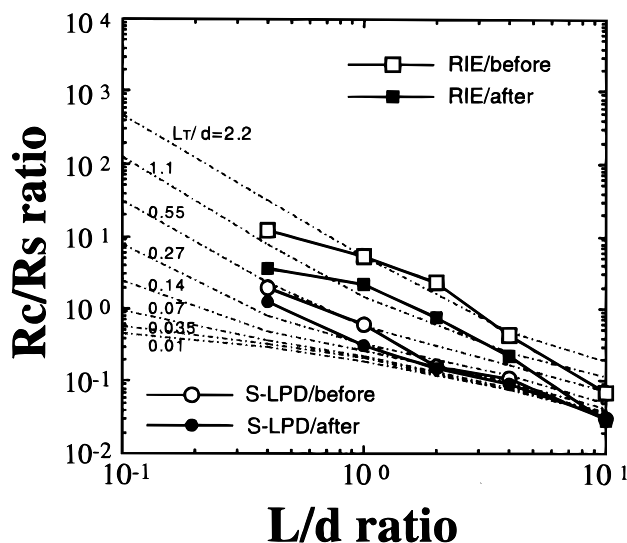

Figure 8. Measured R_C/R_S within simulated universal curves for the Kelvin D-resistors with S-LPD and RIE contact holes, respectively.

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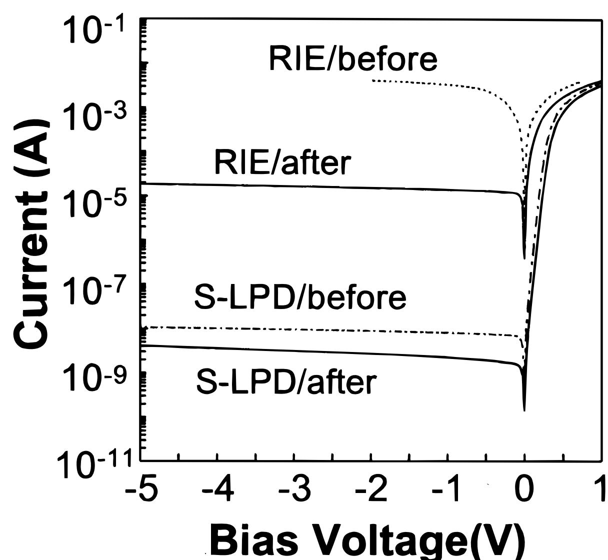

Figure 9. Comparison of I-V characteristics between Schottky diodes with S-LPD and RIE contact holes, before and after sintering (Al/n-Si contact area 500 × 500 μm).

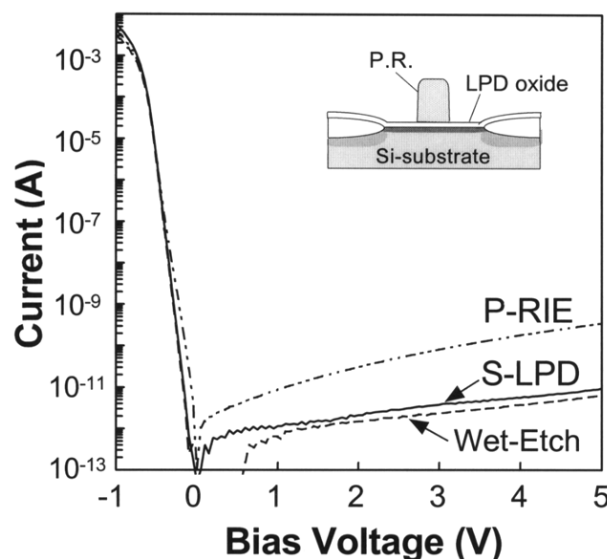

Figure 10. Comparison of I-V characteristics among ultrashallow n^+/p junction diodes with S-LPD, wet-etch (LPD), and P-RIE (PE-TEOS) contact holes (Al/Ti/Si contact) after sintering.

thin[43] and lower the potential barrier. These results indicate that for the RIE Schottky diodes, the sintering is essential to release some of the residues and the defects from the Si surface but is unnecessary for the S-LPD sample. Accordingly, the RIE process becomes more critical and requires additional post-treatment.[16] S-LPD can avert these problems and is indeed a highly promising candidate as a plasma-damage-free, energetic-impurity-free, and polymer-residue-free technology.

Ultrashallow n^+/p junction diodes.—Because the demand for plasma-damage free technology has been increasingly urgent in fabricating deep submicron devices, the S-LPD technique was next applied to the formation of contact holes for ultrashallow n^+/p junctions. Herein, the junction depth estimated with TSUPRUM-4 is about 20-30 nm, while the implantation of 5 keV As^+, 2×10^{15} cm^{-2} is adopted, and following with 15 s, 1050°C RTA. While fabricating the ultrashallow junction diodes, the RIE samples were modified by applying PE-TEOS capping and partial-RIE (P-RIE). Meanwhile, to segregate all lithography residues from the contact region, a simple modification of S-LPD was performed with a thin LPD-oxide (15-20 nm) globally deposited before lithography, as illustrated in the Fig. 10 inset. After finishing S-LPD and removing the photoresist, the thin LPD oxide was removed by dipping buffer HF solution and then the contamination-free contact holes were formed. Besides the large area samples with the Al/Ti/n^+-Si contact area of 60 × 60 μm and the n^+/p junction area of 100 × 100 μm, the submicron samples with junction area of 2.8 × 50 μm and 25 contact holes of 0.8 × 0.8 μm were also fabricated. Photoresist removal and cleaning for the submicron samples was performed by 60 s ozone ashing of 300°C and followed by RCA cleaning. In addition to S-LPD and P-RIE, the reference samples (wet-etch) with LPD-oxide capping and completely butter HF wet-etching were also prepared.

Figure 10 shows the typical I-V characteristics of ultrashallow junction diodes with 60 × 60 μm contact holes prepared by S-LPD, wet-etch, and the P-RIE method, respectively, after sintering. The S-LPD diodes as well as wet-etch reference diodes exhibit nearly identical I-V characteristics in both forward bias and reverse bias. This proves that applying S-LPD can form excellent diodes comparable to the wet-etch reference diode. By contrast, the P-RIE diodes still exhibit two orders higher reverse current than the S-LPD ones at 5.0 V. This can be attributed to some energetic ions or accelerated radicals penetrating through the 20-30 nm remaining oxide into the Si substrate. In addition, the microtrenching effect[44] due to ion reflection from the photoresist sidewall also causes overetch at the contact periphery and enhanced penetration. However, these undesirable problems never occur in the S-LPD diodes.

Figure 11 shows the accumulative reverse-current distribution of all measured S-LPD diodes and P-RIE diodes at reverse bias 2.5 V. All reverse currents of S-LPD diodes accumulate at about several picoampere magnitude either before or after sintering. In addition, the S-LPD diodes after sintering show slightly lower reverse currents than those before sintering. This is consistent with the proposed results of Ti-silicide contact reducing reverse current after thermal treatment.[45,46] For the P-RIE diodes, exhibit not only high reverse currents but also greatly increase to 10^{-4} Å after sintering. This reveals that the titanium occasionally loses its barrier effect in some P-RIE diodes, yet this failure does not occur in all S-LPD diodes. Cumulatively, our results demonstrate that even if P-RIE has been adopted to avoid overetching, S-LPD samples are still superior to P-RIE samples.

Figure 12 shows the typical diode I-V characteristics of the submicron samples. The satisfactory forward and reverse current reveal the complete cleaning for the photoresist of S-LPD samples by combining

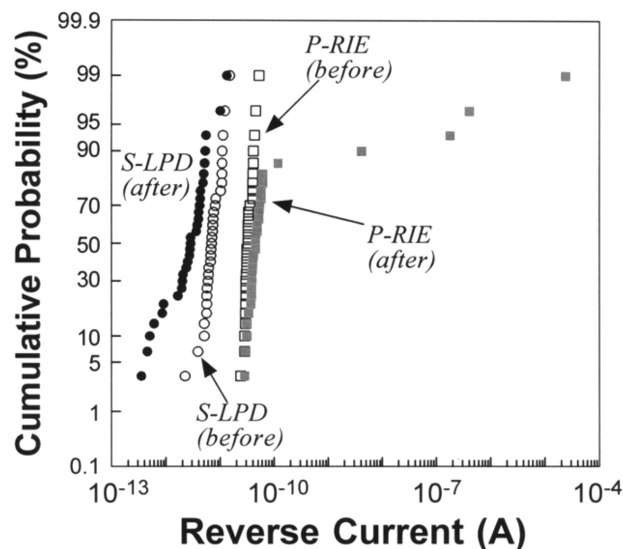

Figure 11. Cumulative distribution for reverse currents, at reverse bias 2.5 V, of all measured S-LPD and P-RIE ultrashallow n^+/p junction diodes before and after sintering.

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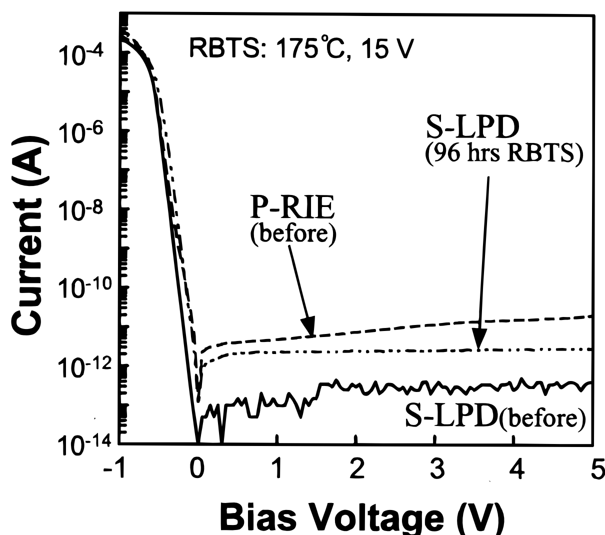

Figure 12. I-V characteristics of S-LPD submicron samples (contact area 0.8 × 0.8 μm; Al/Ti/Si) (——) before and (-·-·-·-) after RBTS.

ozone ashing and RCA cleaning. The extremely low reverse leakage proves the superiority of applying S-LPD instead of RIE to 0.8 μm contact hole formation. These results indicate that S-LPD can be applied to the submicron contact hole processes. A reverse bias (15.0 V) and temperature (175°C) stress (RBTS)[47] was imposed on the S-LPD submicron samples for reliability examination. After stress of 96 h, shown as the dash-dot line in Fig. 12, junction leakage is still kept at very low leakage magnitude (2.8 pA) and is indeed lower than the leakage of the RIE submicron sample before RBTS. This reliability is much better than the proposed results[47] and indicates that a stable $TiSi_2$ structure is formed in S-LPD contact. Our RBTS results suggest S-LPD as a satisfactory method for reliable contact hole formation.

Conclusion

We have successfully applied the novel S-LPD method to form submicron contact holes and investigated its superiority through n^+/p diodes, Kelvin contact resistors, and Schottky diodes. The S-LPD n^+/p diode is superior to the conventional RIE diode with respect to its low reverse current, unity ideality factor, good thermal stability, low contact resistivity, and no problem of etching-rate nonuniformity. Compared with the RIE Schottky diode, the S-LPD Schottky also exhibits excellent rectifying characteristics with high potential barrier, 0.83 eV. The S-LPD ultrashallow junction diodes as well as wet-etch reference diodes show nearly identical I-V characteristics. The similar superiority of S-LPD also exists in our submicron samples. RBTS results suggest S-LPD as a method for reliable contact hole formation. In sum, the S-LPD technique has overcome many undesirable problems induced by RIE. That is, the S-LPD method indeed has the following superiorities in forming contact holes or vias for scaled-down devices: (*i*) it is a plasma-free process; (*ii*) it is a damage-free process; and (*iii*) it is a particle, residue, and contamination-free process. Accordingly, the S-LPD is a promising alternative for replacing conventional RIE for contact hole or via formation. In addition, LPD apparatus costs very little because no vacuum, power, gas-flow equipment, and corresponding etching monitors are needed. Therefore, we believe that in near future, the novel S-LPD method is a good candidate for fabricating the contact holes of deep-submicron devices without plasma damage to fulfill more reliable and more cost-effective requirements in ULSI technologies.

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