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Introductory invited paper

Reliability of ultrathin gate oxides for ULSI devices

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Abstract

Ultrathin gate oxide, which is essential for low supply voltage and high driving capability, is indispensable for the continued scaling of ULSI technologies towards smaller and faster devices. Needless to say, the reliability of ultrathin oxide is of major concerns in the manufacturing of the state-of-the-art metal-oxide-semiconductor devices. This paper reviews the reliability issues regarding ultrathin gate oxide for present and future ULSI technologies. Issues including gate leakage current, time-dependent dielectric breakdown, poly-gate depletion, boron penetration, and plasma process-induced damage will be addressed. Several techniques such as nitrided oxide and alternative processes, which are proposed to improve gate oxide reliabilities, are also discussed. © 1999 Elsevier Science Ltd. All rights reserved.

1. Introduction

To ensure the continued shrinkage of CMOS technologies down to sub-quarter micron regime and beyond, ultrathin gate dielectric with low defect density and high reliability is indispensable. In general, high driving capability and well-controlled short channel characteristics require the use of ultrathin gate oxides. Since Momose et al. first proposed the use of 1.5 nm direct-tunneling (DT) gate oxide for *n*-MOSFET with extremely high device performance in 1994 [1], many aggressive studies regarding direct tunneling gate oxide for sub-quarter micron devices have been carried out [2–10]. The application of DT gate oxide not only achieves high speed for logic circuits, but also essential for high-performance RF applications [8,9]. In addition, the use of thinner oxides is also critical to meet the demands of lower programming voltage for future nonvolatile memories [10,11].

However, the application of DT gate oxide to ULSI devices faces many challenges. Firstly, the presence of large quantum mechanical (QM) tunneling current is a serious scaling limitation in terms of standby power consumption [12]. Secondly, breakdown characteristics for ultrathin oxides become even more critical due to the dramatic increase in electric field across the oxide during normal device operation. Whether oxide becomes inherently more robust or more vulnerable to electric stress as it thins down, therefore, plays a very crucial role for its applications to ULSI devices. Thirdly, poly-gate depletion effects (PDE) are known to get worse with oxide scaling. This is because the operating gate voltage normally does not scale proportionally to the oxide thickness, and therefore, the average surface field increases. The additional voltage drop at the poly depletion layer results in undesirable drive

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current degradation [13]. Since these effects worsen for thinner oxides, it could become a limiting factor for future device scaling.

Furthermore, as gate oxide thickness decreases, several process integration issues emerge as new challenges. Boron penetration from the p^+-poly-Si gate into the thin gate oxide and the channel region in *p*-MOSFETs is one of the major concerns for dual-gate CMOS technologies. The penetration of boron into and through gate oxides results in threshold voltage instability, low-field mobility reduction, and gate oxide degradation [14–18]. The undesirable boron penetration effects are aggravated as gate oxide is scaled down. Finally, plasma-process-induced charging damage can result in severe degradation in oxide integrity as gate oxide thickness is scaled down [19–27]. The frequent use of plasma steps with high-density plasma reactor in advanced circuit manufacturing, coupled with the restriction that no high temperature anneal is allowed in back-end processing, aggravates the situation. It is, therefore, very important to characterize the performance of plasma processes in production with scaled oxides.

In this work, we will review recent studies on issues relating to the reliabilities of ultrathin gate dielectrics for present and future ULSI technologies.

2. Gate leakage current

2.1. Quantum mechanical tunneling

Significant leakage current that flows through gate oxide due to QM tunneling may cause reliability problems and limits device application. It is well known that as the gate oxide thickness is scaled down to 3 nm and below, the gate leakage current increases dramatically due to the occurrence of DT. This happens when oxide voltage is reduced to lower than 3.2 V, the tunneling barrier for electron changes from triangular to trapezoidal. The current conduction mechanism is the so-called DT current [28]. Typical gate current characteristics of ultrathin oxides (2.5–4.2 nm) and the simulated Fowler–Nordheim (F–N) current fitting curves are as shown in Fig. 1, while the simulated DT current for thinner oxides down to 1.5 nm are shown in Fig. 2. The F–N *I*–*V* fitting method for extracting ultrathin oxide thickness has been widely adopted because of its accuracy and convenience as an on-wafer measurement method [29,30]. By taking PDE into account, the method is well suited for ultrathin oxide measurements. This is especially so, considering the fact that PDE has made the extraction of oxide thickness from the traditional *C*–*V* measurements difficult. However, this method is not suitable for measuring oxide thickness thinner than 2 nm because not enough F–N current is available for extraction before oxide breakdown. Therefore, to find an accurate and convenient method to determine the exact oxide thickness in DT conduction region is important and urgent.

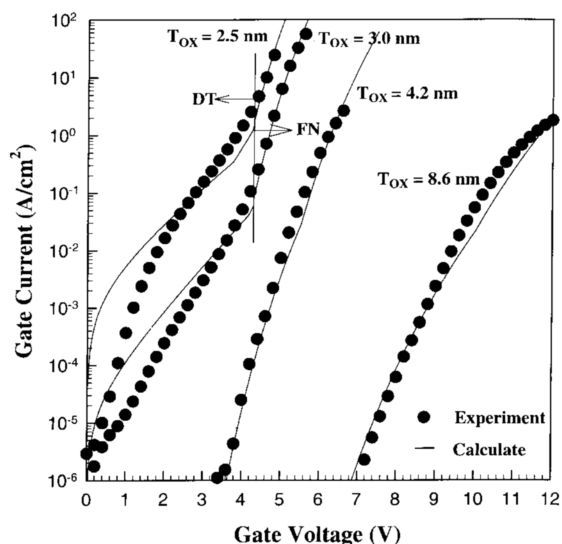

Fig. 1. Typical current–voltage characteristics of ultrathin oxides and the F–N current fitting curves. The stress polarity is under substrate injection mode with the poly-depletion effect taken into account.

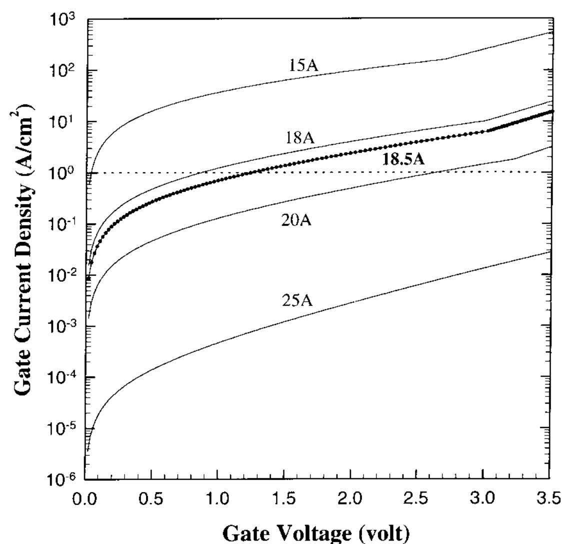

Fig. 2. Simulated current–voltage characteristics of direct tunneling current for ultrathin oxides with thickness ranging from 1.5 to 2.5 nm. The dotted line at $J = 1$ A/cm^2 indicates that the minimum thickness of silicon dioxide as gate dielectric will be around 1.85 nm.

2.2. Gate leakage current as a limitation of scaling

As a general rule, logic circuits can tolerate higher leakage current than memory circuits. It has been shown that the DT current associated with 1.5 nm oxide is comparably small to the large drain current of 0.1 μm MOSFET. However, leakage current of such magnitude could still result in lower data retention time for DRAM, higher chip standby power and accelerated device degradation. Thus, large DT current presents a scaling limitation for future CMOS technologies. To avoid CMOS operation at high electric field with large standby power, the power supply voltage (V_{dd}) has to scale more aggressively. This, however, defeats the purpose of scaling. To maintain device performance, it is projected that the oxide field during normal operation will stay at around 5 MV/cm [11], and that the minimum supply voltage will be around 1 V (0.9 V for worst case). If one assumes that the total active gate area per chip is of the order of 0.1 cm^2 for future generation technologies, the maximum tolerable tunneling current will be about 1–10 A/cm^2 [31]. As indicated in Fig. 2, the minimum thickness of silicon dioxide to meet this criterion as the gate dielectric will be around 1.85 nm.

2.3. Alternate gate dielectrics

To overcome the gate leakage current limitation for scaling of future CMOS technologies, many alternative materials with high dielectric constant ($\varepsilon_r \gg \varepsilon_{SiO_2}$) to serve as the gate dielectric were studied [32–44]. These 'high-k' materials can provide the same equivalent electrical thickness by a physically thicker layer which is, therefore, more controllable and hopefully more manufacturable. These films prepared with various advanced technologies have been shown to effectively reduce gate leakage current, suppress boron penetration and have higher time-dependent dielectric breakdown (TDDB) lifetime as well. These films fall into three main categories. The first group is nitride-related materials including oxynitride grown on nitrogen-implanted substrates [32], jet vapor deposited (JVD) nitride [33,34], and LPCVD nitride [35]. The second group belongs to metal oxides, such as Ta_2O_5 [41,43], TiO_2 [37,42,43], $BaSrTiO_3$ (BST) [42], Al_2O_3 [44] etc. The third group employs stack gate structures such as nitride/oxide [39,42], metal oxide/oxide [36,40] and metal oxide/nitride [39,42]. All three groups appear to be promising as potential replacement for the thermal-grown SiO_2 dielectric. Nevertheless, process optimization and detailed reliability data of these novel materials need to be established before they can be confidently accepted into mass production.

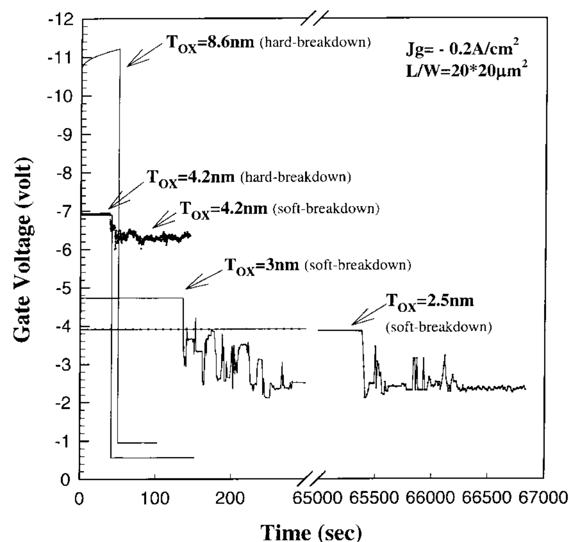

Fig. 3. Typical voltage–time curves for constant-current stressing measurements. The oxide thickness ranges from 8.6 to 2.5 nm. Soft-breakdown occurs when T_{ox} is scaled to 4.2 nm and dominates exclusively when T_{ox} is below 3 nm.

3. Breakdown characteristics

3.1. Occurrence of soft-breakdown

Breakdown characteristics of ultrathin gate oxides are discussed in this section. It was observed that when the oxide is thinner than 6 nm, an anomalous failure mode may be induced during high electric field stressing [45,46]. Specifically, thin gate oxide sometimes exhibits a significant leakage current increase accompanying a characteristic 'noisy' or fluctuating leakage current [47,48]. In contrast to the conventional 'hard breakdown' (HBD), this new breakdown phenomenon is named soft-breakdown (SBD), quasi-breakdown or partial-breakdown. Its occurrence complicates oxide reliability evaluation. Fig. 3 shows typical V–t curves during charge-to-breakdown (Q_{bd}) measurements using constant current stress, which is a well-known and widely accepted method for evaluating oxide reliability, for various gate oxide thickness. The abrupt drop in applied voltage after a certain period indicates the occurrence of oxide breakdown. It can be seen that the magnitude of post-breakdown voltage for SBD and HBD events is quite different. While the post-breakdown voltage after HBD is around 1 V or less, the voltage after SBD can be more than 1 V of magnitude. Moreover, the SBD events depict the characteristic 'noisy' behavior with fluctuating voltage, accompanying by an increase in non-switching $1/f$ noise and random telegraph noise after soft-breakdown [49]. Such

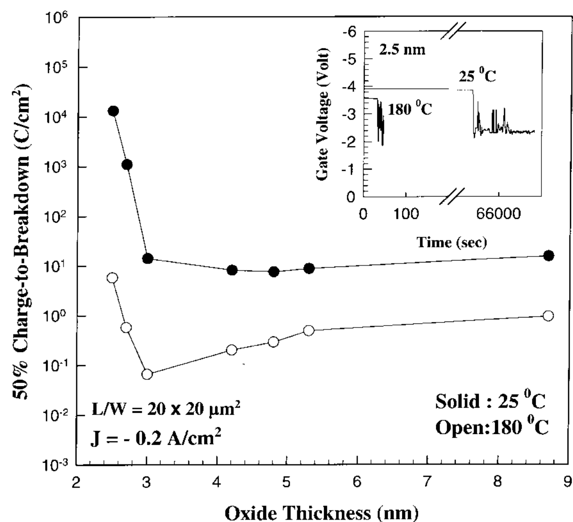

Fig. 4. 50% Q_{bd} as a function of oxide thickness measured at 25°C (solid circle) and 180°C (open circle) under gate injection polarity at a constant current of −0.2 A/cm^2. The area of the capacitor is 4×10^{-6} cm^2. Insert shows typical V–t curves of Q_{bd} tests on 2.5 nm oxide at 25°C and 180°C.

behaviors could be ascribed to on/off switching events of one or more local conduction spots [48].

3.2. Oxide thickness dependence on Q_{bd} characterization

The oxide breakdown characteristics show strong thickness dependence, as is evidenced from Fig. 3. For thicker oxides (e.g., 8.6 nm), only HBD is observed, while both SBD and HBD events are induced in oxide with intermediate thickness (e.g., 4 nm). For ultrathin oxide (e.g., 2.5 nm), SBD is found to dominate exclusively the breakdown events [50]. Moreover, for even thinner oxide (< 2 nm), due to the extremely large DT current, the voltage drop after SBD is very small, and may not be noticeable. Therefore, it becomes very difficult to detect oxide breakdown from the V–t curves [4]. Fig. 4 shows the 50% Q_{bd} values, measured at 25°C and 180°C, as a function of oxide thickness. At room temperature, it is found that Q_{bd} of 2.6 nm-thick oxide is about three orders of magnitude higher than that of thicker oxides. Such 'turn-around' behavior indicates that oxides show higher tolerance to DT current since negligible energy is deposited inside the oxide layer, comparing to the F–N tunneling [47]. However, when temperature is raised to 180°C, Q_{bd} of 2.6 nm-thick oxide is only about one order of magnitude higher than that of thicker oxides. This implies a very significant temperature acceleration effect for ultrathin oxide under DT stressing. This suggests that more attention should be paid to burn-in tests as well other wafer processing steps that encounter elevated

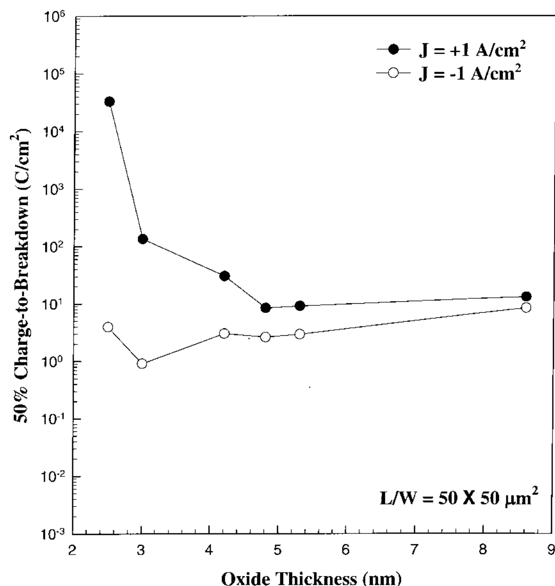

Fig. 5. 50% Q_{bd} measured at 25°C as a function of oxide thickness, both under substrate injection (+1 A/cm^2, solid circle) and gate injection (−1 A/cm^2, open circle). The area of the capacitor is 2.5×10^{-5} cm^2.

temperature in order not to jeopardize the gate oxide integrity (GOI) of ULSI devices employing ultrathin gate oxide [51].

The polarity dependence of Q_{bd}, which is the Q_{bd} difference between gate injection (V_g<0) and substrate injection (V_g > 0) stressing, is shown in Fig. 5. The stressing current density is fixed at 1 A/cm^2. It has been well documented in previous reports that the polarity dependence increases with decreasing oxide thickness (T_{ox}) for oxides thicker than 4 nm. This is ascribed to the different properties between the poly-Si/oxide and oxide/Si interfaces [52,53]. As shown in Fig. 5, as oxide is further scaled down, the polarity dependence becomes even more dramatic. This is mainly due to the rapid rise in Q_{bd} under substrate injection polarity as oxide is thinned down. Q_{bd} under gate injection polarity, however, remains relatively unchanged during F–N stressing.

3.3. Evaluation of ultrathin oxide reliability

As described above, the evaluation of ultrathin oxide reliability becomes much more complicated as oxide is scaled down. Recently, several studies have pointed out that oxide breakdown is a strong function of device geometry [54–56]. As such, the conventional use and its interpretation of Q_{bd} for comparing different MOS processes may lead to erroneous conclusion. For the same token, traditional use of large-area sample (i.e., capacitor) for evaluating oxide reliability

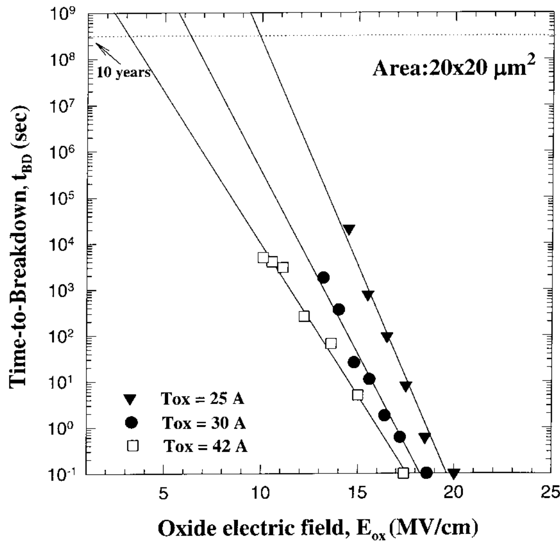

Fig. 6. Time-dependent dielectric breakdown (TDDB) characteristics vs. oxide electric field for various oxide thicknesses. Extrapolation of the data is used to predict a 10-year lifetime under maximum operating oxide field.

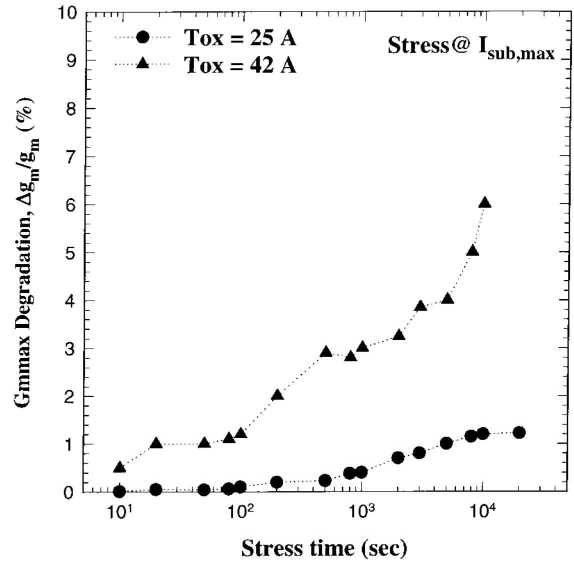

Fig. 7. Transconductance degradation after hot-carrier stressing for devices with 4.2 and 2.5 nm oxide. The hot-carrier stressing was performed under maximum substrate current condition.

may also lead to erroneous conclusion for device level applications [56]. It is also reported that the oxide degradation by SBD may not significantly affect transistor's drain current characteristics but increase gate current and noise [4,47]. However, in more recent studies, it is reported that device can still suffer HBD failure if the channel length of the device is sufficiently small (i.e., 0.2 μm) [55]. Therefore, evaluation of ultrathin oxide reliability remains a critical concern for scaled oxides.

Since Q_{bd} tests is no longer a valid tool to evaluate ultrathin oxide reliability [56], the constant voltage stressing (CVS) method which represents a more realistic situation for practical applications may be more suitable for evaluating ultrathin oxide reliability [55]. Fig. 6 illustrates the TDDB characteristics for various oxide thicknesses (e.g., 4.2, 3.0 and 2.5 nm). Time-to-breakdown (T_{bd}) tests under different oxide voltages at high field stressing are often employed for predicting the oxide lifetime under normal operating field (e.g. 5 MV/cm). As shown in Fig. 6, TDDB improves with decreasing oxide thickness. This can be ascribed to reduced trapped charges as well as smaller interface states generation after electrical stress as oxide is scaled to direct-tunneling regime. By extrapolating the data from Fig. 6, an electric field of over 9 MV/cm at room temperature is projected for 10-year lifetime. It is worthy to note that oxide lifetime is strongly dependent on gate area [57]. While the total gate area on a chip is of the order of 0.1 A/cm^2 for future generation technologies, the projected lifetime from Fig. 6, therefore, may be overestimated. Nonetheless, one can still conclude that TDDB performance is significantly improved with scaled oxides.

Finally, hot-carrier induced oxide degradation has also received much attention for scaled oxides since

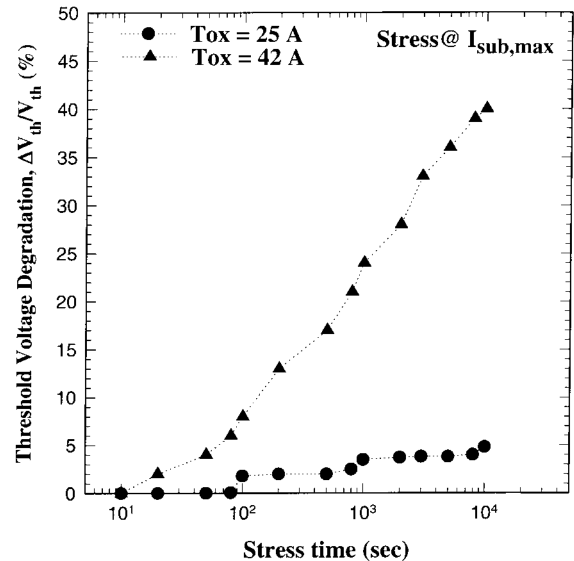

Fig. 8. Threshold voltage (V_{th}) shift after hot-carrier stressing for devices with 4.2 and 2.5 nm oxide. The hot-carrier stressing was performed under maximum substrate current condition.

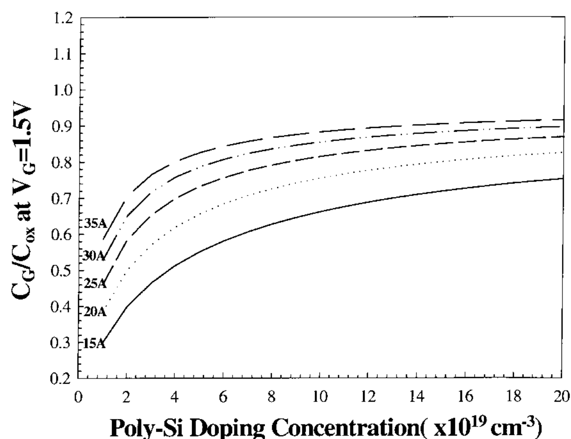

Fig. 9. The calculated gate capacitance to oxide capacitance ratios as a function of effective ploy gate doping for devices under inversion polarity. No QM effect was taken into consideration.

hot-carrier generation becomes more significant [58]. Figs. 7 and 8 depict hot carrier degradation results performed on 2.5 and 4.2 nm oxides. The hot carrier stress was performed with constant drain voltage of 3 V for 2.5 nm oxide and 4 V for 4.2 nm oxide, with appropriate gate bias to ensure maximum substrate current injection. These results confirm that the degradation in transconductance (Fig. 7) and threshold voltage (Fig. 8) are much smaller for the thinner oxide, consistent with data proposed in [58] (T_{ox} range: 1.5–3.8 nm). Thus ultrathin gate oxide do exhibit higher hot-carrier resistance, despite the fact that it is biased under a higher electric field stress due to a not proportionally scaled V_{dd}.

4. Poly-gate depletion effects

Poly depletion effects, caused by insufficient active dopant concentration near the poly/SiO_2 interface, become non-negligible as the miniaturization of devices proceeds into deep sub-micrometer regime. A lower effective surface electric field, due to additional voltage drop across the depletion layer, was reported to cause a significant reduction in drive current [59], difficulties in determining accurate oxide thickness [60], and overestimation of dielectric lifetime [61].

Significant degradation of inversion capacitance caused by poly-gate depletion was found to degrade device driving capability. The effect was more severe for devices with lower rapid thermal annealing (RTA) cycles and/or implant dose [59]. For *n*-MOS transistors with n^+ poly-Si gate, the effect can be explained by the physical model that As or P atoms tend to segregate to grain boundaries and become inactive [61]. Since the depletion width from the poly/SiO_2 interface increases if the oxide electric field increases, the PDE worsens for ultrathin oxide, as the supply voltage usually does not scaled proportionally. Thus, improvement in device performance by oxide scaling can not be achieved without resolving this issue. Fig. 9 shows the calculated gate capacitance to oxide capacitance ratios for devices under inversion polarity as a function of effective ploy gate doping, without taking the QM effect into consideration. The gate oxide thickness ranges from 1.5 to 3.5 nm. We can see that for typical effective doping concentration of 1×10^{20} cm^{-3}, gate capacitance plunges to only 80% of oxide capacitance for 3.5 nm oxide (i.e., 20% degradation). The degradation increases to almost 35% for 1.5 nm oxide. This trend indicates that drain current gain from thinner oxide is partly compensated by poly depletion effect. A heuristic solution to this problem is to enhance the thermal budget and/or implant dose. This, however, will cause adverse side effects. Since for deep submicron technologies, a very steep channel dopant profile and ultra-shallow S/D junction are required to suppress the so-called short-channel effects. Increasing thermal budget certainly jeopardizes the formation of steep doping profile. Furthermore, prolonged activation cycle and higher dopant implantation bring about disastrous penetration effect for *p*MOS transistors with p^+ gate. These factors reduce the available process windows for optimal process integration as the technology is further scaled down.

Recently, several alternative process technologies were proposed to reduce or eliminate altogether poly depletion effects [62–69]. Poly-Si_{1-x} Ge_x has been proposed as a very promising alternative gate material, since it suffers from less poly depletion problem and is also less susceptible to boron penetration [62,63]. The suggested Ge content for optimum performance is about 20% [62]. In addition, refractory metals such as TiN or WN_x have also been proposed as alternate gate materials due to its low gate resistance, and midgap work function [64–69]. Furthermore, being metallic, it is inherently immune to gate depletion problem. Nevertheless, more studies are needed regarding their process compatibility and impacts on device reliability before their acceptance by the ULSI industry.

5. Boron penetration

The effects of boron penetration into and through the gate oxides of *p*-channel devices are discussed in this section.

P^+-polysilicon gate for *p*-channel device is indispensable for deep-submicron CMOS technologies since it offers better short-channel behavior than conventional

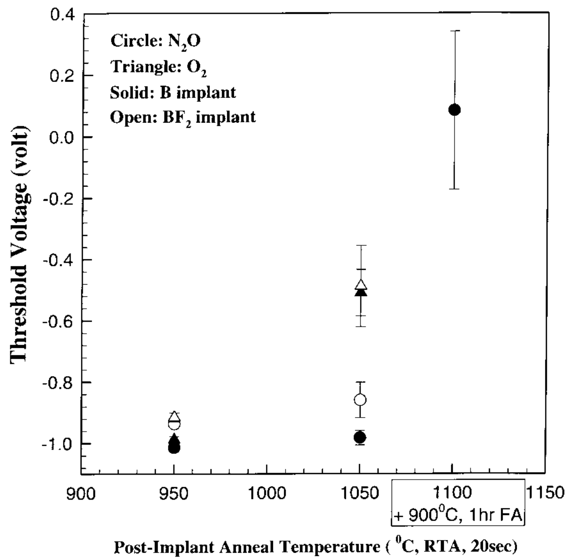

Fig. 10. Threshold voltage (V_{th}) as a function of post-implantation annealing condition for p-MOSFETs with pure oxides and N_2O-nitrided oxides. The oxide thickness is 4.2 nm. Both boron and BF_2 implants were activated for 20 s.

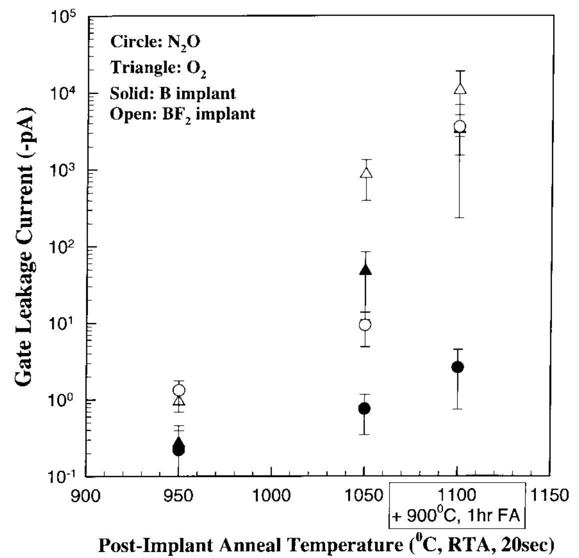

Fig. 11. Gate leakage current as a function of post-implantation annealing condition for p-MOSFETs with pure oxides and N_2O-nitrided oxides. The oxide thickness is 4.2 nm. Both boron and BF_2 implants were activated for 20 s. Gate leakage current was measured at a gate voltage $V_g = -2$ V under inversion polarity and a low drain bias $V_d = -0.1$ V.

buried-channel structure employing n^+-polysilicon gate. However, boron diffusion from the p^+-poly-Si gate into the thin gate oxide and the underlying channel region causes P-channel devices to depict flatband voltage shift, threshold voltage instability, low field mobility, drive current reduction, and gate oxide degradation [15,16], etc. The boron penetration effects may be modeled as the creation of a very thin sheet of negative charge at the Si/SiO_2 interface, which can be regarded as either a fixed negative charge in the gate oxide or a shallow p-type dopant layer in the silicon substrate [14]. Previous studies have shown that boron penetration becomes more severe with increasing anneal temperature [15]. As oxide thickness scales to direct tunneling regime, the situation also worsens. Since the thermal budget must be sufficient to achieve adequate gate dopant activation in order to avoid performance loss caused by gate depletion. These conflicting requirements make the process window between boron penetration and poly-gate depletion very stringent [70,71]. To resolve these issues, boron penetration effects and methods to minimize them have thus been widely studied.

Although it has been reported that fluorine can be used to improve gate oxide integrity for nMOS device, incorporation of fluorine from BF_2 implantation is known to exacerbate boron penetration [72,73]. It is also known that annealing in the presence of hydrogen will enhance boron diffusion [74]. Thus it is crucial to keep the content of fluorine and hydrogen in the process flow as low as possible to minimize boron penetration. Several techniques have also been proposed for suppressing boron penetration, and they could be divided into two categories: the first category is to lower the boron diffusivity in the poly-silicon gate. A typical example is to employ gate structure such as α-Si or stacked poly-Si gates [75–77]. Another example is the use of poly-Si_{1-x} Ge_x, which is shown to depict reduced boron penetration [62,63]. The second category is to improve the immunity of gate dielectric to boron penetration. A typical example is to introduce nitrogen into gate oxide by various processes (e.g., nitridation or nitrogen implantation), therefore, effectively suppress boron penetration and improve gate oxide integrity [78].

Fig. 10 depicts threshold voltage versus various post-implantation annealing conditions for p-MOSFETs with either pure or N_2O-nitrided oxides. The source/drain implant was performed with either boron or BF_2 implants. It is observed that N_2O-nitrided oxide exhibits excellent resistance to boron penetration except for samples under worst annealing condition (i.e. RTA@1100°C, 20 s + FA@900°C, 1 h). This is attributed to diffusion barrier enhancement by incorporation of nitrogen in gate oxide. In addition, it can be seen that using boron, instead of BF_2, can alleviate boron penetration by avoiding the so-called 'fluorine-enhanced' boron diffusion. The effects of

boron penetration on gate leakage current are shown in Fig. 11. Consistent with Fig. 10, severe boron penetration results in large leakage current. Samples with N_2O-nitrided oxide and boron implant depict the smallest leakage current, even under the worst annealing condition. By comparing Figs. 10 and 11, it appears that device performance (i.e., threshold voltage) is more sensitive to boron penetration than oxide leakage current for ultrathin gate oxides. To sum up, process optimization and the use of alternative materials for gate dielectrics or gate electrodes may be necessary for solving boron penetration problem encountered in future ultrathin gate oxide devices.

6. Plasma charging damage

Plasma charging effect, which may lead to severe oxide degradation and profile distortion during processing, has become one of major reliability concerns in ULSI manufacturing since the late 80s [19–27]. This can be attributed to several reasons: (1) oxides become more susceptible to charging damage as T_{ox} is scaled below 10 nm. (2) The number of plasma steps employed in wafer fabrication increases dramatically as the chip functionality and complexity advance. (3) In order to improve the throughput or to meet the critical requirements of deep-submicron manufacturing, process tools with high-density plasma (HDP) reactors for etching and deposition steps are widely used. These process steps may potentially aggravate the extent of charging.

6.1. Causes for plasma charging damage

It is well known that plasma exposure may cause degradation of device performance and decrease device yield and reliability. In general, many processing steps including polysilicon etch [79–81], ion implantation [82], dielectric deposition, oxide contact and via etch [83], metal interconnect etch [84], and resist ashing [85] may each contribute to device damage. Damage could happen by the synergistic effect of ion bombardment [86], charging due to plasma non-uniformity [87–89], contamination [90], and ultraviolet radiation [91]. Here, we focus on charging damage. Charge imbalance is the main cause responsible for plasma charging damage. The local ion and electron fluxes are out of balance due to charge imbalance, and result in charge built-up. When voltage due to charge built-up is sufficiently large, F–N tunneling occurs. Current collected by the antenna structure is channeled through the thin gate oxide by F–N tunneling. Under such situations, electron current injected into the oxide may deposit energy in the oxide and lead to trap creation and interface state generation. Consequently, gate oxide integrity is degraded. However, the damage depends on many factors from different process conditions and device applications.

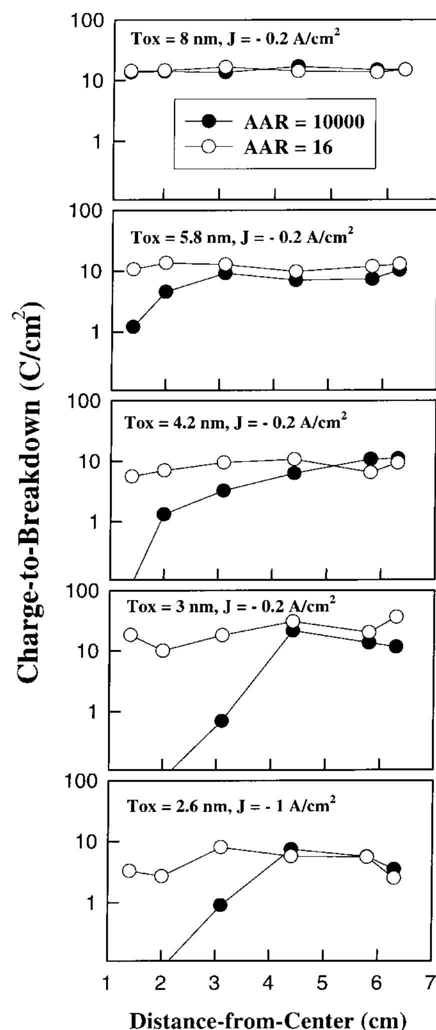

Fig. 12. Position dependence of Q_{bd} for various antenna ratios with oxide thickness ranging from 8 to 2.6 nm.

Fig. 12 shows the Q_{bd} results as a function of device location and antenna area ratio for oxides with thickness ranging from 8.7 to 2.5 nm. Charging damage is induced by a photoresist ashing step after wet metal pad definition. For devices with large antenna area ratio (AAR, e.g., 10K), significant damage begins to appear at the wafer center as oxide thickness is scaled below 6 nm. For oxide thinner than 4 nm, oxide breakdown is induced at the wafer center. These results suggest that plasma charging damage is strongly dependent on thickness and device location.

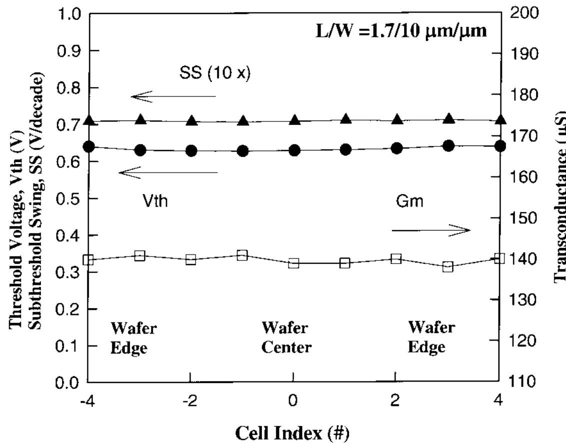

Fig. 13. Threshold voltage (V_{th}), subthreshold swing, and transconductance as a function of cell position. Antenna area ratio of the devices is 20K. Oxide thickness is 2.5 nm. No significant position dependence is observed across the wafer.

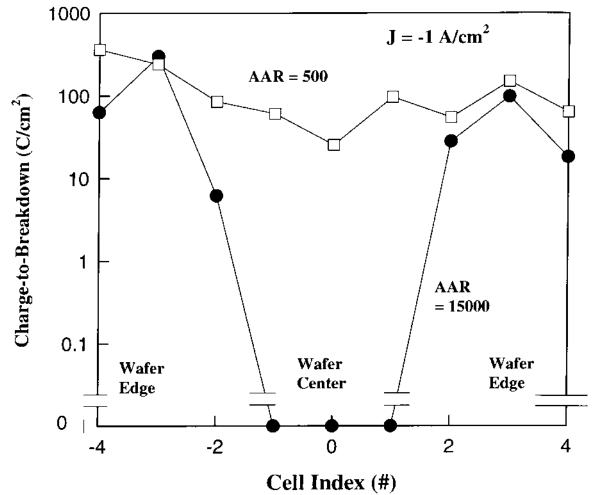

Fig. 14. Charge-to-breakdown (Q_{bd}) values as a function of cell position. Channel length and width of the measured transistors are 1.2 and 10 μm, respectively.

6.2. Evaluation of plasma charging damage

When entering sub-quarter micron era (i.e., $T_{ox}<6$ nm), the dependence of plasma charging damage on oxide thickness presents an important and controversial topic. Park and Hu studied the damage induced in oxides (2.2 nm$<T_{ox}<$7.7 nm) during metal and contact etching processes, and concluded that thinner oxide has superior immunity [21]. Alavi et al. showed that, as oxide is thinned down, the damage increases up to a point (~4 nm), and then decreases due to directing tunneling [22]. Similar trends were also reported by Noguchi et al. in investigating the electron shading effects [23]. On the other hand, the results of Bayoumi et al. ([24], T_{ox} range: 8–4 nm), Krishinan et al. ([25], T_{ox} range: 6–3.5 nm) and Chien et al. ([92], T_{ox} range: 8–4 nm) showed that the susceptibility to damage increases with decreasing oxide thickness. More recently, Krishnan et al. further indicated that severe damage could be induced in gate oxide as thin as 2.1 nm under certain inductively coupled plasma (ICP) metal etching conditions [93]. These different findings are understandable since process conditions and equipment configurations can be very different from one study to another. Besides, oxide degradation characteristics under high field stressing may change significantly as T_{ox} is thinned down. Thus different indicators (e.g., Q_{bd}, breakdown field, threshold voltage (V_{th}), etc.) that are used to characterize the damage by different investigators may lead to different outcomes.

Many test vehicles have been traditionally used in evaluating plasma-induced antenna effects, including Q_{bd} [94], initial-electron-trapping-rate (IETR) [95], relative linear transconductance reduction [96], hot-carrier-injection (HCI) [97–100], stress-induced leakage current (SILC) [101,102], and charge pumping (CP) [103,104], etc. However, as oxide is scaled into direct tunneling regime, some traditional measurements may become insensitive in detecting the charging damage. Fig. 13 depicts threshold voltage, subthreshold swing and transconductance of transistors as a function of cell location. We can see that, even with a large AAR value, these parameters vary only slightly across the wafer. In addition, no significant difference in transistor characteristics is found among transistors with various AAR values. Based on these results, one would tend to conclude that the plasma damage is negligible. However, significant damage is actually identified by the Q_{bd} measurements, as illustrated in Fig. 14. The insensitivity of transistor parameters to charging damage could be explained by the negligible surface state generation and bulk trapping after plasma process, which is intrinsic to ultrathin oxides. Therefore, one would have to conclude that some traditional methods are no longer sensitive for detecting charging damage for ultrathin oxides. Other methods, such as charge-to-breakdown, gate leakage current and noise measurement, are more sensitive and, therefore, more suitable for characterizing the plasma charging effects. In fact, for deep submicron devices, the situation may probably become more complicated. Thus, evaluation of plasma charging damage of ultrathin oxide device should be carefully examined.

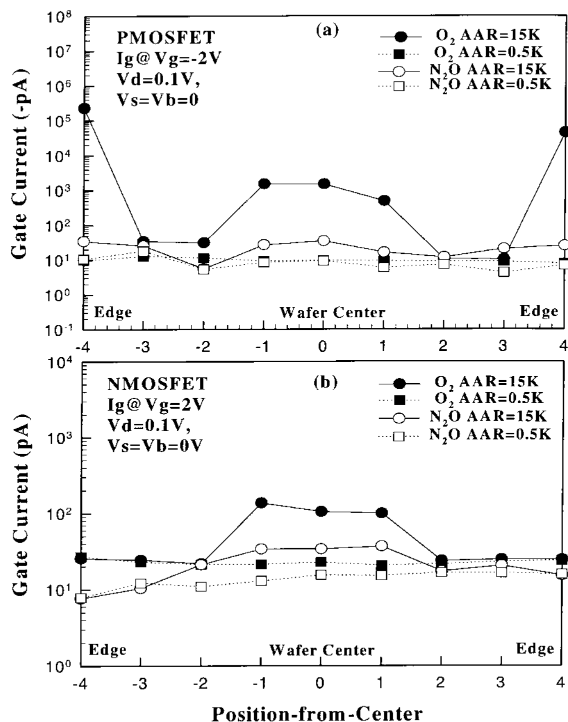

Fig. 15. Gate leakage current as a function of cell position for both pure and N_2O-nitrided oxides. Gate leakage current was measured at a gate voltage $V_g = |2|$ V under inversion polarity (i.e., (a) +2 V for *n*MOS, and (b) −2 V for *p*MOS) and a low drain bias $V_d = |0.1|$ V (i.e., (a) +0.1 V for *n*MOS, and (b) −0.1 V for *p*MOS). Transistors with two different antenna area ratios were measured.

6.3. Methods to improve plasma charging immunity

Since plasma charging damage could cause serious device degradation, several approaches are employed to alleviate it. These approaches include using protection diode [105,106], setting tight design rules for circuit, and introducing robust gate dielectrics [107]. Protection diode may be the most effective method to eliminate charging damage. However, additional layout/process and loss of integrity are its main drawbacks. The resort to design rule, on the other hand, limits the circuit layout flexibility. Finally, N_2O-nitrided oxide can be employed to effectively suppress the charging damage. In contrast with pure oxide, the leakage current characteristics of antenna devices with nitrided oxide are significantly improved, as shown in Fig. 15. Only slight increase in gate leakage current is observed on antenna devices with nitrided oxide. These improvements can be attributed to the formation of strong Si–N bonds replacing strained Si–O bonds and weak Si–H bonds [107]. The enhanced interface hardness of nitrided oxide results in improved gate oxide integrity. Therefore, N_2O-nitrided oxide is an extremely effective approach to improve the immunity to plasma damage in ultrathin oxides.

7. Conclusion

The continued scaling of ULSI technologies has demanded immediate attention to reliability issues of ultrathin oxides. In this work, we have reviewed recent status on the issues relating specially to the reliabilities of ultrathin gate dielectrics for present and future ULSI technologies. Several challenges facing the application of ultrathin gate oxides are discussed and can be summarized as followed:

1. The quantum mechanical tunneling current will eventually become a scaling limitation for the continued brute-force scaling of thermal silicon dioxide as gate dielectric. Alternative gate dielectrics with lower leakage current and comparable performance have to be introduced before the thermal oxide eventually becomes the show-stopper.
2. Ultrathin gate oxides exhibit superior TDDB characteristics. However, its increased dependence on temperature and polarity should be carefully taken into consideration in process integration, especially for processing steps that require high temperature.
3. Better understanding of breakdown mechanism of ultrathin oxide is essential for device lifetime prediction under normal operation condition, and for choosing proper reliability evaluation indicators.
4. The conflicting requirements in thermal cycle for poly depletion effect and boron penetration will severely restrict the process window. Alternative gate dielectrics and electrode materials may be inevitable in order to resolve this issue.
5. Plasma charging damage remains a major concern for ultrathin oxide reliability. More efforts need to be made to understand and minimize the charging damage.

References

[1] Momose HS, Ono M, Yoshitomi T, Ohguro T, Nakamura S, Saito M, Iwai H. Tunneling gate oxide approach to ultra-high current drive in small-geometry MOSFETs. IEDM Tech 1994:593.

[2] Matsuoka T, Kakimoto S, Nakano M, Kotaki H, Hayashida S, Sugimoto K, Adachi K, Morichita S, Uda K, Sato Y, Yamanaka M, Ougura T, Takagi J. Direct tunneling N_2O gate oxynitrides for low-voltage operation of dual gate CMOSFETs. IEDM Tech 1995:851.

[3] Kuroi T, Shimizu S, Ogino S, Teramoto A, Shirahata M, Okumura Y, Inuishi M, Miyoshi H. Sub-quarter-micron dual gate CMOSFETS with ultra-thin gate oxide of 2 nm. Symp. VLSI Technol Dig Tech 1996:210.
[4] Weir BE, Silverman PJ, Monroe D, Krisch KS, Alam MA, Alers GB, Sorsch TW, Timp GL, Baumann F, Liu CT, Ma Y, Huang D. Ultra-thin gate dielectrics: they breakdown, but do they fail? IEDM Tech 1997:73.
[5] Timp G, et al. Low leakage, ultra-thin gate oxides for extremely high performance sub-100 nm *n*-MOSFETs. IEDM Tech 1997:930.
[6] Xiang Q, Yeap G, Bang D, Song M, Ahmed K, Ibok E, Lin MR. Performance and reliability of sub-100 nm MOSFETs with ultra thin direct tunneling gate oxides. Symp VLSI Technol Dig Tech 1998:160.
[7] Sorsch T, et al. Ultra-thin, 1.0–3.0 nm, gate oxides for high performance sub-100 nm technology. Symp VLSI Technol Dig Tech 1998:222.
[8] Momose HS, Fujimoto R, Otaka S, Morifuji E, Yoshitomi T, Ohguro T, Saito M, Morimoto T, Katsumata Y, Iwai H. RF noise in 1.5 nm gate oxide MOSFETs and the evaluation of the NMOS LNA circuit integrated on a chip. Symp VLSI Technol Dig Tech 1998:96.
[9] Momose HS, Morifuji E, Yoshitomi T, Ohguro T, Saito M, Morimoto T, Katsumata Y, Iwai H. High frequency AC characteristics of 1.5 nm gate oxide MOSFETs. IEDM Tech 1996:105.
[10] Wann CHJ, Hu C. High endurance ultra-thin tunnel oxide for dynamic memory application. IEDM Tech 1995:867.
[11] Hu C. Gate oxide scaling limits and projection. IEDM Tech 1996:319.
[12] Lo SH, Buchanan DA, Taur Y, Han LK, Wu E. Modeling and characterization of n^+- and p^+-polysilicon-gate ultra-thin oxides (21-26A). Symp. VLSI Technol Dig Tech 1997:149.
[13] Wang SJ, Chen IC, Tigelaar HL. Effects of poly depletion on the estimate of thin dielectric lifetime. IEEE Electron Device Lett 1991;12:617.
[14] Pfiester JR, Baker FK, Mele TC, Tseng HH, Tobin PJ, Hayden JD, Miller JW, Gunderson CD, Parrillo LC. The effects of boron penetration on p^+ polysilicon gated PMOS devices. IEEE Trans Electron Devices 1990;37:1842.
[15] Sun JYC, Wong C, Taur Y, Hsu CH. Study of boron penetration through thin oxide with p^+ polysilicon gate. Symp VLSI Technol Dig Tech 1989:17.
[16] Hayashida H, Toyoshima Y, Suizu Y, Mitsuhashi K, Iwai H, Maeguchi K. Dopant redistribution in dual gate W-polyside CMOS and its improvement by RTA. Symp VLSI Technol Dig Tech 1989:29.
[17] Hao MY, Nayak D, Rakkhit R. Impact of boron penetration at p^+-poly/gate oxide interface on deep-submicron device reliability for dual-gate CMOS technologies. IEEE Electron Device Lett 1997;18:215.
[18] Cao M, Voorde PV, Cox M, Greene W. Boron diffusion and penetration in ultrathin oxide with poly-Si gate. IEEE Electron Device Lett 1998;19:291.
[19] Shone F, Wu K, Shaw J, Hokelek E, Mittal S, Haranahalli A. Gate oxide charging and its elimination for metal antenna capacitor and transistor in VLSI CMOS double layer metal technology. Symp VLSI Technol Dig Tech 1989:73.
[20] Wu IW, Koyanaki M, Holland S, Huang TY, Brouce RH, Anderson GB, Chiang A. Breakdown yield and lifetime of thin gate oxides in CMOS processing. J Electrochem Soc 1989;136:1638.
[21] Park D, Hu C. Plasma charging damage on ultrathin oxides. Int Symp Plasma Process Induced Damage (P2ID) 1997:15.
[22] Alavi M, Jacobs S, Ahmed S, Chern CH, McGregor P. Effects of MOS device scaling on process-induced gate charging. Int Symp Plasma Process Induced Damage (P2ID) 1997:7.
[23] Noguchi K, Tokashiki K, Horiuchi T, Miyamoto H. Reliability of thin gate oxide under plasma charging caused by topography-dependence electron shading effect. IEDM Tech 1997:441.
[24] Bayoumi A, Ma S, Langley B, Cox M, Tavassoli M, Diaz C, Cao M, Marcoux P, Ray G, Greene W. Scalability of plasma damage with gate oxide thickness. Int Symp Plasma Process Induced Damage (P2ID) 1997:11.
[25] Krishnan S, Dostalik WW, Brennan K, Aur S. Inductively coupled plasma metal etch damage to 35-60 A gate oxide. IEDM Tech 1996:731.
[26] McVittie JP. Process charging in ULSI: mechanisms, impact and solutions. IEDM Tech 1997.
[27] Krishnan S, Amerasekera A, Rangan S, Aur S. Antenna device reliability for ULSI processing. IEDM Tech 1998:601.
[28] Schuegraf KF, Park D, Hu C. Reliability of thin SiO_2 at direct-tunneling voltages. IEDM Tech 1994:609.
[29] Schuegraf KF, King CC, Hu C. Ultra-thin silicon dioxide leakage current and scaling limit. Symp VLSI Technol Dig Tech 1992:18.
[30] Chen K, Hu C, Fang P, Gupta A. Experimental confirmation of an accurate CMOS gate delay model for gate oxide and voltage scaling. IEEE Electron Device Lett 1997;18:275.
[31] Taur Y, Nowak EJ. CMOS devices below 0.1 μm: how high will performance go? IEDM Tech 1998:789.
[32] Han LK, Crowder S, Hargrove M, Wu E, Lo SH, Guarin F, Crabbe E, Su L. Electrical characteristics and reliability of sub-3 nm gate oxides grown on nitrogen implanted silicon substrate. IEDM Tech 1997:643.
[33] Tseng HH, et al. Application of JVD nitride gate dielectric to a 0.35 micron CMOS process for reduction of gate leakage current and boron penetration. IEDM Tech 1997:647.
[34] Khare M, Guo X, Wang XW, Ma TP. Ultra-thin silicon nitride gate dielectric for deep-submicron CMOS devices. Symp VLSI Technol Dig Tech 1997:51.
[35] Tseng HH, O'Meara DL, Tobin PJ, Wang VS, Guo X, Hegde R, Yang IY, Gilbert P, Cotton R, Hebert L. Reduced gate leakage current and boron penetration of 0.18 μm 1.5 V MOSFETs using integrated RTCVD oxynitride gate dielectric. IEDM Tech 1998:793.
[36] Momiyama Y, et al. Ultra-thin Ta_2O_5/SiO_2 gate insula-

tor with TiN gate technology for 0.1 μm MOSFETs. Symp VLSI Technol Dig Tech 1997:135.
[37] Kim HS, Gilmer DC, Campbell SA, Polla DL. Leakage current and electrical breakdown in metal-organic chemical vapor deposited TiO_2 dielectrics on silicon substrates. Appl Phys Lett 1996;69(25):3860.
[38] Song SC, Luan HF, Chen YY, Gardner M, Fulford J, Allen M, Kwong DL. Ultra thin (<20A) CVD Si_3N_4 gate dielectric for deep-sub-micron CMOS devices. IEDM Tech 1998:373.
[39] Guo X, Ma TP, Tamagawa T, Halpern BL. High quality ultra-thin TiO_2/Si_3N_4 gate dielectric for giga scale MOS technology. IEDM Tech 1998:377.
[40] Park D, Lu Q, King TS, Hu C. $SiON/Ta_2O_5/TiN$ gate-stack transistor with 1.8 nm equivalent SiO_2 thickness. IEDM Tech 1998:377.
[41] Chatterjee A, et al. CMOS metal replacement gate transistors using tantalum pentoxide gate insulator. IEDM Tech 1998:777.
[42] Jeon Y, Lee BH, Zawadzki K, Qi WJ, Lucas A, Nieh R, Lee JC. Effect of barrier layer on the electrical and reliability characteristics of high-k gate dielectric films. IEDM Tech 1998:797.
[43] VanDover RB, Fleming RM, Schneemeyer LF, Alers GB, Werder DJ. Advanced dielectrics for gate oxide, DRAM and rf capacitors. IEDM Tech 1998:823.
[44] Manchanda L, et al. Gate quality doped high K films for CMOS beyond 100 nm: 3–10 nm Al_2O_3 with low leakage and low interface states. IEDM Tech 1998:605.
[45] Lee SH, Cho BJ, Kim JC, Choi SH. Quasi-breakdown of ultrathin gate oxide under high field stress. IEDM Tech 1994:605.
[46] Depas M, Nigam T, Heyns MM. Soft breakdown of ultra-thin gate oxide layers. IEEE Trans Electron Devices 1996;43:1499.
[47] Lin HC, Wang MF, Chen CC, Hsien SK, Chien CH, Huang TY, Chang CY, Chao TS. Characterization of plasma charging damage in ultra-thin gate oxides. In: Proc. 36th Int. Reliab. Phys. Symp. IRPS98. 1998. p. 312.
[48] Miranda E, Sune J, Rodriguez R, Nafria M, Aymerich X. Switching behavior of the soft breakdown conduction characteristics in ultra-thin (<5 nm) oxide MOS capacitors. In: Proc 36th Int Reliab Phys Symp IRPS98. 1998. p. 42.
[49] Sakura T, Utsunomiya H, Kamakura Y, Taniguchi K. A detailed study of soft- and pre-soft-breakdowns in small geometry MOS structures. IEDM Tech 1998:183.
[50] Chen CC, Lin HC, Chang CY, Chien CH, Hsien SK, Wang MF, Huang TY, Chao TS, Liang MS. Plasma charging damage in ultrathin (8.6∼2.5 nm) gate oxides. International Electron Devices and Materials Symposia 1998:34.
[51] Chen CC, Lin HC, Chang CY, Chien CH, Huang TY, Liang MS. Temperature-accelerated dielectric breakdown in ultra-thin gate oxides. Appl Phys Lett 1999;74(24):3708–3710.
[52] Hokari Y. Stress voltage polarity dependence of thermally grown thin gate oxide wearout. IEEE Trans Electron Devices 1988;35:1299.
[53] Han LK, Bhat M, Wristers D, Fulford J, Kwong DL. Polarity dependence of dielectric breakdown in scaled SiO_2. IEDM Tech 1994:617.
[54] Crupi F, Degraeve R, Guido, Groeseneken, Nigam T, Maes HE. On the properties of the gate and substrate current after soft breakdown in ultra-thin oxide layers. IEEE Trans Electron Devices 1998;45:2329.
[55] Wu E, Nowak E, Aitken J, Abadeer W, Lan LK, Lo S. Structural dependence of dielectric breakdown in ultra-thin gate oxides and its relationship to soft breakdown modes and device failure. IEDM Tech 1998:187.
[56] Nigam T, Degraeve R, Groeseneken G, Heyns MM, Maes HE. Constant current charge-to-breakdown: still a valid tool to study the reliability of MOS structures. In: Proc 36th Intl Reliab Phys Symp IRPS98. 1998. p. 62.
[57] Stathis JH, DiMaria DJ. Reliability projection for ultra-thin oxides at low voltage. IEDM Tech 1998:167.
[58] Momose HS, Nakamura S, Ohguro T, Yoshitomi T, Saito M, Morimoto T, Katsumata Y, Iwai H. A study of hot-carrier degradation in *n*- and *p*-MOSFETs with ultra-thin gate oxides in direct-tunneling regime. IEDM Tech 1997:452.
[59] Yu B, Ju DH, Kepler N, King TJ, Hu C. Gate engineering for performance and reliability in deep-submicron CMOS technology. Symp VLSI Technol Dig Tech 1997:105.
[60] Buchanan DA, Lo SH. Reliability and integration of ultra-thin gate dielectrics for advanced CMOS. Microelectronic Engineering 1997;36:13.
[61] Moran S, Hurley PK, Mathewson A. Test structure for investigating activated doping concentrations in polycrystalline silicon. In: Proc IEEE Int Conf on Microelectronic Test Structures, March. 1996. p. 217.
[62] Lee WC, King TJ, Hu C. Optimized poly-$Si_{1-x}Ge_x$-gate technology for dual gate CMOS application. Symp VLSI. Technol Dig Tech 1998:190.
[63] Ponomarev YV, Salm C, Schmitz J, Woerlee PH, Stolk PA, Gravesteijn DJ. Gate-workfunction engineering using poly-(Si,Ge) for high performance 0.18 μm CMOS technology. IEDM Tech 1997:829.
[64] Chatterjee A, et al. Sub-100 nm gate length metal gate NMOS transistors fabricated by a replacement gate process. IEDM Tech. 1997:821.
[65] Hu JC, Yang H, Kraft R, Rotondaro AL, Hattangady S, Lee WW, Chapman RA, Chao CP, Chatterjee A, Hanratty M, Rodder M, Chen IC. Feasibility of using W/TiN as metal gate for conventional 0.13 μm CMOS technology and beyond. IEDM Tech 1997:825.
[66] Lee BH, Sohn DK, Park JS, Han CH, Huh YJ, Byun JS, Kim JJ. In-situ barrier formation for high reliable W/barrier/poly-Si gate using denudation of WN_x on polycrystalline Si. IEDM Tech 1998:385.
[67] Hiura Y, Azuma A, Nakajima K, Akasaka Y, Miyano K, Nitta H, Honjo A, Tsuchida K, Toyoshima Y, Suguro K, Kohyama Y. Integration technology of polymetal (W/WSiN/poly-Si) dual gate CMOS for 1Gbit DRAMs and beyond. IEDM Tech 1998:389.
[68] Wakabayashi H, Yamamoto T, Yoshida K, Soda E, Tokunaga KI, Mogami T, Kunio T. An ultra-low resistance and thermally stable W/pn-poly-Si gate CMOS

technology using Si/TiN buffer layer. IEDM Tech 1998:393.

[69] Ohnishi K, et al. Improving gate oxide integrity (GOI) of a W/WN_x/dual-poly Si stacked-gate by using wet-hydrogen oxidation in 0.14-μm CMOS devices. IEDM Tech 1998:397.

[70] Aoyama T, Suzuki K, Tashiro H, Tada Y, Arimoto H. Flat-band voltage shifts in *p*-MOS devices caused by carrier activation in p^+-polycrystalline silicon and born penetration. IEDM Tech 1997:627.

[71] Tuinhout HP, Montree AH, Schmitz J, Stolk PA. Effects of gate depletion and boron penetration on matching of deep submicron CMOS transistors. IEDM Tech 1997:631.

[72] Sung JJ, Lu CY. A comprehensive study on p^+ polysilicon-gate MOSFET's instability with fluorine incorporation. IEEE Trans Electron Devices 1990;37:2312.

[73] Tseng HH, Oriowski M, Tobin PJ, Hance RL. Fluorine diffusion on a polysilicon grain boundry network in relation to boron penetration from p^+ gates. IEEE Electron Device Lett 1992;13:14.

[74] Grove AS, Leistiko O, Sah CT. Redistribution of acceptor and donor impurities during thermal oxidation of silicon. J Appl Phys 1964;35:2695.

[75] Lin CY, Juan KC, Chang CY, Pan FM, Chou PF, Hung SF, Chen LJ. A comprehensive study of suppression of boron penetration by amorphous-Si gate in p^+-gate PMOS devices. IEEE Trans Electron Devices 1995;42:2080.

[76] Wu SL, Lee CL, Lei TF. Suppression of boron penetration into an ultra-thin gate oxide (<7 nm) by using a stacked-amorphous-silicon (SAS) film. IEDM Tech 1993:329.

[77] Lin YH, Lai CS, Lee CL, Lei TF, Chao CS. Nitridation of the stacked poly-Si gate to suppress the boron penetration in PMOS. IEEE Electron Device Lett 1995;16:248.

[78] Han LK, Bhat M, Wristers D, Wang HH, Kwong DL. Recent developments in ultra thin oxynitride gate dielectrics. Microelectronic Engineering 1995;28:89.

[79] Gabriel Calvin T. Gate oxide damage from polysilicon etching. J Vac Sci Technol B 1991;9(2):370.

[80] Casta'n E, de Dios A, Bailo'n L, Barbolla J, Cabruja E, Dominguez C, Lora-Tamayo E. Characterization of the electrical damage due to polysilicon RIE (SF_6 + Cl_2 plasma). Etching J Electrochem Soc 1992;139(1):193.

[81] Greene WM, Kruger JB, Kooi G. Magnetron etching of polysilicon: electrical damage. J Vac Sci Technol B 1991;9(2):366.

[82] Kenji Yoneda, Kenji Hagiwara, Yasihiro Todokoro. The influence of medium dose ion implantation on the reliability of thin gate oxide. J Electrochem Soc 1995;142(5):1619.

[83] Cavin Gabiel, Subhas Bothra, Milind, Tim Herbst. Plasma process-induced charging through contacts and vias. Proc of VMIC 1995:394.

[84] Tsui Bing-Yue, Liu Shunn-Her, Geeng-Lih, Ho Jau-Hwang, Chang Chia-Haur, Lu Chih-Yuan. Recovery phenomenon and local field sensitivity on wafer charge-up effect of magnetically enhanced reactive ion etch system. IEEE Electron Device Lett 1995;16:64.

[85] Fang S, Murakawa S, McVittie JP. Modeling of oxide breakdown from gate charging during resist ashing. IEEE Trans Electron Device 1994;41(10):1848.

[86] Felch SB, Salimian S, Hodul DT. J Vac Sci Technol B 1992;10:1320.

[87] Gabriel CT, Mcvittie JP. Solid State Technol 1992;June:81.

[88] Fang S, McVittie JP. IEEE Electron Device 1992;ED-13:288.

[89] Samukawa S. Jpn J Appl Phys 1990;29:134.

[90] Yapsir AS, Fortuno-Wiltshire G, Gambino JP, Kastl RH, Parks CC. J Vac Sci Technol B 1992;6:268.

[91] Buchanan DA, Fortuno-Wiltshire G. J Vac Sci Technol A 1991;9:804.

[92] Chien CH, Chang CY, Lin HC, Chang TF, Chiou SG, Chen LP, Huang TY. Resist-related damage on ultra-thin gate oxide during ashing. IEEE Electron Device Lett 1997;18:33.

[93] Krishnan S, Rangan S, Hattangaty S, Xing G, Bernnan K, Rodder M, Ashok S. Assessment of charge-induced damage to ultra-thin gate MOSFETs. IEDM Tech 1997:445.

[94] Eriguchi Koji, Uraoka Yukihara, Nakagawa Hideo, Tamaki Tokuhiko, Kuboto Masafumi, Nomura Noboru. Quantative evaluation of gate oxide damage during plasma processing using antenna-structure capacitors. Jpn J Appl Phys 1994;33:83.

[95] Cheung KP. An efficient method for plasma-charging damage measurement. IEEE Trans Electron Device Lett 1994;15(11):460.

[96] Shin H, King C-C, Horiuchi T, Chenming Hu. Thin oxide charging current during plasma etching of aluminum. IEEE Electron Device Lett 1991:404.

[97] Doyle B, Bourcerie M, Marchetaux J-C, Boudou A. Interface state creation and charge trapping in the medium to high gate voltage range during hot carrier stressing of *n*-MOS transistors. IEEE Trans Electron Device 1990;37:744.

[98] Mistry KR, Fishbein BJ, Doyle BS. Effect of plasma-induced charging damage on n-channel and p-channel MOSFET hot carrier reliability. In: IEEE Int Reliab Phys Symposium. 1994. p. 42.

[99] Lee YH, Yau L, Chau R, Hansen E, Sabi B, Hui S, Moon P, Vandentop C. Correlation of plasma process induced charging with Fowler–Nordheim stress in P- and N-channel transistors. IEEE IEDM Tech 1992:65.

[100] Kin P. Cheung. A new method to monitor gate-oxide reliability degradation. Symp VLSI Technol 1995:83.

[101] Lin HC, Chien CH, Huang TY. Characterization of antenna effect by nondestructive gate current measurement. Jpn J Appl Phys 1996;35:L1044.

[102] Lee YH, Wu K, Sery G, Mielke N, Lin W. In: Third Int Symp P2ID. 1998. p. 7.

[103] Rangan S, Krishnan S, Ashok S. Process-induced damage—a study of hydrogen and deuterium passivation. In: Third Int Symp P2ID. 1998. p. 213.

[104] Ma ZJ, Shin H, Ko PK, Hu C. Effects of plasma charging damage on the noise performance of thin-oxide MOSFET's. IEEE Electron Device Lett 1994;15:224.

[105] Shin H, Ma ZJ, Hu C. Impact on plasma charging damage and diode protection on scaled thin oxide. IEDM Tech 1993:467.

[106] Zheng S, Park D, Bui N, Hu C, Yue J. A quick experimental technique in estimating the cumulative plasma charging current with MOSFET and determining the reliability of the protection diode in the plasma ambient. In: First Int Symp P2ID. 1996. p. 27.

[107] Joshi AB, Hann R, Chung L, Bhat M, Cho TH, Min BW, Kwong DL. Suppressed process-induced damage in N_2O-annealed SiO_2 gate dielectrics. IEEE Int Reliab Phys Symp 1995:156.