

# Enhancement of Integrity of Polysilicon Oxide by Using a Combination of N<sub>2</sub>O Nitridation and CMP Process

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**Abstract**—This work prepares and demonstrates, for the first time, a high-quality polysilicon oxide, by combining N<sub>2</sub>O nitridation and Chemical Mechanical Polishing (CMP) process. Our results demonstrate that capacitors with this process have an improved  $Q_{bd}$  (charge-to-breakdown) due to the planar surface and more concentrated nitrogen at the interface of polysilicon oxide.

## I. INTRODUCTION

TO obtain adequate data retention in nonvolatile memories, basic requirements of polysilicon oxides are low-leakage current, high dielectric strength, and high charge-to-breakdown [1]–[3]. However, the integrity of polysilicon oxide heavily depends on the surface morphology of polysilicon-oxide/polysilicon interface and the oxidants that were used for growth or post-oxidation annealing [4]–[6]. Previous investigations have attempted to improve electric properties of polysilicon oxides grown or post-oxidation annealed in N<sub>2</sub>O ambient [4]–[6]. Incorporating nitrogen by using N<sub>2</sub>O leads to such an improvement. Meanwhile, other investigators have applied an adequately controlled Chemical Mechanical Polishing (CMP) process to improve the surface morphology of polysilicon [7], [8]. The planar surface morphology, after the CMP process, has been shown to result in an improved integrity of polysilicon oxide.

This work demonstrates, for the first time, growth of the polysilicon oxide combining N<sub>2</sub>O nitridation and CMP process. According to our results, a higher and more concentrated nitrogen profile is found at the polysilicon oxide interface. In addition, the surface morphology and the charge-to-breakdown are also significantly improved.

## II. EXPERIMENT

Samples were fabricated on p-type (100) silicon wafers which were oxidized to grow 2000 Å silicon dioxide films. A 3000 Å Poly-Si film, Poly-1, was deposited at 620 °C and

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doped by POCl<sub>3</sub> (with a sheet resistance of 50–70 Ω/□). Some of the Poly-Si films were polished by CMP technique [8], followed by cleaning in a scrubber and ultrasonic oscillator with NH<sub>4</sub>OH:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O (= 1:1:10) solution to remove the particles and metallic contamination. Next, an additional RCA clean process was performed. Polysilicon oxides were then grown in two oxidants, in dilute dry O<sub>2</sub> ambient (N<sub>2</sub>:O<sub>2</sub> = 6:1),  $T_{ox} = 13.6$  nm, at 900 °C, and in pure N<sub>2</sub>O ambient,  $T_{ox} = 13.8$  nm, at 900 °C. The samples having underwent N<sub>2</sub>O/O<sub>2</sub> oxidation but without CMP process are referred to as Non-CMP-N<sub>2</sub>O/Non-CMP-O<sub>2</sub>; whereas with the CMP process, they are referred to as CMP-N<sub>2</sub>O/CMP-O<sub>2</sub>. Subsequently, poly-2 was deposited and doped to a sheet resistance of 25–35 Ω/□ by POCl<sub>3</sub>. After defining poly-2 to form the capacitors, all samples were thermally oxidized to grow a 1000 Å-thick oxide using wet oxidation. Contact holes were opened, and then Al was deposited and patterned to form contacts to the poly-2 electrodes. The area of the capacitor is  $6 \times 10^{-4}$  cm<sup>2</sup>. The polysilicon oxide thicknesses were determined by using Keithley C-V measurement. Finally, electrical characteristics and constant current stress were performed using a HP4156 semiconductor parameter analyzer.

## III. RESULTS AND DISCUSSION

The surface morphology images of polysilicon-oxide/polysilicon interface before and after oxidation were investigated by AFM (atomic force microscope) and depicted in Fig. 1(a)–(e). To reveal the real surface of the lower polysilicon layers, dilute HF solution was used to strip the oxides after the thermal oxidation. The original surface without CMP before oxidation was shown in Fig. 1(a). For the Non-CMP polysilicon after oxidation, rougher and nonuniform interfaces were observed and shown in Fig. 1(b) and (d) for Non-CMP-O<sub>2</sub> and Non-CMP-N<sub>2</sub>O samples, respectively. According to these figures, the roughness, root-mean-square,  $R_q$ , after oxidation in dilute O<sub>2</sub> ambient ( $\sim 5.4$  nm) was slightly larger than that in N<sub>2</sub>O ambient ( $\sim 4.4$  nm) where the original surface without CMP before oxidation was  $\sim 4.3$  nm. For the CMP samples, smoother and uniform surfaces were formed and shown in Fig. 1(c) and (e) for the CMP-O<sub>2</sub> ( $R_q \sim 1.8$  nm) and CMP-N<sub>2</sub>O ( $R_q \sim 1.7$  nm), respectively.

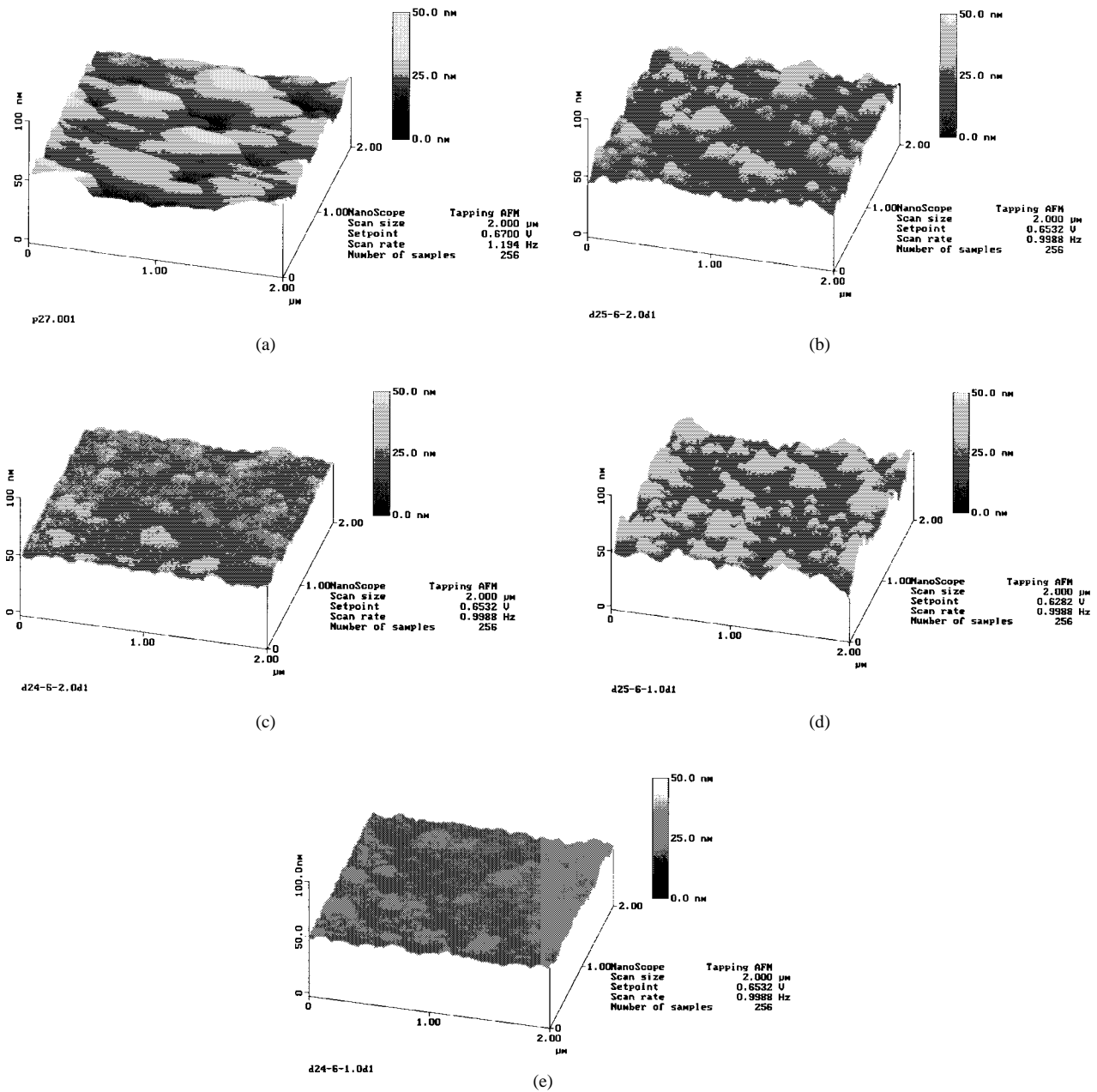


Fig. 1. Surface image measured by AFM for (a) without CMP before oxidation (b) Non-CMP-O<sub>2</sub>, (c) CMP-O<sub>2</sub>, (d) Non-CMP-N<sub>2</sub>O, (e) CMP-N<sub>2</sub>O.

Fig. 2 displays the SIMS depth profiles of nitrogen for these four samples. It indicates that nitrogen was indeed incorporated into the polysilicon oxides after oxidation in N<sub>2</sub>O ambient. Moreover, the nitrogen profile of the CMP-N<sub>2</sub>O sample exhibits the narrowest and largest peak distribution among these four samples. It is suggested that during the high-temperature thermal oxidation, the oxidant may diffuse deeper through the grain boundary in the rougher (or nonuniform) surface and has broader and lower nitrogen distribution.

Fig. 3(a) and (b) present the charge-to-breakdown (Q<sub>bd</sub>) characteristics of these four samples under +10 mA (+V<sub>g</sub>) and -10 mA (-V<sub>g</sub>) gate injection. According to Fig. 3(a), the Non-CMP-N<sub>2</sub>O under +V<sub>g</sub> gate injection was only slightly better than that of the O<sub>2</sub> sample while nearly the same under -V<sub>g</sub> gate injection as grown in dilute O<sub>2</sub> ambient. By

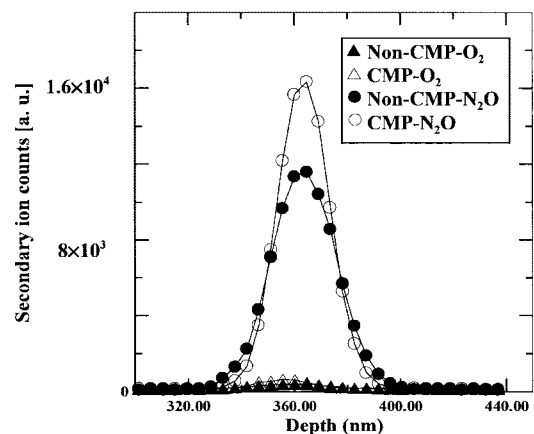
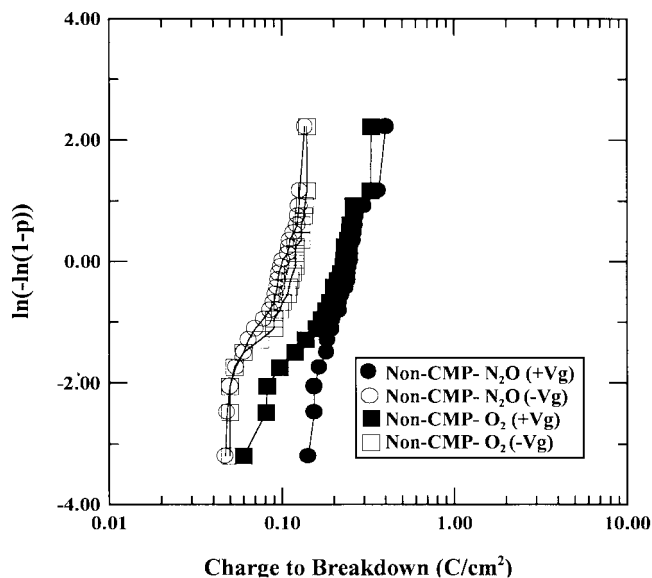
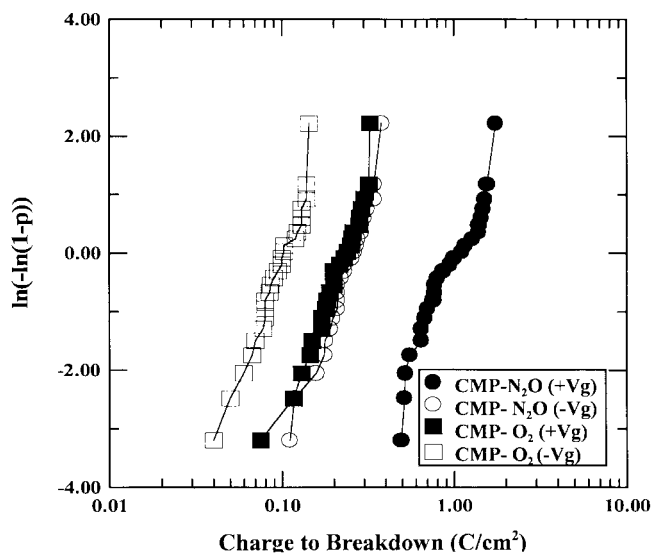


Fig. 2. SIMS depth profile of nitrogen of Non-CMP-N<sub>2</sub>O/O<sub>2</sub>, CMP-N<sub>2</sub>O/O<sub>2</sub>, respectively.



(a)



(b)

Fig. 3. (a) Charge-to-breakdown of polysilicon oxide for samples Non-CMP-N<sub>2</sub>O and Non-CMP-O<sub>2</sub>. (b) Charge-to-breakdown of polysilicon oxide for samples CMP-N<sub>2</sub>O and CMP-O<sub>2</sub>.

using CMP process, the  $Q_{bd}$  of oxide grown in N<sub>2</sub>O ambient, both under  $+V_g$  and  $-V_g$  gate injections, were markedly higher than those of O<sub>2</sub> samples, as shown in Fig. 3(b). Also, this figure obviously reveals that the  $Q_{bd}$  of CMP-N<sub>2</sub>O/CMP-O<sub>2</sub> samples under  $+V_g$  injection was significantly improved over the corresponding samples shown in Fig. 3(a)

due to the planar surface morphology and reduced interface roughness. Hence, the above results, indicate that adding an adequately controlled CMP process not only improved the surface roughness of the Poly-1 but also increased the concentration of the incorporated nitrogen in N<sub>2</sub>O ambient. We believe that although incorporating nitrogen can improve the  $Q_{bd}$  of oxide, the rough surface reduces this effect for the Non-CMP samples under both  $+V_g$  and  $-V_g$  gate injection. By adding the CMP process, the “bumps” on the Poly-1 surface [1] are removed and a smooth surface can be obtained. Moreover, this planar surface increases the concentration of the incorporated nitrogen at the interface in N<sub>2</sub>O ambient. Consequently, combining N<sub>2</sub>O nitridation and CMP process allows us to achieve an optimized polysilicon oxide.

#### IV. CONCLUSIONS

This work demonstrates, for the first time, that the integrity of the polysilicon oxide can be improved by using a combination of N<sub>2</sub>O nitridation and CMP process. The surface of polysilicon becomes smoother by using the CMP process, resulting in a concentrated and increased nitrogen profile at the interface after N<sub>2</sub>O nitridation.

#### REFERENCES

- [1] J. C. Lee and C. Hu, “Polarity asymmetry of oxides grown on polycrystalline silicon,” *IEEE Trans. Electron Devices*, vol. 35, p. 1063, July 1988.
- [2] L. Faraone, R. D. Vibronek, and J. T. McGinn, “Characterization of thermally oxidized n<sup>+</sup> polycrystalline silicon,” *IEEE Trans. Electron Devices*, vol. ED-32, p. 577, Mar. 1985.
- [3] S. L. Wu, C. Y. Chen, T. Y. Lin, C. L. Lee, T. F. Lei, and M. S. Liang, “Investigation of the polarity asymmetry on the electrical characteristics of thin polyoxides grown on n<sup>+</sup> polysilicon,” *IEEE Trans. Electron Devices*, vol. 44, p. 153, Jan. 1997.
- [4] F. C. Jong, T. Y. Huang, T. S. Cho, H. C. Lin, L. Y. Leu, K. Young, C. H. Lin, and K. Y. Chiu, “Improved flash cell performance by N<sub>2</sub>O annealing of interpoly oxide,” *IEEE Electron Device Lett.*, vol. 18, p. 343, July 1997.
- [5] C. S. Lai, T. F. Lei, and C. L. Lee, “The characteristics of polysilicon oxide grown in pure N<sub>2</sub>O,” *IEEE Trans. Electron Devices*, vol. 43, p. 326, 1996.
- [6] P. Candelier, F. Mondon, B. Guillaumot, G. Reimbold, and F. Martin, “Simplified 0.35- $\mu$ m flash EEPROM process using high-temperature oxide (HTO) deposited by LPCVD as interpoly dielectrics and peripheral transistors gate oxide,” *IEEE Electron Devices Lett.*, vol. 16, p. 385, Sept. 1995.
- [7] T. F. Lei, J.-Y. Cheng, S. Y. Shiau, T. S. Chao, and C. S. Lai, “A novel polysilicon oxide grown on chemical-mechanical polished polysilicon film,” *IEEE Electron Device Lett.*, vol. 18, p. 306, July 1997.
- [8] ———, “Characteristics of polysilicon oxides thermally grown and deposited on the polished polysilicon films,” *IEEE Trans. Electron Devices*, vol. 45, p. 912, Apr. 1998.