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# Process Optimization and Integration for Silicon Oxide Intermetal Dielectric Planarized by Chemical Mechanical Polish

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The chemical mechanical planarization (CMP) characteristics of silicon oxide films are studied systematically for the optimization of planarization for intermetal dielectric (IMD) processes. By way of orthogonal array experimental design, the influences of physical parameters during CMP upon the polishing behaviors of silicon oxide dielectric materials are investigated. Polishing results with a removal rate greater than 200 nm/min and a within-wafer nonuniformity less than 4% can be achieved and an optimized polish process is derived from parametric experiments, which are based on the summarized trends from orthogonal array experimental results. The optimized polish process is applied to planarize patterned IMD wafers with different metal line pitch and IMD thickness. Incorporating the IMD geometric factors and CMP polishing performance, a rule including the integral nonuniformity, thickness of dielectric, efficiency of planarization, geometry of device, removal rate, and its variation for CMP time estimation (INTEGRATE) is proposed to approximate the required IMD thickness and CMP polish time for ImD process integration. High efficiency of the planarization process and excellent planarity are both achieved based on the rule of INTEGRATE.
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As the trend toward shrinking design rules for ultralarge scale integrated circuits (ULSI) continues, the requirements of the planarization process become more and more stringent due to concerns over narrowing lithographic process latitudes in the presence of ever-reducing depth of focus. Among the planarization technologies, chemical mechanical polishing (CMP) is the only technique that is capable of achieving global planarization across the lithographic field, and therefore becomes one of the most important ULSI process technologies for the 0.25 μm generation and beyond.[1]

Despite its popularity and widespread applications, the practice of CMP still remains at an empirical level owing to the numerous process parameters involved and the lack of a systematic methodology for characterizing and optimizing the process. For instance, for the planarization of intermetal dielectric (IMD) through CMP, process engineers are often confronted with the challenge of determining the thickness of deposited IMD layer that will be removed subsequently by the CMP step. This problem is further complicated when it comes to optimize the numerous CMP process parameters in order to broaden the process latitude, while maintaining a high enough planarization efficiency in the presence of varying pattern densities that would lead to over- or underpolishing of the dielectrics within a chip.

To investigate the influence of each parameter over a wide range of variables and to reduce the sample size under such a complex variable experiments, this study utilized the standard L-25 orthogonal array experiments design[2,3] to derive the characteristic trends of removal rate and within-wafer nonuniformity (WIWNU) against various CMP process parameters. With the L-25 orthogonal array experimental setting, removal rate and WIWNU values may be biased if certain polishing parameters dominate the output results or there exists interaction between parameters. To correct this, parametric experiments based on the summary from orthogonal array results are performed afterward to eliminate the side effects. This also provides precise numerical data of each parameter for the decision of optimal value for subsequent experimental setting. The optimal polishing conditions derived above are then adopted to planarize the intermetal dielectric oxide films with various patterned metal pitches underneath to investigate the efficiency of planarization (%EOP). Based on the observation of the above experimental results, a rule including the integral nonuniformity, thickness of dielectric, efficiency of planarization, geometry of device, removal rate, and its variation for CMP polishing time estimation (INTEGRATE) is proposed to estimate the required dielectric thickness and polish time for the integration of IMD and CMP processes. Scanning electron microscopy (SEM) cross-sectional micrographs and chip level long scan profiles reveal the excellent global planarization achieved through the practice of the proposed INTEGRATE rule in this study.

## Experimental

First, the plasma-enhanced chemical vapor deposited (PECVD) silicon dioxide thin films were laid on 150 mm Si(100) wafers in a dual frequency PECVD reactor at 400°C and a pressure of 2.2 Torr. A low frequency RF power was applied on the wafer surface to enhance ion bombardment on the as-deposited films to improve the film quality, whereas a high frequency RF power was applied on the gas inlet to decompose the $SiH_4 + N_2O$ reaction gas mixtures for the deposition of silicon dioxide films. The films so deposited were subject to polishing with IC1000/Suba IV composite pad. The SC-1 slurry used for polishing consists of colloidal silica particles with size about 30 ~ 100 nm suspended in KOH solution with pH value at 10.0 to 10.5 at 22°C. The slurry was diluted with deionized (DI) water at different volume ratios. An IPEC 472 Avanti™ commercial CMP system was employed for the polishing experiments with ex situ pad conditioning and the wafer back-side pressure was held at 0.5 psi throughout the experiments.

The goal of the experiments for polishing parameter investigation is to find out the optimal polishing conditions for maintaining a reasonable removal rate while minimizing WIWNU for patterned wafer study. In this study, six CMP process parameters, namely, down force, platen rpm, carrier rpm, carrier oscillation speed, slurry flow rate, and slurry concentration, are chosen for this investigation. The L-25 orthogonal array experimental condition[3] is adopted to simplify the complex multivariable CMP experiments. The arrangement of parameters for all 25 sets of experiments and raw data results of removal rate and WIWNU are summarized in Table I. By means of the orthogonal design, the effects from other parameters can be considered as constant, since the average trend of a specific parameter due to the influences from other parameters are the same. For example, in Table I, the *R*/*R* results of slurry dilute % in the far right column represent the averages over the five rows with the same dilute %. The weighing and extent of all other parameters are the same for each value of dilute %. As a consequence, the influences from all other parameters are the same when the dilute % is varied. The same thing applies when other parameters are varied. By this method the sample size of this investigation can be reduced significantly.

Following the orthogonal array experiments, parametric experiments should be performed to eliminate the bias from possible dom-

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**Table I. Experimental conditions and results for the orthogonal array and parametric studies.**

| Experiment no. | Parameters/Variables | | | | | | Column 1 experimental results | |
|---|---|---|---|---|---|---|---|---|
| Experimental conditions Unit | Slurry dilute (%) | Slurry flow (sccm) | Down force (psi) | Platen rotation (rpm) | Carrier rotation (rpm) | Carrier oscillation (mm/s) | *R*/*R* of each row (nm/min) | *R*/*R* results of slurry dilute (%) (nm/min) |
| 1 | 200 | 100 | 2 | 30 | 30 | 2 | 61 | |
| 2 | 200 | 150 | 5 | 40 | 40 | 5 | 157 | |
| 3 | 200 | 200 | 8 | 50 | 50 | 8 | 265 | 224 |
| 4 | 200 | 250 | 11 | 60 | 60 | 11 | 250 | |
| 5 | 200 | 300 | 14 | 70 | 70 | 14 | 446 | |
| 6 | 150 | 100 | 5 | 50 | 60 | 14 | 159 | |
| 7 | 150 | 150 | 8 | 60 | 70 | 2 | 276 | |
| 8 | 150 | 200 | 11 | 70 | 30 | 5 | 398 | 253 |
| 9 | 150 | 250 | 14 | 30 | 40 | 8 | 364 | |
| 10 | 150 | 300 | 2 | 40 | 50 | 11 | 70 | |
| 11 | 100 | 100 | 80 | 70 | 40 | 11 | 264 | |
| 12 | 100 | 150 | 11 | 30 | 50 | 14 | 288 | |
| 13 | 100 | 200 | 14 | 40 | 60 | 2 | 433 | 250 |
| 14 | 100 | 250 | 2 | 50 | 70 | 5 | 73 | |
| 15 | 100 | 300 | 5 | 60 | 30 | 8 | 191 | |
| 16 | 50 | 100 | 11 | 40 | 70 | 8 | 334 | |
| 17 | 50 | 150 | 14 | 50 | 30 | 11 | 555 | |
| 18 | 50 | 200 | 2 | 60 | 40 | 14 | 69 | 272 |
| 19 | 50 | 250 | 5 | 70 | 50 | 2 | 180 | |
| 20 | 50 | 300 | 8 | 30 | 60 | 5 | 220 | |
| 21 | 0 | 100 | 14 | 60 | 50 | 5 | 624 | |
| 22 | 0 | 150 | 2 | 70 | 60 | 8 | 347 | |
| 23 | 0 | 200 | 5 | 30 | 70 | 11 | 128 | 283 |
| 24 | 0 | 250 | 8 | 40 | 30 | 14 | 263 | |
| 25 | 0 | 300 | 11 | 50 | 40 | 2 | 377 | |

Note: Characteristics of each parameter can be summed and an average taken since effects from other parameters can be assumed constant.

inance of certain parameters, and to provide precise and optimal value of each parameter for the verification of the trends acquired from orthogonal array experiment. In the parametric experiments, only one specified parameter is varied at a time while others are held at their mean value. Throughout the investigation of CMP polishing parameters, removal rate (*RR*) was taken as the average over 49 measurement points across the 150 mm wafers. Meanwhile, the WIWNU is defined as

$$WIWNU = \left[\left(\frac{RR_{\text{max}} - RR_{\text{min}}}{RR_{\text{avg}}}\right) \times \frac{1}{2}\right] \times 100\% \quad [1]$$

Patterned wafers with different metal line pitches (width + spacing) and oxides of different thickness deposited on top of them were subject to polishing by the optimal polishing conditions achieved based on the aforementioned experimental setup. The layout rules of the CMP test patterns are listed in Table II. To map out the optimal CVD/CMP process integration strategies between planarization performance and process cost, cross-sectional SEM and across-chip long scan profiles were both conducted. The rule of INTEGRATE was then proposed to evaluate the CMP process performance of silicon oxide film for the integration of CVD and CMP processes.

**Table II. The layout rule of metal line test pattern used in this study.**

| Metal width/ metal spacing (μm) | 0.6 | 2 | 5 | 20 | 100 |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 4 |
| 10 | 1 | 1 | 1 | 6 | 1 |
| 35 | 1 | 1 | 6 | 1 | 1 |
| 70 | 1 | 6 | 1 | 1 | 1 |
| 10 | 4 | 1 | 1 | 1 | 1 |

Note 1. The numbers stand for the number of repeating patterns.
2. Pattern density = width/(width + spacing).
3. Pattern modules are separated by 20 μm.

## Results and Discussion

*Effects of slurry: physical aspects.*—Results of the orthogonal array (Ort.) and parametric (Par.) experiments are displayed in Fig. 1 to 6. The removal rate (*RR*) and nonuniformity (*NU*) for the orthogonal array experiments are taken as the average over results of the five experimental conditions at the specified parameter. For the parametric experiments, the *RR* and *NU* are determined with the controlled parameter while keeping other parameters at their mean values, as described before.

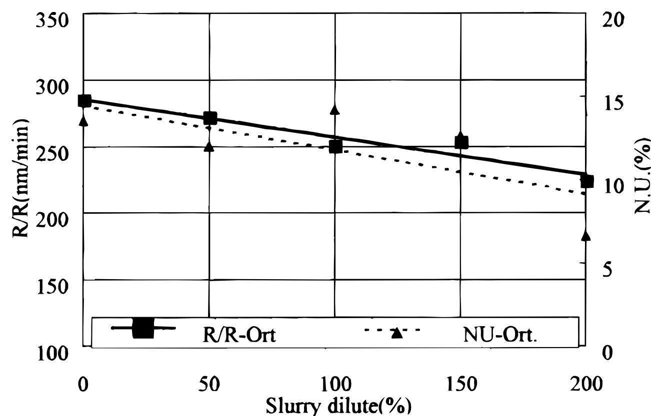


**Figure 1.** Orthogonal array results of slurry dilute % vs. *R*/*R* and *NU*%.

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Figure 1 shows the polishing results of slurry dilute percentage vs. PECVD silicon oxide removal rate (*RR*) and nonuniformity (*NU*). Both *RR* and *NU* were found to decrease as more DI water was added, reducing the viscosity and silica particle concentration in the slurry. The slurry pH, on the other hand, did not change due to dilution. The lowered removal rates can be attributed to the reduction in scrubbing efficiency between abrasives and the oxide surface, since the number of abrasive particles per unit volume of slurry has been reduced due to dilution. Meanwhile the lower nonuniformity is probably the consequence of the decreased slurry viscosity, which gives rise to enhanced hydrophilicity and improved wettability between slurry and oxide surface. As a result, the contact between the slurry and wafer surface is more uniform, leading to a decrease in polishing nonuniformity. Based on the results above, a fixed slurry dilution percent of 200% was chosen for further study considering the trade-off between *RR* and nonuniformity.

Figure 2 illustrates the impacts of slurry flow rate upon *RR* and nonuniformity from orthogonal and parametric experiments, respectively. The removal rate decreases while the nonuniformity increases with increasing slurry flow rate, as exhibited in both the orthogonal and parametric experimental results in Fig. 2.

Certainly, the slurry flow rate considered here does not represent the true fluid flow across the wafer surface in any case. However, with a higher slurry flow rate dripping down onto the platen surface, more slurry (and abrasive particles as well) will get carried into the fluid layer along the wafer pad interface by the relative motion between the carrier and platen, leading to a thicker fluid layer. According to the asperity contact model,[4] the existence of thicker fluid layer would result in semidirect or even indirect contact, both of which reduce the contact area between wafer and pad. Besides, as the contact area is reduced, the actual down force exerted by the abrasive particles onto the wafer is lowered on the microscopic scale.[5] The two scenarios described above would result in reduction in nonuniformity and removal rate, respectively. Besides, since the chemical erosion during oxide CMP is a highly sensitive temperature-dependent process,[6] the increased influx of the "cooler" slurry (22°C) into the wafer carrier would aggravate the temperature nonuniformity across wafer surface, which was originally in contact with the pad at a higher temperature induced by the "hotter" polishing platen (37°C). This thermal effect, too, would contribute to the decreases in *RR* and *NU*. The results in Fig. 2 are similar to at least one previous study.[7]

*Effects of down force*.—Figures 3 shows the effects of polishing down force pressure on removal rate and nonuniformity determined from orthogonal array experiments. Clearly, a higher down force pressure leads to a higher removal rate and lower nonuniformity. The removal rates exhibit a nearly linear dependence on down force, in accordance with the Preston equation[8] or other removal rate model.[9] On the other hand, *NU* displays a declining trend with increasing applied down force. This can be attributed to the fact that, under a higher down force pressure, the wafer surface would conform more uniformly to the pad, leading to a more uniform pressure distribution across the wafer and thus a lower polish nonuniformity.[10] A similar trend, i.e., the decrease of NU with increasing down force, was also observed in other experimental studies with the same[11] or different[12] type of rotary polish tool. The increase in *RR* and decrease in *NU* with increasing down force may not be definite, however, since, as the down force increases, the pad surface features and hence the slurry holding capacity would deteriorate in an ever faster rate due to intensified mechanical abrasion. As a result, the removal rate starts to decline and the nonuniformity elevates when the down force is increased over a certain level, as found in one previous study.[13] Compared with other machine variables, the results also show that the down force plays the dominant role in changing *RR* and *NU*. Similar results have also been reported in various studies.[10-12]

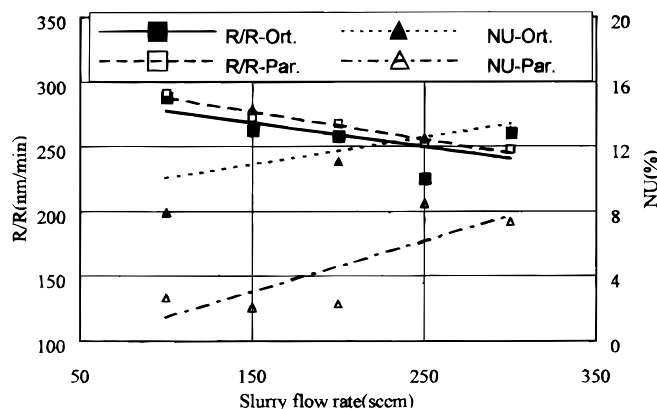


**Figure 2.** Orthogonal array (Ort.) and parametric (par.) experimental results of slurry flow rate vs. *R/R* and *NU*%.

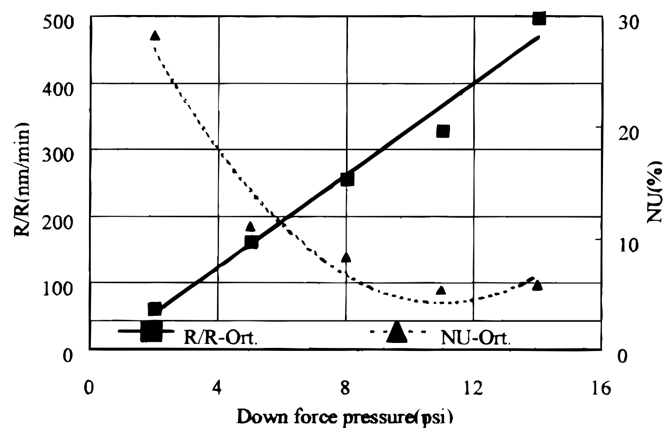


**Figure 3.** Orthogonal array results of down force pressure vs. *R/R* and *NU*%.

*Effects of kinematics*.—Both the orthogonal array and parametric experiment results in Fig. 4 suggest that removal rate can be raised by increasing the platen rotation speed. Specifically, based on the results of parametric study, the removal rate exhibits a nonlinear (platen rpm)$^{1/2}$ dependence from the parametric results. Such a deviation from Preston equation has been found and reported previously and in close agreement with one removal rate model, which states that[9]

$$RR = M\,P^{5/6}\,V^{1/2} \quad [2]$$

where *M* is a weighing factor related to the materials, chemical, and other processes during CMP; *P* is the down force; and *V* is the relative velocity between platen and carrier. Compared with the Preston

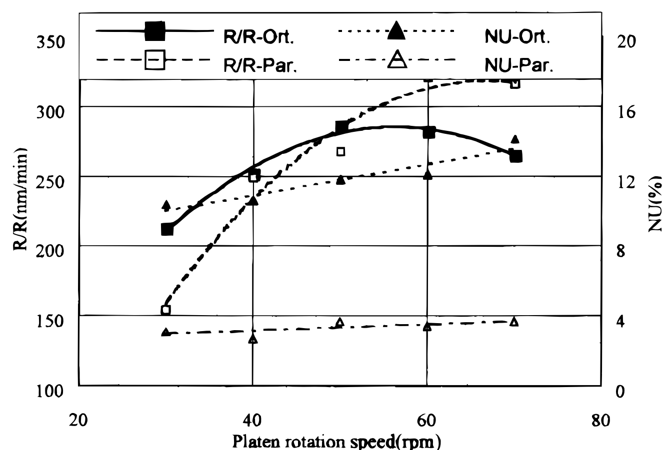


**Figure 4.** Orthogonal array and parametric experimental results of platen rpm vs. *R/R* and *NU*%.

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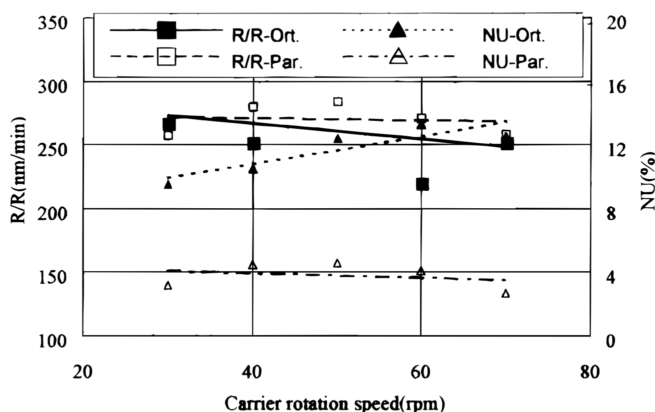


**Figure 5.** Orthogonal array and parametric experimental results of carrier rpm vs. $R/R$ and $NU$%.

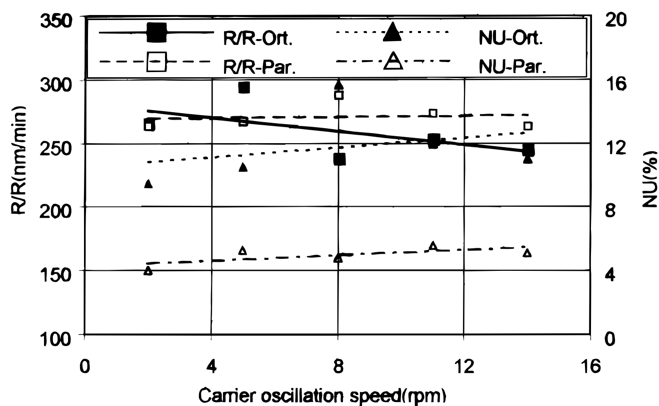


**Figure 6.** Orthogonal array and parametric experimental results of carrier oscillation speed vs. $R/R$ and $NU$%.

equation ($RR = K_pPV$, where $K_p$ is the Preston coefficient), this removal rate model prescribes a weaker dependence of *RR* on velocity than on down force. In fact, across comparison between Fig. 3 and 4 does reveal such a trend.

From the orthogonal array results in Fig. 4, however, a peak removal rate is found at a platen rotation of ~50 rpm, over which *RR* decreases gradually. This is consistent with the report by Sivaram et al.[1] that too high a platen speed may elevate pad glazing and enlarge the net contract area between the pad and the wafer, reducing the local down force pressure across wafer surface and hence the removal rate. Besides, the pad glazing effect would also degrade the slurry distribution uniformity over the pad, resulting in a slight increase in *NU*. Note that, in the current study, *NU* increases over the range of platen rpm investigated (30~70 rpm). On the other hand, *NU* was found to decrease in the lower platen rpm range (10~28 rpm)[11] with the same type of polishing tool. Such a transitional behavior can be a direct consequence of the variation in the relative velocity of a fixed point on the wafer with the platen rpm. Results of kinematic analysis indicate that at platen rpm below 30 rpm, and carrier rpm equal to 50 rpm (the same as used in the present study), the nonuniformity of relative velocity decreases with increasing platen rpm,[14] consistent with the trend of polish *NU*.

The effects of carrier rpm on the polish process are displayed in Fig. 5. Compared with Fig. 4, obviously, carrier rpm plays a minor role in *RR* and *NU*. Both *RR* and *NU* exhibit slim variations over the rpm range investigated. Again, this behavior is rationalized from the polish kinematics,[14] which can be perceived more easily from a simple geometric argument[11] that the larger platen will render a longer distance traveled by a point on the wafer per unit time than the smaller carrier does. In general, based on the kinematics for a rotary CMP system,[14] the combination of a high platen rpm and a low carrier rpm would give rise to a high relative velocity which leads to a high *RR*; and a more uniform distribution of distance traveled, which would result in a relatively low polish *NU*.

The effect of carrier oscillation speed across the polishing pad is also examined in this study. As Fig. 6 indicates, *RR* remains virtually unchanged and *NU* exhibits a slight increase as the oscillation speed increases from 2 to 14 mm/s. Notice that the axial oscillation speed (about $10^0$~$10^1$ mm/s) of the carrier is small compared with the platen and carrier rpm (about $10^3$ mm/s). Therefore, it adds only a small axial component to the velocity during polishing and would not contribute significantly to the relative velocity ($V$) term in Eq. 2 and hence to the removal rate. Regarding the polish *NU*, a greater distance between the centers of carrier and platen would induce a higher degree of velocity uniformity, according to the kinematics of the polish tool.[14] Therefore, contrary to common belief, a greater oscillation speed would disrupt, instead of improve, the polish uniformity, since it brings the carrier close to the center of platen and disturbs the distribution of velocity across wafer, as shown in Fig. 6. Given the above, however, a reasonable carrier oscillation speed is still adopted during manufacturing in light of long-term process reproducibility and polishing pad life concerns.

Once the parametric results are obtained the trend chart and polishing process conditions for device wafer study can be selected. This is given in Table III. A removal rate greater than 200 nm/min and a within-wafer nonuniformity of less than 4% are used as the criteria to determine the optimized process. The above polish conditions are implemented and integrated with CVD oxide and IMD planarization processes, as discussed in the next section.

*IMD and CMP process optimization and integration: planarization issues*.—Once polishing variables are optimized, the optimization of CVD silicon oxide thickness and the reduction in CMP process time for the planarization of IMD become the major integration concerns. Specifically, the process thus developed has to avoid over polishing in the center of wide intrametal line spacing, while allowing a wide enough process latitude to achieve a high degree of planarization, a high efficiency of planarization, and to compensate for the CMP-induced within-chip nonuniformity[15] during polishing of the IMD layer for ULSI device processing.

**Table III. A summary of results of the characteristics of CMP polishing parameters derived from the experimental design in Table I.**

| Factor Increased Unit | Slurry dilution (%) | Slurry flow (sccm) | Down force (psi) | Platen rotation (rpm) | Carrier rotation (rpm) | Carrier oscillation (mm/s) |
|---|---|---|---|---|---|---|
| Experimental conditions | 0, 50, 100, 150, 200 | 100, 150, 200, 250, 300 | 2, 5, 8, 11, 14 | 30, 40, 50, 60, 70 | 30, 40, 50, 60, 70 | 2, 5, 8, 11, 14 |
| Removal rate R/R | ↘ | ~ | ↑ | ↗↘ | ~ | ~ |
| Nonuniformity | ↘ | ↗ | ↓ | ↗ | ~ | ~ |
| Polish recipe used | 200 | 200 | 11 | 40 | 40 | 5 |
| Symbol | ↘ slow decrease | ↗ slow increase | ↓ fast decrease | ↑ fast increase | ↗↘ with peak value | ~ no effect |

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To evaluate the gap-fill performance of dielectric deposition process, a step height ratio ($SH\%$) is defined according to the features in Fig. 7

$$SH\% = \left(\frac{H_d^i}{H_m}\right) \times 100\% \quad [3]$$

where $H_m$ is the height of the metal feature, and $H_d^i$ is the prepolish step height (initial step height) resulting from dielectric deposition process. For typical CVD process, the $SH\%$ might be higher than 100% due to poor bottom step coverage. For the dielectric process with self-planarizing capability (e.g., SOG), the step height can be reduced to a certain degree. Pre-CMP planarization treatments, such as plasma etchback, also reduce the step height from deposition. Thus not only the metal patent step height, but also the pre-CMP dielectric planarization capability should be taken into account when implementing the IMD-CMP process. To evaluate the planarization performance, the degree of planarization (%*DOP*) is used

$$\%DOP = \frac{(H_d^i - H_d^f)}{H_d^i} \times 100\% \quad [4]$$

where $H_d^f$ is the final step height of the dielectric (oxide).

The performance of planarization can also be assessed by the efficiency of planarization (%*EOP*)

$$\%EOP = \left(\frac{T_r - T_d}{T_r}\right) \times 100\% \quad [5]$$

where $T_r$ is the dielectric thickness removed by CMP on top of metal line, $T_d$ is oxide thickness loss at the center area of wide space of intrametal line. The IMD is considered fully planarized when the topography is eliminated, that is, a 100% *DOP* is achieved. Additionally, 100% *EOP* should be obtained to insure the absence of intrametal line oxide loss.

The effect of intrametal line oxide loss as shown in Fig. 7 results from thinning of the gap-fill dielectric at the center area of wide space of intrametal line. The polishing pad conforms to the surface topography of the wafer so that the "down" feature is being polished simultaneously with the "up" feature, leading to slightly polishing the recess area. Apparently, according to Fig. 7 and Eq. 5, a large amount of polishing of the recess area will lead to severe loss in %*EOP*. In order to avoid this detrimental effect, thicker films are usually deposited first and subject to polish subsequently until global planarization is achieved. Such a practice is also used to compensate for the lower %*EOP* at the wider intraline recess area ($\%EOP_W$) than at the narrower intraline recess area ($\%EOP_N$), with the disadvantages of higher CVD and CMP process costs. Such a dilemma should be resolved by considering the $SH\%$ (related to dielectric deposition process) and %*EOP* (related to CMP performance) simultaneously. Quantitative analysis for such a pattern-density-dependent efficiency of planarization is required in order to lay out a better integration scheme for the CVD and CMP processes.

The correlation between pattern density and efficiency of planarization is investigated by chip-level long scan profiler through different module of pattern density. Detail metal pattern density is described in Table II. From results of thickness measurement and topography scanning, the efficiency of planarization (%*EOP*) for each pattern density can be calculated and the result is plotted against CMP polish time with various metal pattern density in Fig. 8. The intermetal dielectrics deposited contain 700 nm subatmospheric CVD oxide as the gap-fill layer followed by a 1600 nm plasma-enhanced CVD tetraethoxysilane (TEOS) oxide as the CMP sacrificial layer. The polishing conditions summarized in Table III are adopted for planarization. This would give a removal rate of ~200 nm/min on blanket oxide wafers. The results suggest that loss in %*EOP* due to pad deformation induced polishing at recess area is more severe at shot polish times with wide interconnect spacing. At narrow metal spacing, the topography of the dielectric deposited is nearly planarized so that a short CMP step would quickly bring it to full planarization. While, for wide metal spacing, the large topographical variation of the IMD layer would induce a lower difference in *RR* between the up and down features and hence a higher degree of polishing at the recess area, which would require a longer polish time to compensate. the planarization rate is obviously a function of the step height and pattern density. In this study, the planarization rate can be approximated as the rate of change in %*EOP* with time, which combined with the Burke's model,[16] can be expressed as

$$\frac{d(\%EOP)}{dt} \cong \frac{(1 - D_o)}{H_d^i} H_d RR_u + C \quad [6]$$

where $D_o$ is the ratio of the removal rate of the "down" feature to "up" features; $H_d$ is the instantaneous step height during CMP; $RR_u$ is the removal rate of the "up" feature; and $C$ is the residue variation. Equation 6 states that the planarization rate is proportional to step height ($H_d$) so that as polish progresses, the step height reduces and the planarization rate slows down accordingly. This can be perceived from the change in slope with time of %*EOP* in Fig. 8. Difficulties arise, however, when it comes to determine $D_o$ and $RR_u$. Since the removal rates of "down" and "up" features vary with metal spacing, $D_o$ is actually a function of pattern density. On the other hand, although $RR_u$ is approximately equal to the blanket removal rate for narrow metal spacing (e.g., 1 μm in the present case), it would be much greater for wide metal spacings. Both the pattern-density-related issues above make it complicated when Eq. 6 is applied to model the planarization performance.

Based on the planarization model incorporating the pattern density effect,[17,18] the final IMD thickness $T$ at a given point on a chip can be expressed as a function of global pattern density $d$

$$T = T_o + kT_h(d - d_o) + \delta \quad [7]$$

where $T_o$ is the target IMD thickness, $T_h$ is the metal height, $d_o$ is the median global metal pattern density, $k$ is the fitting parameter to account for the effective step height, and $\delta$ is the residue variation. Equation 7 predicts a linear relationship between the pattern density and IMD thickness when the features are planarized for a long enough time. This can serve as a guideline for the CMP process

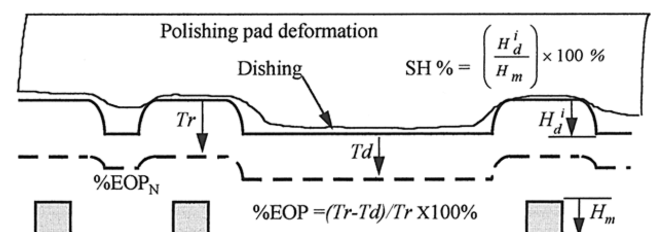


**Figure 7.** The definitions of dishing, $SH\%$ and %*EOP*.

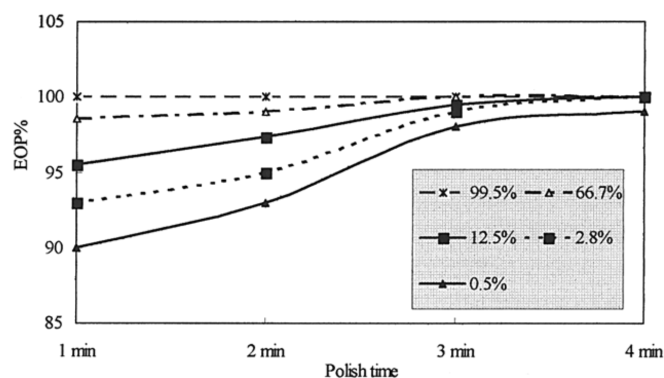


**Figure 8.** Efficiency of planarization (%*EOP*) vs. polishing time for wafers with different pattern density.

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design given known pattern density and initial step height. This point is elaborated later.

*IMD and CMP process optimization and integration: integration issues.*—As pointed out in the previous section, the IMD thickness left to be planarized has to be considered for a full implementation and integration of IMD and CMP processes. Figure 9 illustrates the mimic IMD profile over different interconnect spacing. The required minimum IMD thickness to be deposited is denoted as $T_t$; the minimum required post-CMP oxide thickness from the device isolation concern is denoted as $T_i$, and maximum metal step height (or topography) is denoted as $T_h$, the same as in Eq. 7. The rule for determining CMP polishing time, $t_p$, or the IMD thickness, $T_t$, can then be formulated

$$t_p = \left\{\left[\left(T_h\ SH\%\right) + T_i\right]\left[1 + NU\right]\left(\frac{1}{\%EOP}\right)\right\}\left[\frac{1}{(RR_{avg} \pm \sigma)}\right] \quad [8]$$

where $RR_{avg}$ and σ are within-wafer average removal rate (*RR*) and removal rate variation, respectively; and *NU* is the abbreviation for WIWNU. For ideal IMD and CMP processes, i.e., $SH\% = \%EOP = 100\%$, $NU = 0$, and Eq. 8 reduces to

$$t_p = (T_i + T_h)/RR_{AVG} \quad [9]$$

In reality, since 100 SH% is rarely achieved in the IMD process, it should be incorporated into the thickness rule to correct the maximum step height. Similarly, from the viewpoint of device isolation requirement, a factor of $(1/EOP\%)$ should be multiplied with the $[1 + NU]$ term to compensate for the thickness variation due to nonideal planarization efficiency and polish nonuniformity.

From Eq. 8, the IMD oxide thickness ($T_c$) to be deposited for process integration would be

$$T_c = [(T_h\ SH\%) + T_i][1 + NU]\left(\frac{1}{EOP\%}\right) \quad [10]$$

CMP polishing time can be acquired by multiplying $t_c$ with CMP average remove rate, which incorporates removal rate variation (σ). In this equation $T_h$, $T_i$ are prespecified, whereas $RR_{avg}$, $SH\%$, $\%EOP$, and σ are determined from experiments. Based on Eq. 8 and Eq. 10, IMD oxide thickness can be calculated and predicted before deposition. Moreover evaluation of the CMP process performance such as $\%EOP$ and removal rate variation (σ) can be executed from the predetermined oxide thickness. To account for the influence of pattern density, Eq. 8 is further modified by combining it with Eq. 7. Setting $T_o = T_i$, this yields

$$T_c = \{T + T_h[SH\% - k(d - d_0)] + \delta\}[1 + NU]\left(\frac{1}{EOP\%}\right) \quad [11]$$

and the total polish time can be estimated as

$$t_p = \{T + T_h[SH\% - k(d - d_0)] + \delta\}[1 + NU]\left(\frac{1}{EOP\%}\right)\left[\frac{1}{RR_{avg} \pm \sigma}\right] \quad [12]$$

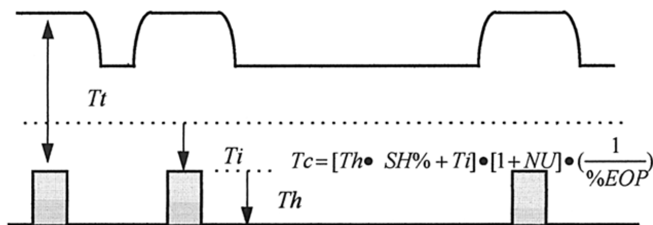


**Figure 9.** Schematic representation of the optimized IMD thickness rule in Eq. 10.

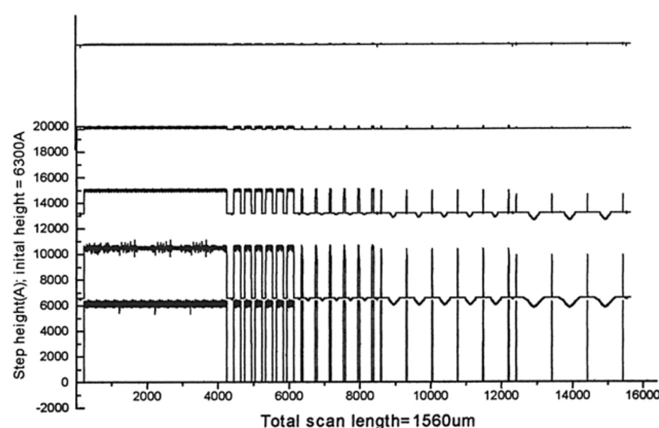


**Figure 10.** Chip-level long scan profiler measurement results over a distance of 1560 μm before polishing, after 1, 2, 3, and 4 min of polishing.

Equations 11 and 12 suggest that a thinner IMD layer or a shorter polish time is required to achieve planarization in an area with high pattern density (narrow metal spacing). Equations 11 and 12 incorporate integral nonuniformity, thickness of dielectric, efficiency of planarization, geometry of device, and removal rate and its variation for CMP polishing time estimation, and are thus termed INTEGRATE. This result is consistent with the trends shown in Fig. 8.

To demonstrate the feasibility of the rule of INTEGRATE, a sample polish process is described below. For patterned wafers with 100 μm interconnect spacing, the removal rate deviation is 10%, and the *EOP* and *SH* are 90 and 100%, respectively. Based on Eq. 10, to planarize the IMD to a minimum remaining oxide thickness of 600 nm, it would take a CVD oxide thickness within the range between 1613 and 1467 nm, with or without considering the 10% removal rate deviation across the wafer. Figure 10 shows results of long scan profiler measurement of chip-level topography variation per each polishing interval of 1 min. The measurements indicate that, to achieve global planarization, 4 min of polishing is required. Figures 11 and 12 show the cross-sectional SEM micrographs of post-CMP topography with initial oxide thickness of 1200 and 1500 nm over the metal pattern, respectively, which support the micro view result of a long scan profiler. To planarize the 100 μm interconnect spacing free of recess, the oxide remaining is about 400 nm thick in samples with an initial oxide thickness of 1200 nm. Such a remaining oxide thickness is insufficient since the device specifications require at least a 600 nm IMD for isolation purpose. Conversely, the sample with an initial oxide thickness of 1500 nm in

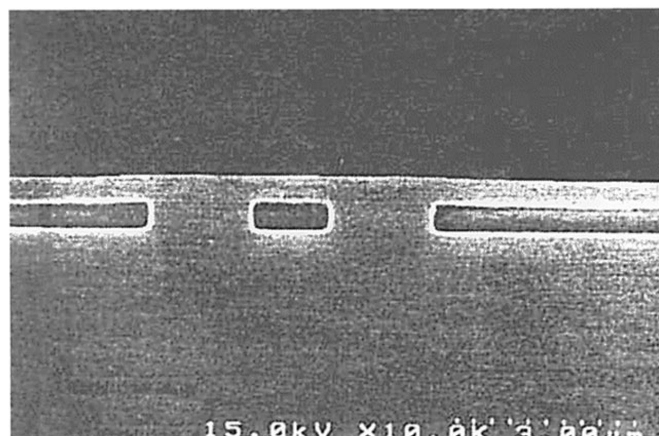


**Figure 11.** Features with an initial (deposited) oxide thickness of 1200 nm polished back to 400 nm shows insufficient oxide thickness for IMD application.

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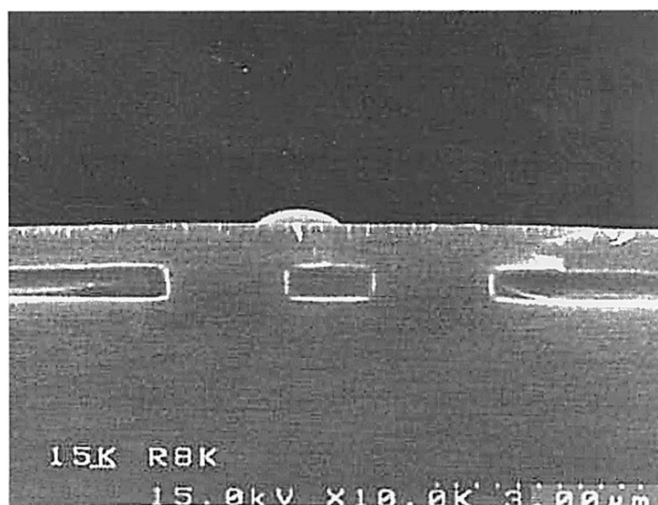


**Figure 12.** Features with an initial (deposited) oxide thickness of 1500 nm polished back to 670 nm shows sufficient oxide thickness for IMD application.

Fig. 12 yields a remaining oxide thickness of 670 nm, which meets the requirement. The above process integration scheme based on the rule of INTEGRATE considers concurrently both IMD geometric factors and CMP polishing performances for the approximation of the required IMD thickness and CMP polish time. The actual device wafer with excellent global planarization shown in Fig. 13 demonstrates the effectiveness and feasibility of the rule of INTEGRATE for providing the successful process integration results.

## Conclusion

An integrated IMD/CMP process is developed in this study. Experimental design by means of orthogonal array and parametric studies is executed to characterize and evaluate the effects of machine parameters on the polishing process. Down force pressure is found to be the dominant mechanical attribute to the polish process, affecting both removal rate and within-wafer nonuniformity remarkably. Platen rpm plays a secondary role in the polish process while the effects of other parameters, such as percent slurry dilution, slurry flow rate, carrier rpm, and carrier oscillation, are marginal compared with those of down force and platen rpm. Optimized CMP process latitude is extracted from results of the experimental design.

Patterned wafers with different metal pitches and different dielectric thickness on top are subjected to polishing with the optimized CMP process developed. Wafers with narrow metal spacing achieve 100% efficiency of planarization within a relatively short time. Based on polishing results with various polishing time and IMD thickness, the rule of INTEGRATE is proposed for estimating the required IMD thickness to be deposited and the optimal polishing time for an integrated solution to the IMD/CMP process. Excellent planarity is demonstrated through experiments based on the optimal polish conditions and the rules proposed.

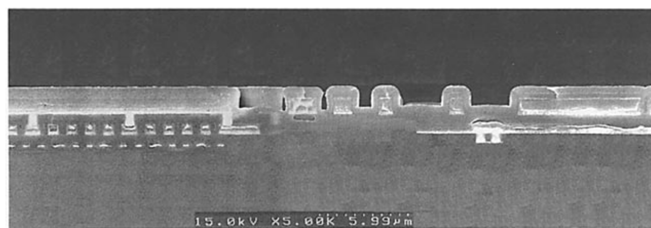


**Figure 13.** Global planarization achieved using the polishing conditions derived in Table III.

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